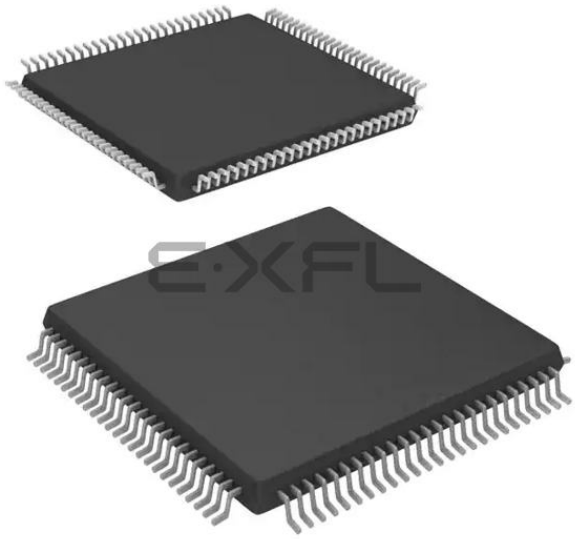

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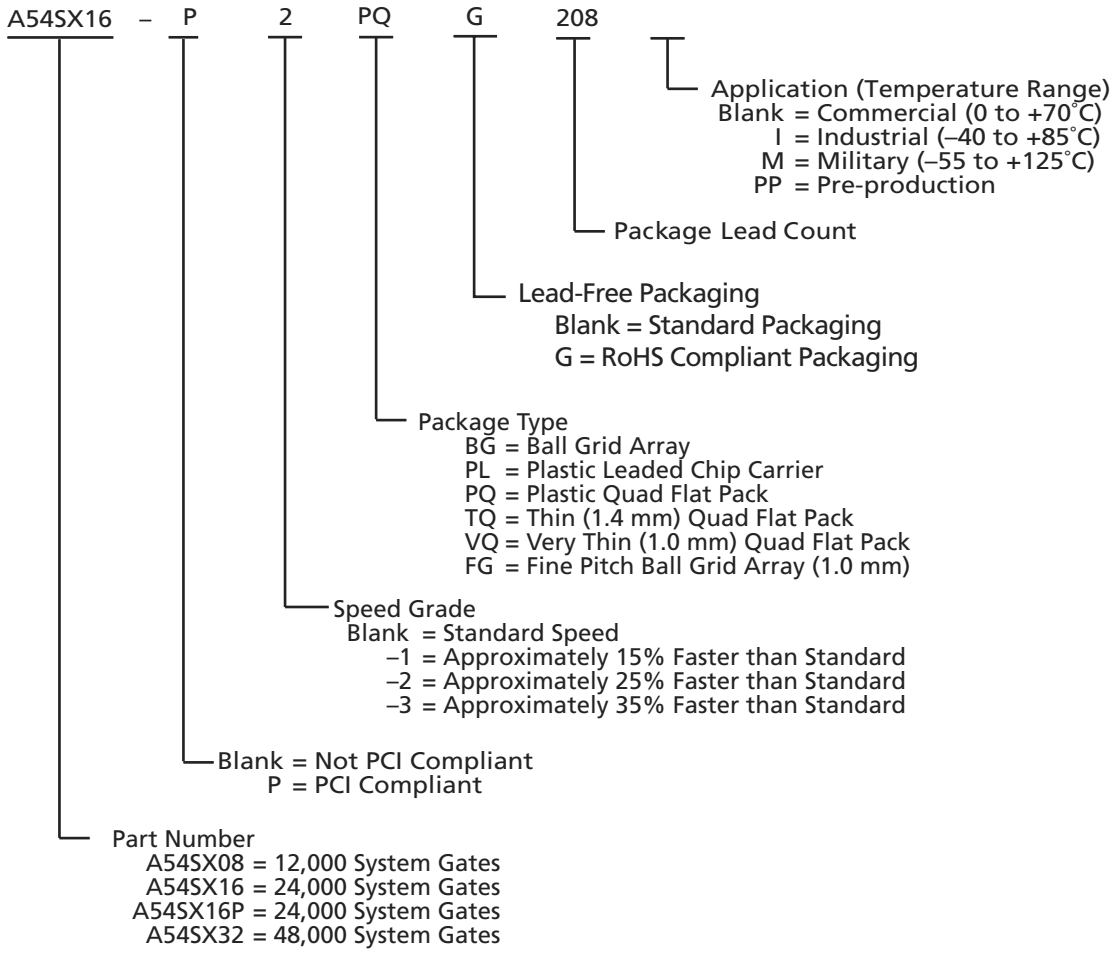
Details	
Product Status	Obsolete
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	12000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx08-2vq100i

Ordering Information



Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PLCC 84-Pin	VQFP 100-Pin	PQFP 208-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 313-Pin	PBGA 329-Pin	FBGA 144-Pin
A54SX08	69	81	130	113	128	–	–	111
A54SX16	–	81	175	–	147	–	–	–
A54SX16P	–	81	175	113	147	–	–	–
A54SX32	–	–	174	113	147	249	249	–

Note: *Package Definitions (Consult your local Actel sales representative for product availability):*
PLCC = Plastic Leaded Chip Carrier
PQFP = Plastic Quad Flat Pack
TQFP = Thin Quad Flat Pack
VQFP = Very Thin Quad Flat Pack
PBGA = Plastic Ball Grid Array
FBGA = Fine Pitch (1.0 mm) Ball Grid Array

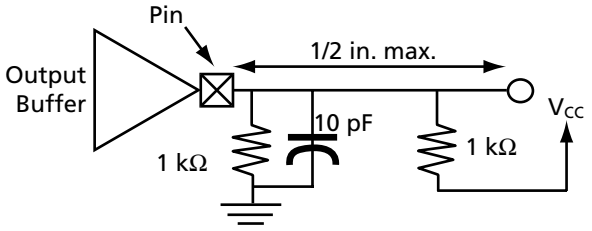
A54SX16P AC Specifications for (PCI Operation)

Table 1-7 • **A54SX16P AC Specifications for (PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 1.4$[1]	–44		mA
		$1.4 \le V_{OUT} < 2.4$[1, 2]	$–44 + (V_{OUT} – 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}$[1, 3]		EQ 1-1 on page 1-11	
	(Test Point)	$V_{OUT} = 3.1$[3]		–142	mA
$I_{OL(AC)}$	Switching Current High	$V_{OUT} \ge 2.2$[1]	95		mA
		$2.2 > V_{OUT} > 0.55$[1]	$V_{OUT}/0.023$		
		$0.71 > V_{OUT} > 0$[1, 3]		EQ 1-2 on page 1-11	mA
	(Test Point)	$V_{OUT} = 0.71$[3]		206	mA
I_{CL}	Low Clamp Current	$–5 < V_{IN} \le –1$	$–25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load[4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load[4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 1-9 on page 1-11. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half-size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 1-9 on page 1-11. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*



A54SX16P AC Specifications (3.3 V PCI Operation)

Table 1-9 • **A54SX16P AC Specifications (3.3 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CC}$ [1]			mA
		$0.3V_{CC} \le V_{OUT} < 0.9V_{CC}$ [1]	$-12V_{CC}$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}$ [1, 2]	$-17.1 + (V_{CC} - V_{OUT})$	EQ 1-3 on page 1-14	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$ [2]		$-32V_{CC}$	mA
$I_{OL(AC)}$	Switching Current High	$V_{CC} > V_{OUT} \ge 0.6V_{CC}$ [1]			mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}$ [1]	$16V_{CC}$		mA
		$0.18V_{CC} > V_{OUT} > 0$ [1, 2]	$26.7V_{OUT}$	EQ 1-4 on page 1-14	mA
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ [2]		$38V_{CC}$	
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$-3 < V_{IN} \le -1$	$25 + (V_{IN} - V_{OUT} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate[3]	$0.2V_{CC}$ to $0.6V_{CC}$ load	1	4	V/ns
$slew_F$	Output Fall Slew Rate[3]	$0.6V_{CC}$ to $0.2V_{CC}$ load	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*

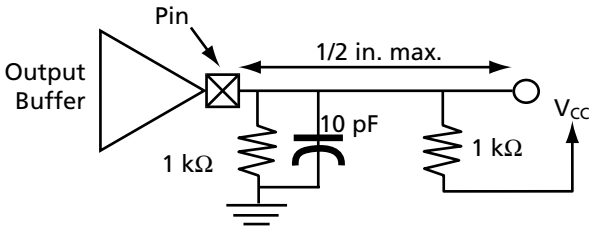


Figure 1-10 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

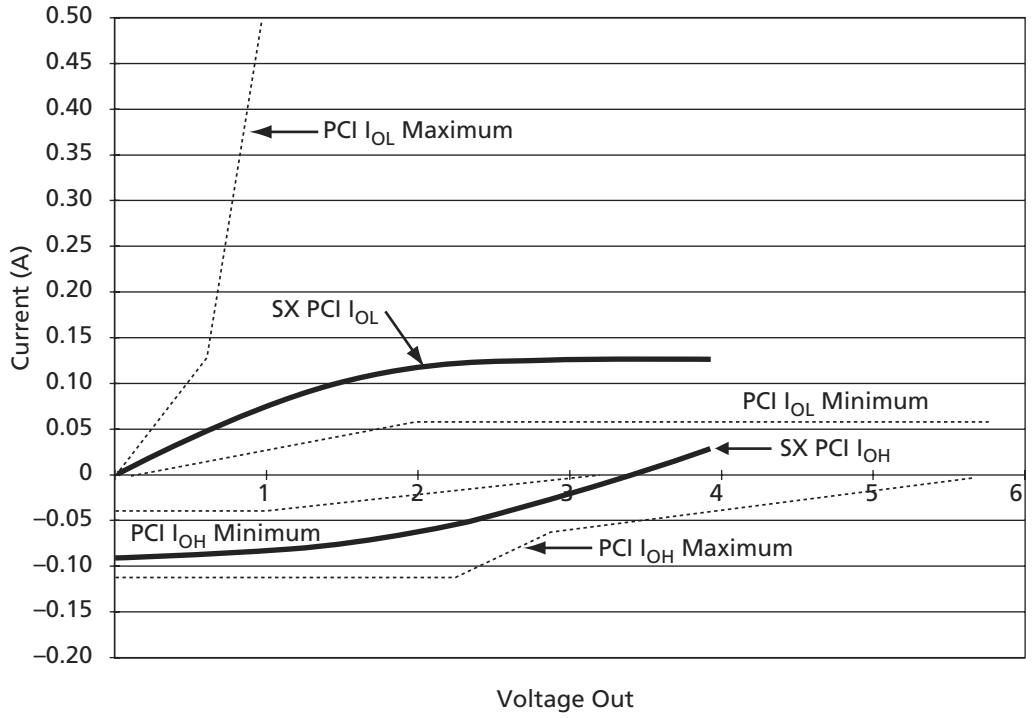


Figure 1-10 • **3.3 V PCI Curve for A54SX16P Device**

$$I_{OH} = (98.0/V_{CC}) \times (V_{OUT} - V_{CC}) \times (V_{OUT} + 0.4V_{CC})$$
$$\text{for } V_{CC} > V_{OUT} > 0.7\ V_{CC} \qquad \textit{EQ 1-3}$$

$$I_{OL} = (256/V_{CC}) \times V_{OUT} \times (V_{CC} - V_{OUT})$$
$$\text{for } 0\ V < V_{OUT} < 0.18\ V_{CC} \qquad \textit{EQ 1-4}$$

Table 1-13 shows capacitance values for various devices.

Table 1-13 • **Capacitance Values for Devices**

	A54SX08	A54SX16	A54SX16P	A54SX32
C_{EQM} (pF)	4.0	4.0	4.0	4.0
C_{EQI} (pF)	3.4	3.4	3.4	3.4
C_{EQO} (pF)	4.7	4.7	4.7	4.7
C_{EQCR} (pF)	1.6	1.6	1.6	1.6
C_{EQHV}	0.615	0.615	0.615	0.615
C_{EQHF}	60	96	96	140
r_1 (pF)	87	138	138	171
r_2 (pF)	87	138	138	171

Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A54SX16P device. A pattern of 0101… was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101… caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

Table 1-14 • **Power Consumption Guidelines**

Description	Power Consumption Guideline
Logic Modules (m)	20% of modules
Inputs Switching (n)	# inputs/4
Outputs Switching (p)	# outputs/4
First Routed Array Clock Loads (q_1)	20% of register cells
Second Routed Array Clock Loads (q_2)	20% of register cells
Load Capacitance (C_L)	35 pF
Average Logic Module Switching Rate (f_m)	f/10
Average Input Switching Rate (f_n)	f/5
Average Output Switching Rate (f_p)	f/10
Average First Routed Array Clock Rate (f_{q1})	f/2
Average Second Routed Array Clock Rate (f_{q2})	f/2
Average Dedicated Array Clock Rate (f_{s1})	f
Dedicated Clock Array Clock Loads (s_1)	20% of regular modules

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{Total} = P_{AC} \text{ (dynamic power)} + P_{DC} \text{ (static power)}$$

EQ 1-9

AC Power Dissipation

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

EQ 1-10

$$P_{AC} = V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + (n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + (0.5\ (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + (0.5\ (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2}))_{RCLKB} + (0.5\ (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]$$

EQ 1-11

Step 1: Define Terms Used in Formula

	V_{CCA}	3.3
Module		
Number of logic modules switching at f_m (Used 50%)	m	264
Average logic modules switching rate f_m (MHz) (Guidelines: f/10)	f_m	20
Module capacitance C_{EQM} (pF)	C_{EQM}	4.0
Input Buffer		
Number of input buffers switching at f_n	n	1
Average input switching rate f_n (MHz) (Guidelines: f/5)	f_n	40
Input buffer capacitance C_{EQI} (pF)	C_{EQI}	3.4
Output Buffer		
Number of output buffers switching at f_p	p	1
Average output buffers switching rate f_p(MHz) (Guidelines: f/10)	f_p	20
Output buffers buffer capacitance C_{EQO} (pF)	C_{EQO}	4.7
Output Load capacitance C_L (pF)	C_L	35
RCLKA		
Number of Clock loads q_1	q_1	528
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q1}	200
Fixed capacitance (pF)	r_1	138
RCLKB		
Number of Clock loads q_2	q_2	0
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q2}	0
Fixed capacitance (pF)	r_2	138
HCLK		
Number of Clock loads	s_1	0
Variable capacitance of dedicated array clock (pF)	C_{EQHV}	0.615
Fixed capacitance of dedicated array clock (pF)	C_{EQHF}	96
Average clock rate (MHz)	f_{s1}	0

Step 2: Calculate Dynamic Power Consumption

$V_{CCA} \times V_{CCA}$	10.89
$m \times f_m \times C_{EQM}$	0.02112
$n \times f_n \times C_{EQI}$	0.000136
$p \times f_p \times (C_{EQO}+C_L)$	0.000794
$0.5\ (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1})$	0.11208
$0.5(q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2})$	0
$0.5\ (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1})$	0

P_{AC} = 1.461 W

Step 3: Calculate DC Power Dissipation

DC Power Dissipation

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + X \times V_{OL} \times I_{OL} + Y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-12

For a rough estimate of DC Power Dissipation, only use $P_{DC} = (I_{standby}) \times V_{CCA}$. The rest of the formula provides a very small number that can be considered negligible.

$P_{DC} = (I_{standby}) \times V_{CCA}$

P_{DC} = .55 mA × 3.3 V

P_{DC} = 0.001815 W

Step 4: Calculate Total Power Consumption

$P_{Total} = P_{AC} + P_{DC}$

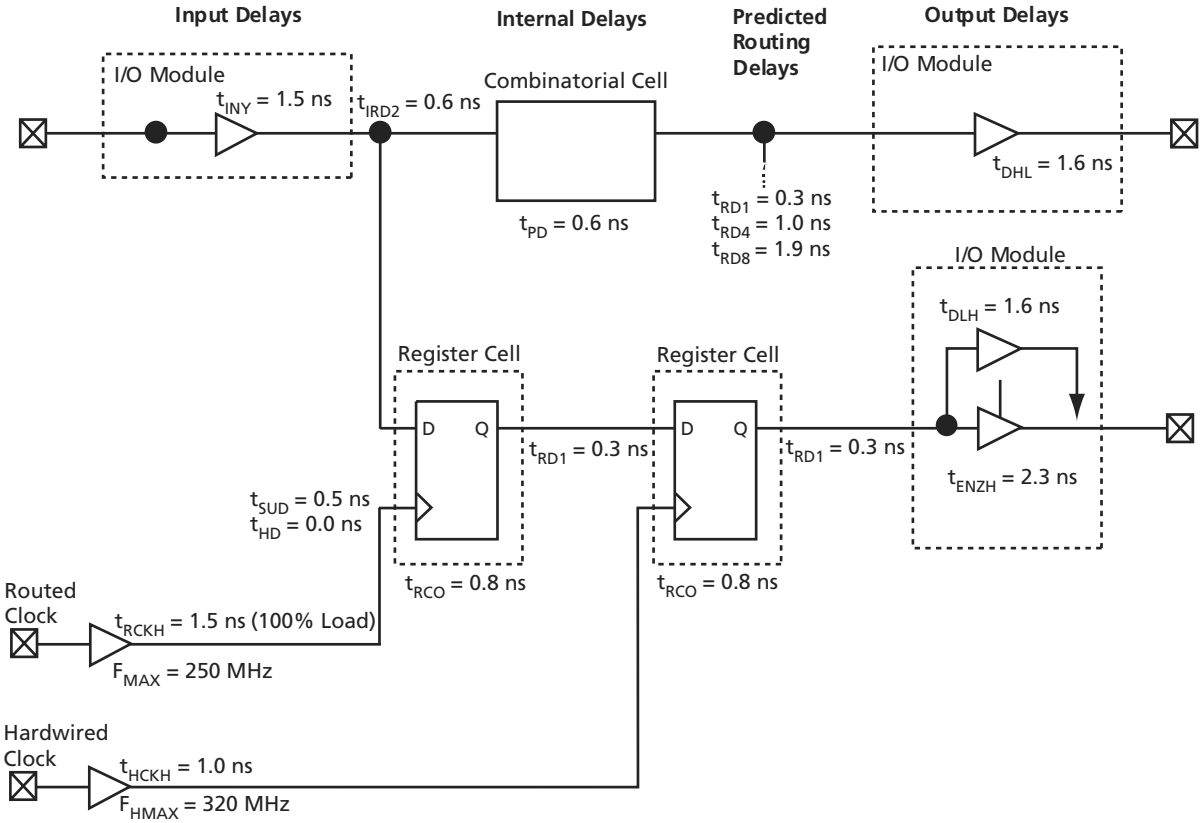
P_{Total} = 1.461 + 0.001815

P_{Total} = 1.4628 W

Step 5: Compare Estimated Power Consumption against Characterized Power Consumption

The estimated total power consumption for this design is 1.46 W. The characterized power consumption for this design at 200 MHz is 1.0164 W.

SX Timing Model



Note: *Values shown for A54SX08-3, worst-case commercial conditions.*

Figure 1-12 • **SX Timing Model**

Hardwired Clock

External Setup = $t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH}$
= 1.5 + 0.3 + 0.5 – 1.0 = 1.3 ns

EQ 1-15

Clock-to-Out (Pin-to-Pin)

= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.0 + 0.8 + 0.3 + 1.6 = 3.7 ns

EQ 1-16

Routed Clock

External Setup = $t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH}$
= 1.5 + 0.3 + 0.5 – 1.5 = 0.8 ns

EQ 1-17

Clock-to-Out (Pin-to-Pin)

= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.52+ 0.8 + 0.3 + 1.6 = 4.2 ns

EQ 1-18

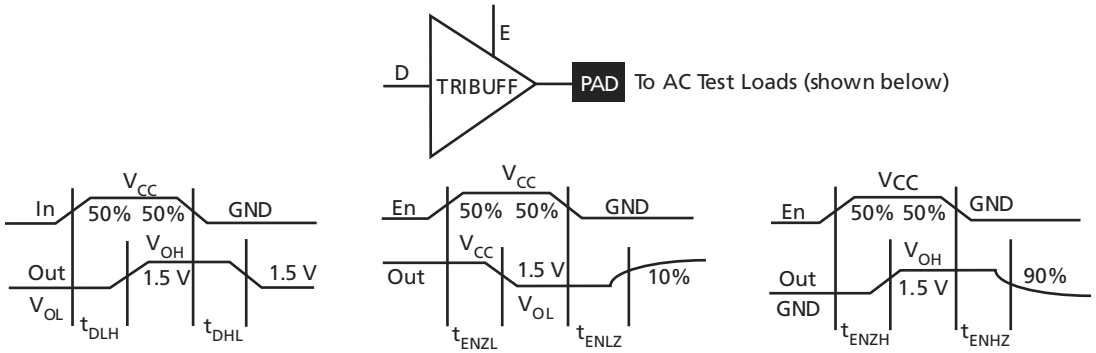


Figure 1-13 • **Output Buffer Delays**

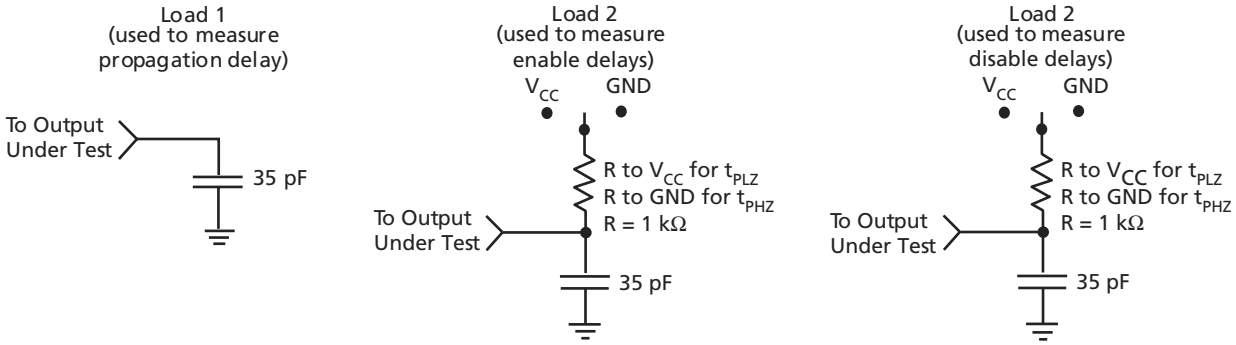


Figure 1-14 • **AC Test Loads**

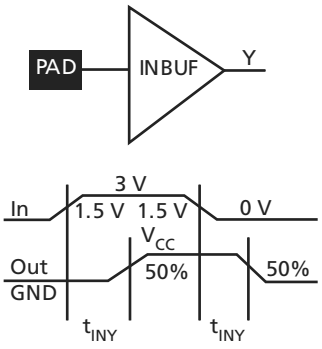


Figure 1-15 • **Input Buffer Delays**

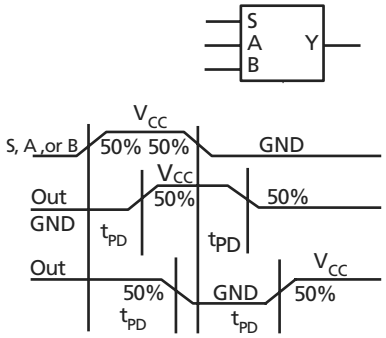


Figure 1-16 • **C-Cell Delays**

Register Cell Timing Characteristics

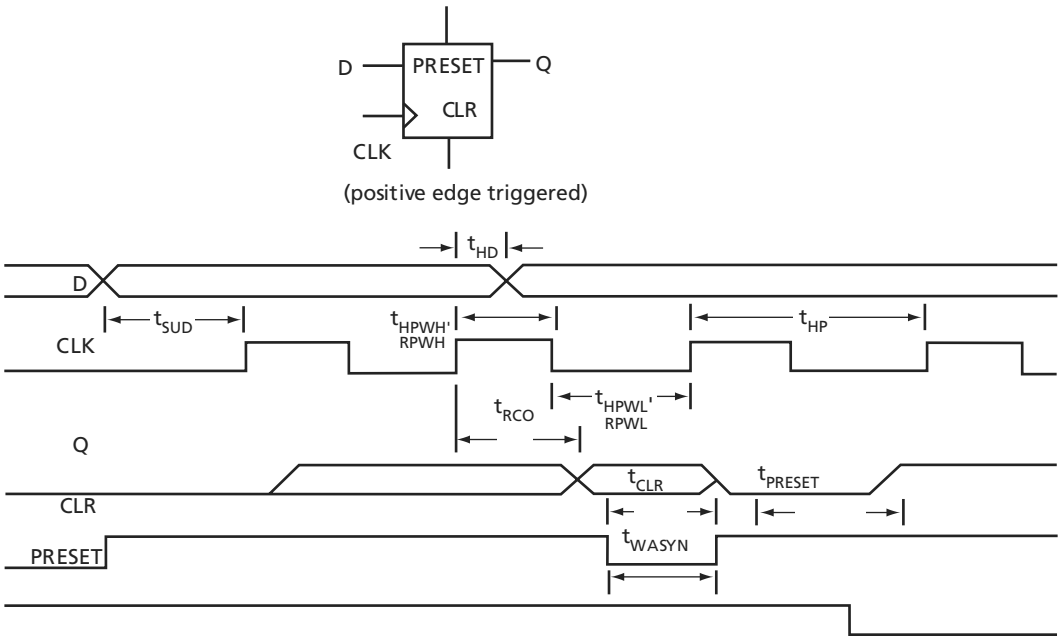


Figure 1-17 • **Flip-Flops**

Timing Characteristics

Timing characteristics for SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO = 24) routing delays in the datasheet specifications section.

Timing Derating

SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

A54SX08 Timing Characteristics

Table 1-17 • **A54SX08 Timing Characteristics (Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Input Module Predicted Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics (Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH}, the loading is 5 pF.*

Package Pin Assignments

84-Pin PLCC

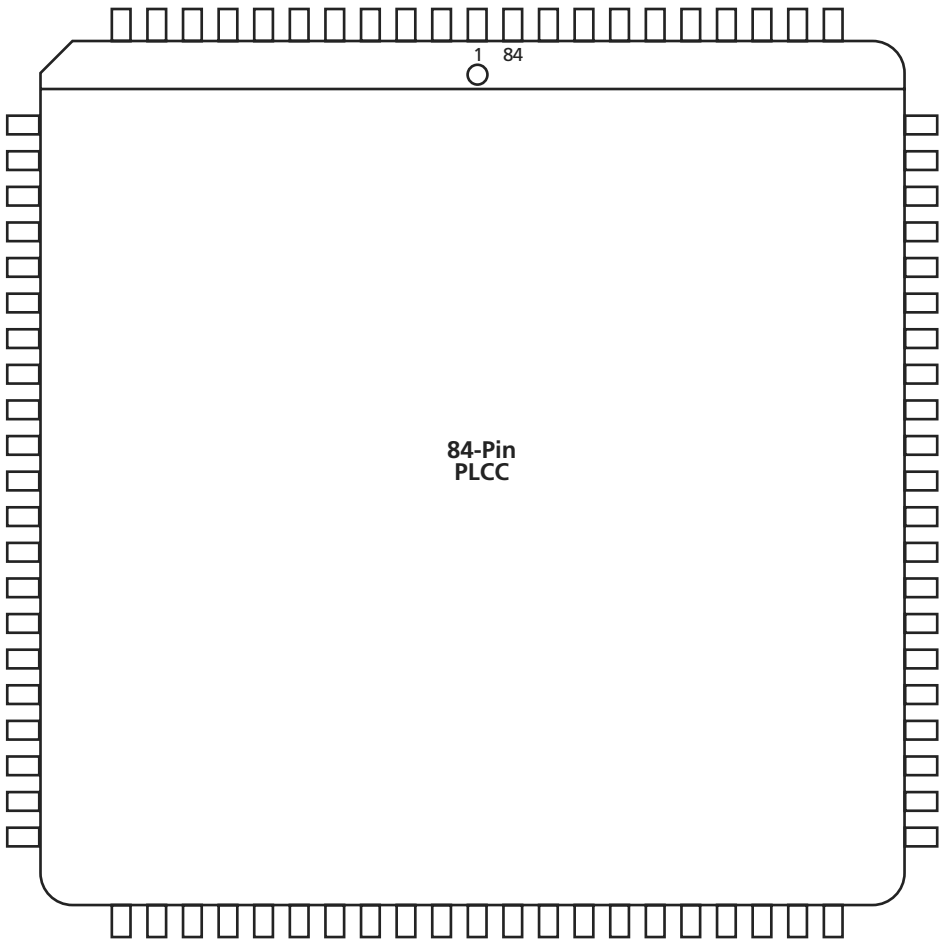


Figure 2-1 • **84-Pin PLCC (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

84-Pin PLCC	
Pin Number	**A54SX08 Function**
1	V_{CCR}
2	GND
3	V_{CCA}
4	PRA, I/O
5	I/O
6	I/O
7	V_{CCI}
8	I/O
9	I/O
10	I/O
11	TCK, I/O
12	TDI, I/O
13	I/O
14	I/O
15	I/O
16	TMS
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V_{CCI}
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O

84-Pin PLCC	
Pin Number	**A54SX08 Function**
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V_{CCA}
42	GND
43	V_{CCR}
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V_{CCA}
60	V_{CCI}
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V_{CCA}
69	GND
70	I/O

84-Pin PLCC	
Pin Number	**A54SX08 Function**
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	CLKA
84	CLKB

208-Pin PQFP

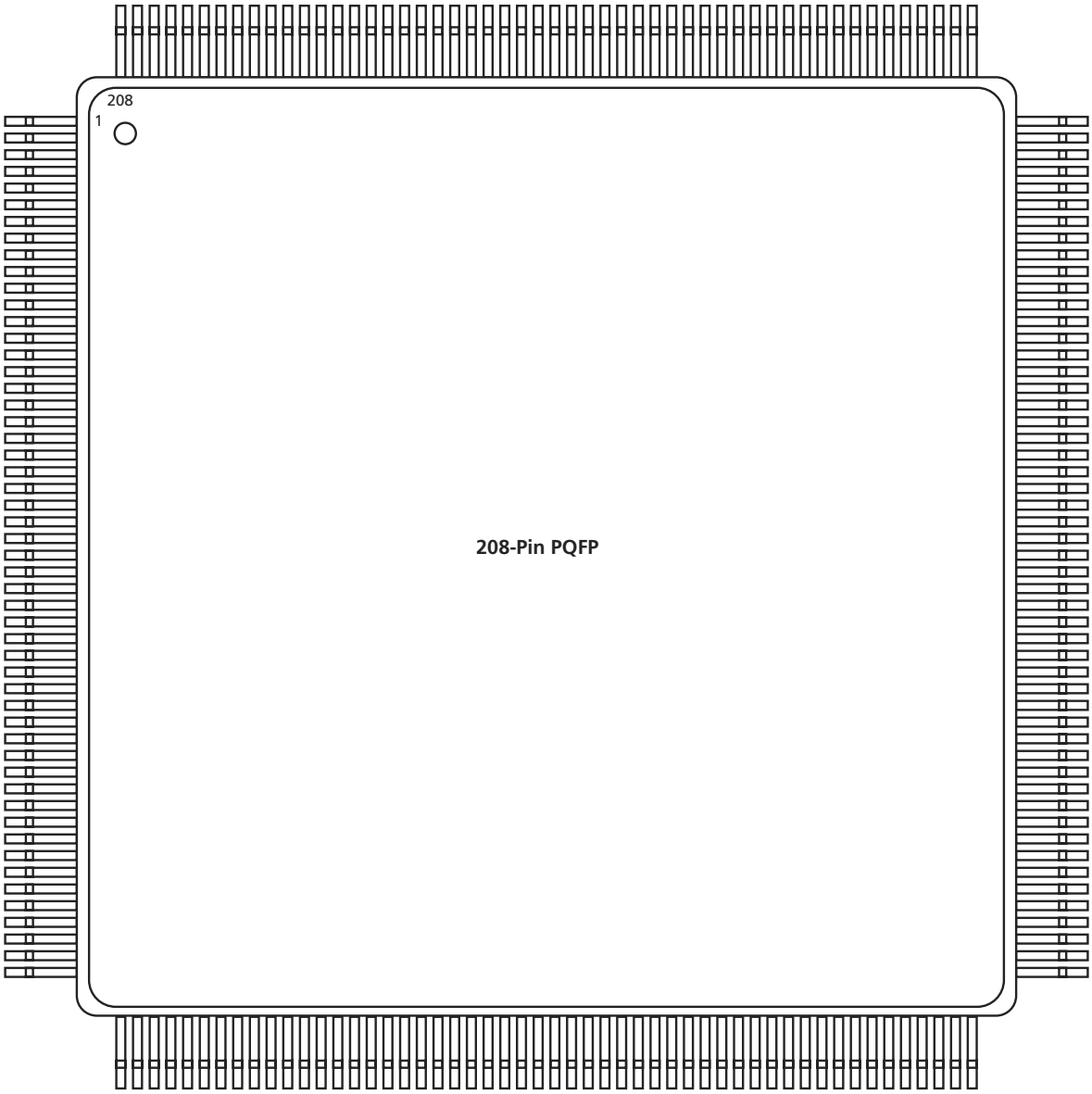


Figure 2-2 • **208-Pin PQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
145	V_{CCA}	V_{CCA}	V_{CCA}
146	GND	GND	GND
147	I/O	I/O	I/O
148	V_{CCI}	V_{CCI}	V_{CCI}
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	NC	I/O	I/O
156	NC	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	V_{CCI}	V_{CCI}	V_{CCI}
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	NC	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	NC	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	NC	I/O	I/O
177	I/O	I/O	I/O
178	I/O	I/O	I/O
179	I/O	I/O	I/O
180	CLKA	CLKA	CLKA

208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
181	CLKB	CLKB	CLKB
182	V_{CCR}	V_{CCR}	V_{CCR}
183	GND	GND	GND
184	V_{CCA}	V_{CCA}	V_{CCA}
185	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	NC	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	NC	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	NC	I/O	I/O
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	NC	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	V_{CCI}	V_{CCI}	V_{CCI}
202	NC	I/O	I/O
203	NC	I/O	I/O
204	I/O	I/O	I/O
205	NC	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O

Note: ** Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

100-Pin VQFP		
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	TMS	TMS
8	V_{CCI}	V_{CCI}
9	GND	GND
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	V_{CCI}	V_{CCI}
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	PRB, I/O	PRB, I/O

100-Pin VQFP		
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
35	V_{CCA}	V_{CCA}
36	GND	GND
37	V_{CCR}	V_{CCR}
38	I/O	I/O
39	HCLK	HCLK
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	V_{CCI}	V_{CCI}
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	TDO, I/O	TDO, I/O
50	I/O	I/O
51	GND	GND
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	V_{CCA}	V_{CCA}
68	GND	GND

100-Pin VQFP		
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
69	GND	GND
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	V_{CCI}	V_{CCI}
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	CLKA	CLKA
88	CLKB	CLKB
89	V_{CCR}	V_{CCR}
90	V_{CCA}	V_{CCA}
91	GND	GND
92	PRA, I/O	PRA, I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	TCK, I/O	TCK, I/O

329-Pin PBGA

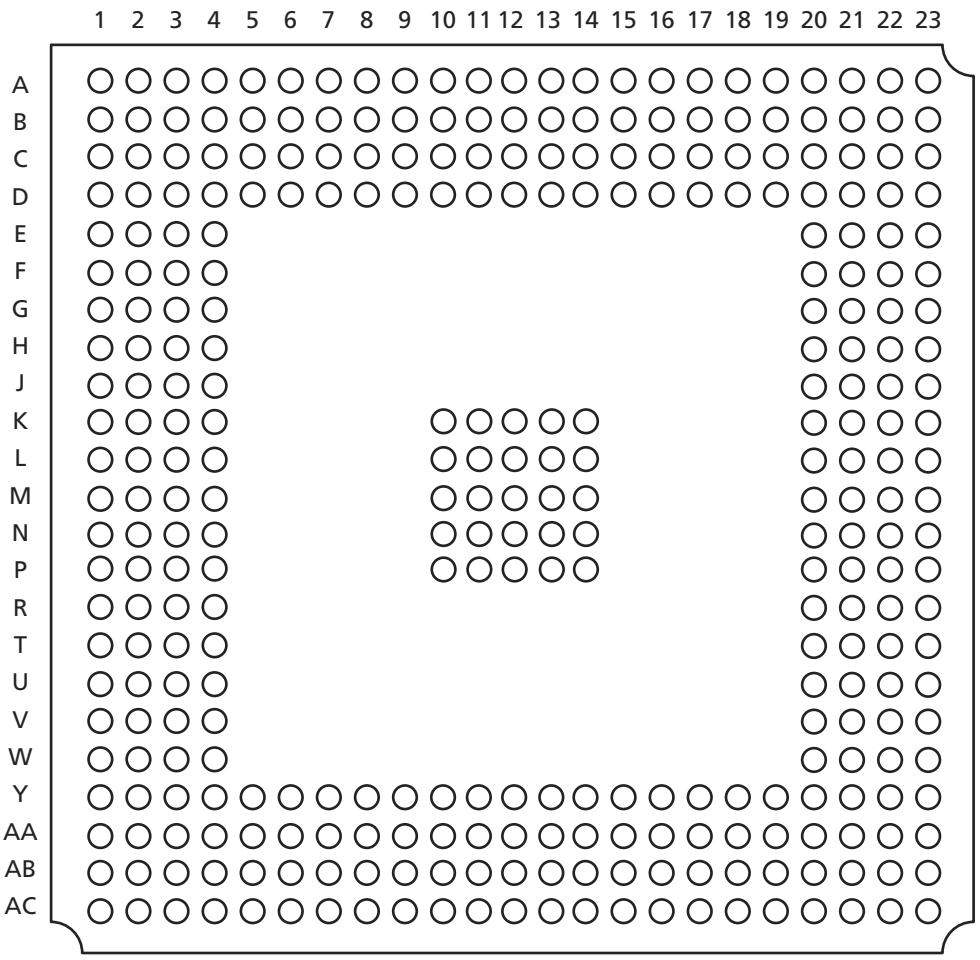


Figure 2-7 • **329-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

329-Pin PBGA	
Pin Number	**A54SX32 Function**
A1	GND
A2	GND
A3	V_{CCI}
A4	NC
A5	I/O
A6	I/O
A7	V_{CCI}
A8	NC
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	CLKB
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
A20	I/O
A21	NC
A22	V_{CCI}
A23	GND
AA1	V_{CCI}
AA2	I/O
AA3	GND
AA4	I/O
AA5	I/O
AA6	I/O
AA7	I/O
AA8	I/O
AA9	I/O
AA10	I/O
AA11	I/O
AA12	I/O

329-Pin PBGA	
Pin Number	**A54SX32 Function**
AA13	I/O
AA14	I/O
AA15	I/O
AA16	I/O
AA17	I/O
AA18	I/O
AA19	I/O
AA20	TDO, I/O
AA21	V_{CCI}
AA22	I/O
AA23	V_{CCI}
AB1	I/O
AB2	GND
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AB10	I/O
AB11	PRB, I/O
AB12	I/O
AB13	HCLK
AB14	I/O
AB15	I/O
AB16	I/O
AB17	I/O
AB18	I/O
AB19	I/O
AB20	I/O
AB21	I/O
AB22	GND
AB23	I/O
AC1	GND

329-Pin PBGA	
Pin Number	**A54SX32 Function**
AC2	V_{CCI}
AC3	NC
AC4	I/O
AC5	I/O
AC6	I/O
AC7	I/O
AC8	I/O
AC9	V_{CCI}
AC10	I/O
AC11	I/O
AC12	I/O
AC13	I/O
AC14	I/O
AC15	NC
AC16	I/O
AC17	I/O
AC18	I/O
AC19	I/O
AC20	I/O
AC21	NC
AC22	V_{CCI}
AC23	GND
B1	V_{CCI}
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	PRA, I/O
B13	CLKA

329-Pin PBGA	
Pin Number	**A54SX32 Function**
B14	I/O
B15	I/O
B16	I/O
B17	I/O
B18	I/O
B19	I/O
B20	I/O
B21	I/O
B22	GND
B23	V_{CCI}
C1	NC
C2	TDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O
C21	V_{CCI}
C22	GND
C23	NC
D1	I/O
D2	I/O

144-Pin FBGA

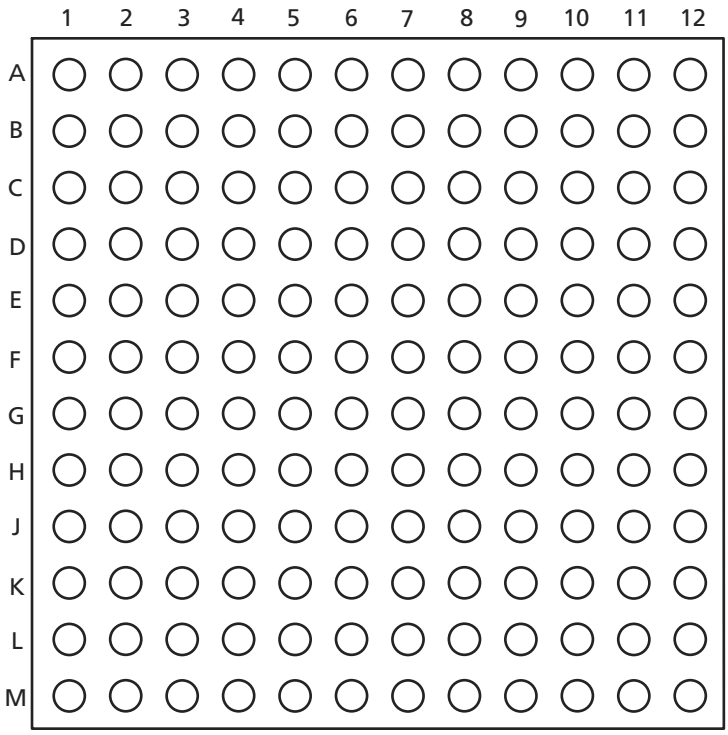


Figure 2-8 • **144-Pin FBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.