Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.
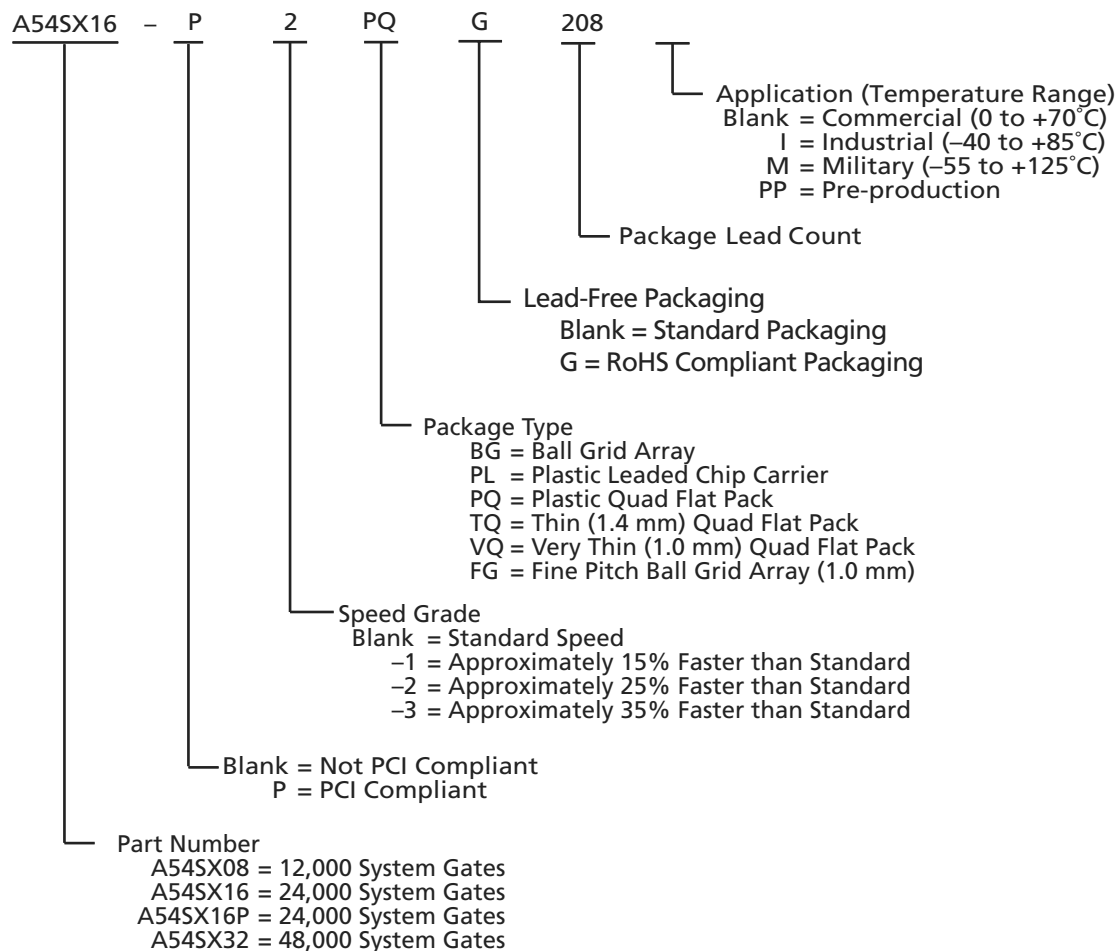
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	12000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx08-vqg100

Ordering Information

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A54SX16  –  P   2   PQ   G   208
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Application (Temperature Range)
Blank = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
PP = Pre-production

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
BG = Ball Grid Array
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flat Pack
TQ = Thin (1.4 mm) Quad Flat Pack
VQ = Very Thin (1.0 mm) Quad Flat Pack
FG = Fine Pitch Ball Grid Array (1.0 mm)

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% Faster than Standard
–2 = Approximately 25% Faster than Standard
–3 = Approximately 35% Faster than Standard

Blank = Not PCI Compliant
P = PCI Compliant

Part Number
A54SX08 = 12,000 System Gates
A54SX16 = 24,000 System Gates
A54SX16P = 24,000 System Gates
A54SX32 = 48,000 System Gates

Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PLCC 84-Pin	VQFP 100-Pin	PQFP 208-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 313-Pin	PBGA 329-Pin	FBGA 144-Pin
A54SX08	69	81	130	113	128	–	–	111
A54SX16	–	81	175	–	147	–	–	–
A54SX16P	–	81	175	113	147	–	–	–
A54SX32	–	–	174	113	147	249	249	–

Note: *Package Definitions (Consult your local Actel sales representative for product availability):*
PLCC = Plastic Leaded Chip Carrier
PQFP = Plastic Quad Flat Pack
TQFP = Thin Quad Flat Pack
VQFP = Very Thin Quad Flat Pack
PBGA = Plastic Ball Grid Array
FBGA = Fine Pitch (1.0 mm) Ball Grid Array

SX Family FPGAs

General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX's flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

Logic Module Design

The SX family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.
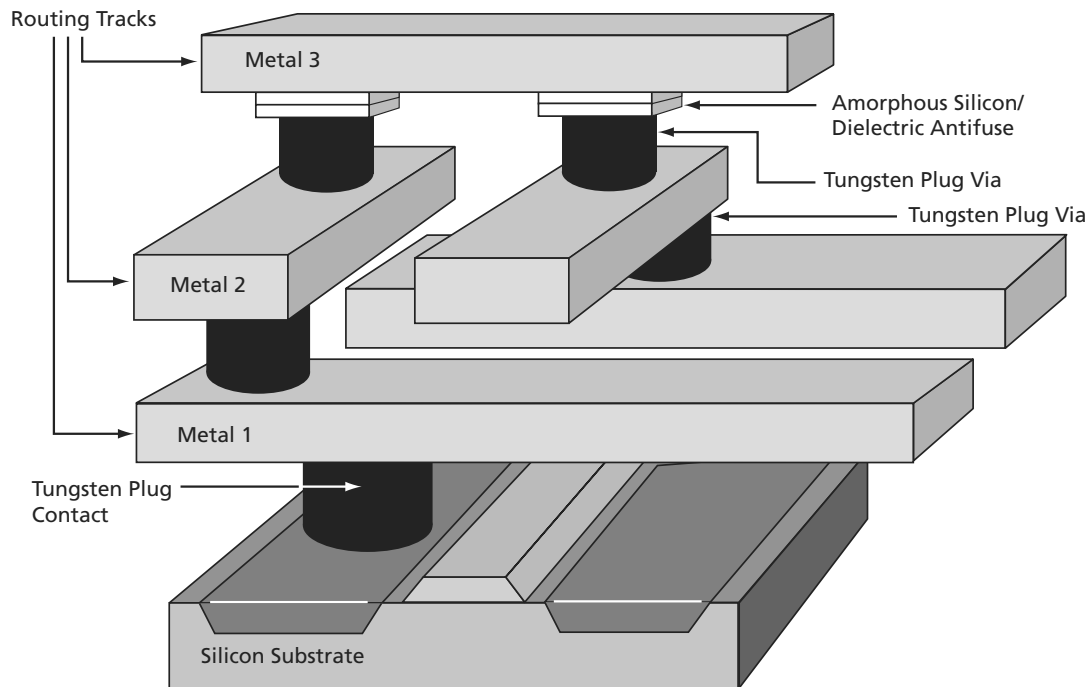

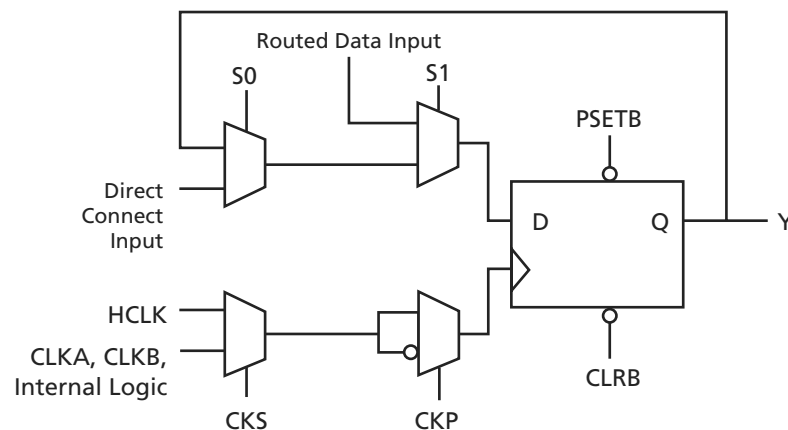*Figure 1-1* • **SX Family Interconnect Elements**

Figure 1-2 • **R-Cell**

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.
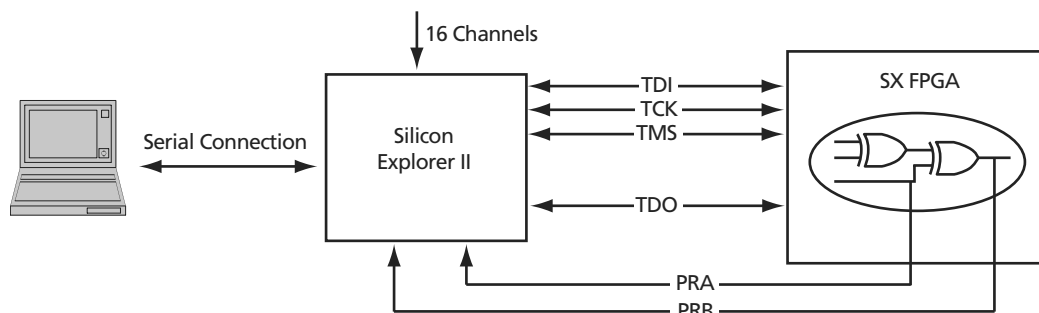
Figure 1-8 • **Probe Setup**

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II are compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an SX device using Silicon Sculptor II are as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming SX devices, refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

3.3 V / 5 V Operating Conditions

Table 1-3 • **Absolute Maximum Ratings[1]**

Symbol	Parameter	Limits	Units
V_{CCR}[2]	DC Supply Voltage[3]	–0.3 to + 6.0	V
V_{CCA}[2]	DC Supply Voltage	–0.3 to + 4.0	V
V_{CCI}[2]	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	–0.3 to + 4.0	V
V_{CCI}[2]	DC Supply Voltage (A54SX16P)	–0.3 to + 6.0	V
V_I	Input Voltage	–0.5 to + 5.5	V
V_O	Output Voltage	–0.5 to + 3.6	V
I_{IO}	I/O Source Sink Current[3]	–30 to + 5.0	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*

2. V_{CCR} *in the A54SX16P must be greater than or equal to* V_{CCI} *during power-up and power-down sequences and during normal operation.*

3. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than* V_{CC} *+ 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward-bias and can draw excessive current.*

A54SX16P DC Specifications (3.3 V PCI Operation)

Table 1-8 •   **A54SX16P DC Specifications (3.3 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		3.0	3.6	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		−0.5	$0.3V_{CC}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CC}$		±10	µA
V_{OH}	Output High Voltage	$I_{OUT} = -500$ µA	$0.9V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OUT} = 1500$ µA		$0.1V_{CC}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance[4]			8	pF

Notes:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.*

2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*

3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

4. *Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].*

Figure 1-10 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.
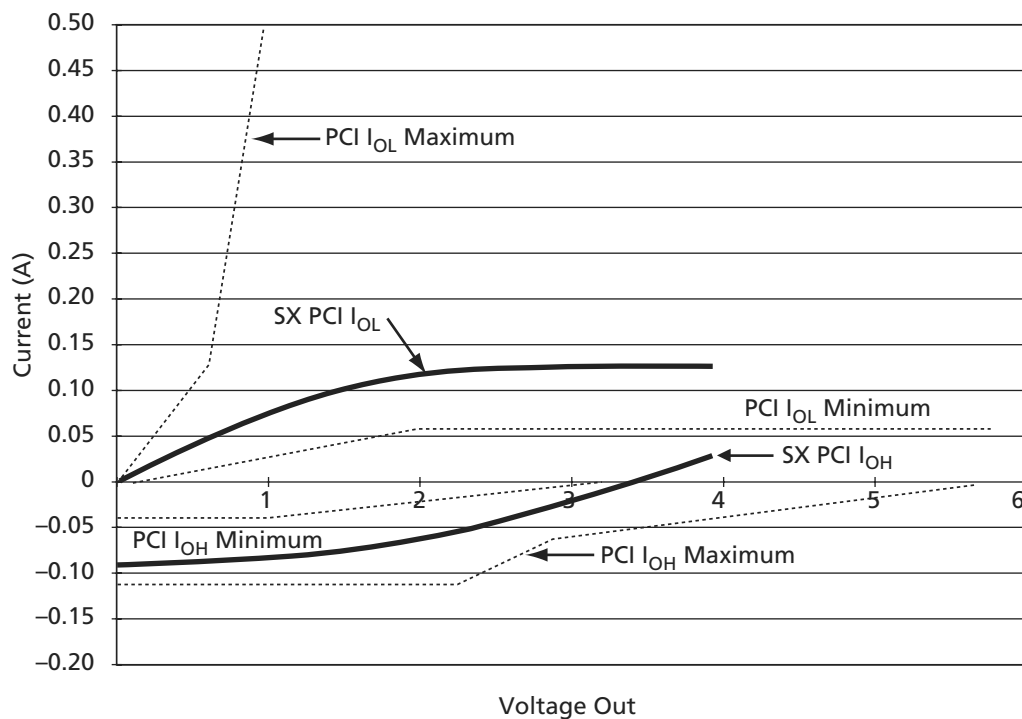

Figure 1-10 • **3.3 V PCI Curve for A54SX16P Device**

$I_{OH} = (98.0/V_{CC}) \times (V_{OUT} - V_{CC}) \times (V_{OUT} + 0.4V_{CC})$

for $V_{CC} > V_{OUT} > 0.7\ V_{CC}$

EQ 1-3

$I_{OL} = (256/V_{CC}) \times V_{OUT} \times (V_{CC} - V_{OUT})$

for $0\ V < V_{OUT} < 0.18\ V_{CC}$

EQ 1-4

Table 1-15 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min.	Units
Plastic Leaded Chip Carrier (PLCC)	84	12	32	22	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Very Thin Quad Flatpack (VQFP)	100	10	38	32	°C/W
Plastic Quad Flat Pack (PQFP) without Heat Spreader	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	14.5	°C/W
Plastic Ball Grid Array (PBGA)	313	3	23	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W

Note: *SX08 does not have a heat spreader.*

Table 1-16 • **Temperature and Voltage Derating Factors***

V_{CCA}	Junction Temperature						
	–55	**–40**	**0**	**25**	**70**	**85**	**125**
3.0	0.75	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.70	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.66	0.69	0.77	0.78	0.87	0.92	1.02

Note: **Normalized to worst-case commercial, T_J = 70°C, V_{CCA} = 3.0 V*

SX Timing Model
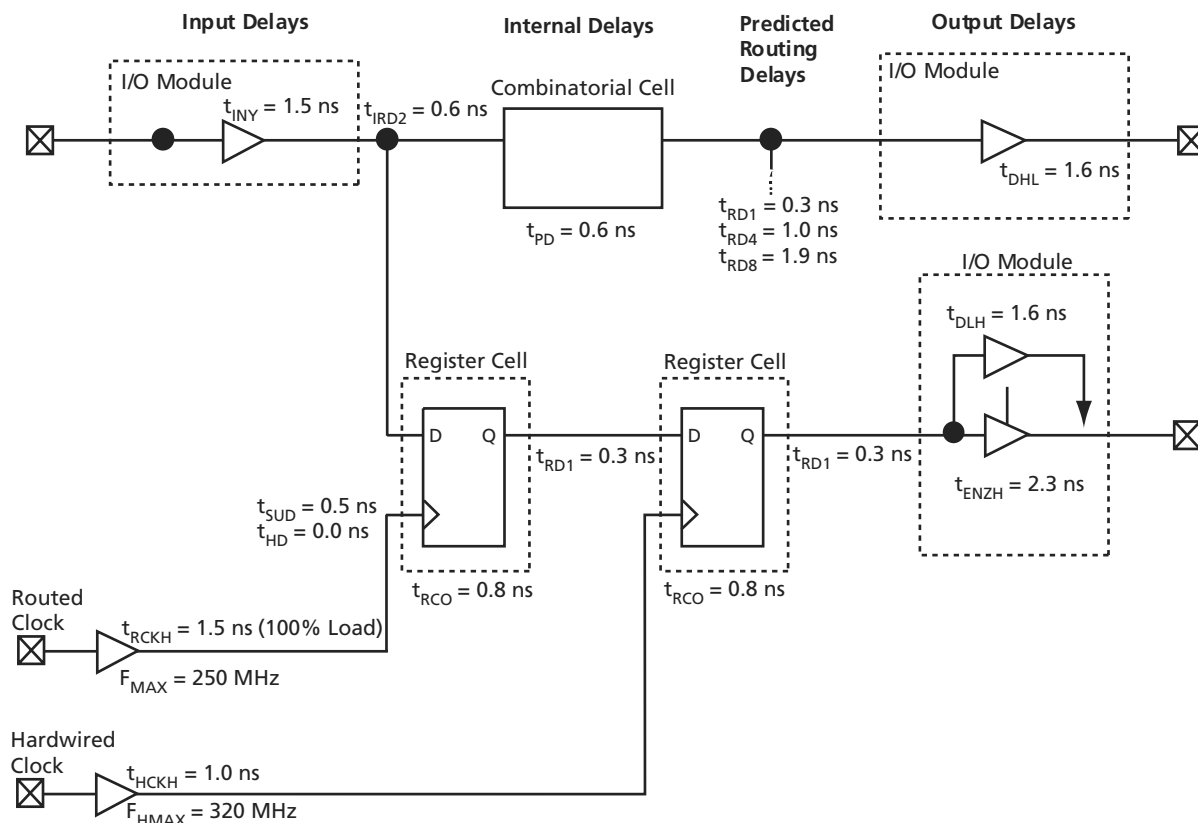
Note: *Values shown for A54SX08-3, worst-case commercial conditions.*

Figure 1-12 • **SX Timing Model**

Hardwired Clock

External Setup = $t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH}$

= $1.5 + 0.3 + 0.5 - 1.0 = 1.3$ ns

EQ 1-15

Clock-to-Out (Pin-to-Pin)

= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= $1.0 + 0.8 + 0.3 + 1.6 = 3.7$ ns

EQ 1-16

Routed Clock

External Setup = $t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH}$

= $1.5 + 0.3 + 0.5 - 1.5 = 0.8$ ns

EQ 1-17

Clock-to-Out (Pin-to-Pin)

= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= $1.52 + 0.8 + 0.3 + 1.6 = 4.2$ ns

EQ 1-18

Register Cell Timing Characteristics

Figure 1-17 • **Flip-Flops**

Timing Characteristics

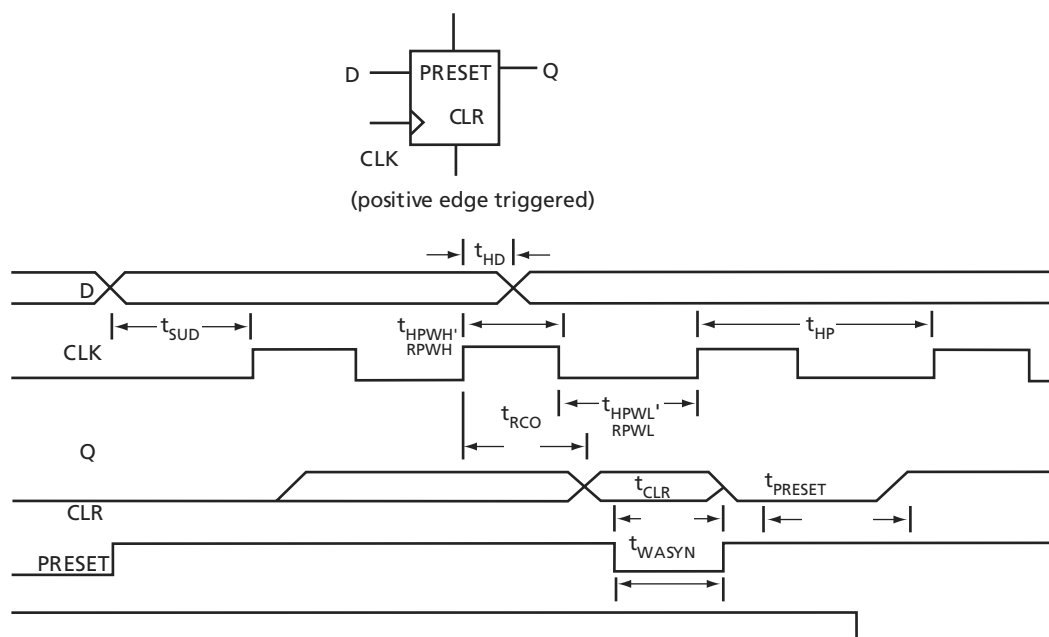Timing characteristics for SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO = 24) routing delays in the datasheet specifications section.

Timing Derating

SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

A54SX08 Timing Characteristics

Table 1-17 • **A54SX08 Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	'–3' Speed Min.	'–3' Speed Max.	'–2' Speed Min.	'–2' Speed Max.	'–1' Speed Min.	'–1' Speed Max.	'Std' Speed Min.	'Std' Speed Max.	Units
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Input Module Predicted Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

Table 1-18 • **A54SX16 Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V$_{CCR}$ = 4.75 V, V$_{CCA}$, V$_{CCI}$ = 3.0 V, T$_J$ = 70°C)

Parameter	Description	'–3' Speed Min.	'–3' Speed Max.	'–2' Speed Min.	'–2' Speed Max.	'–1' Speed Min.	'–1' Speed Max.	'Std' Speed Min.	'Std' Speed Max.	Units
Dedicated (Hardwired) Array Clock Network										
t$_{HCKH}$	Input LOW to HIGH (pad to R-Cell input)		1.2		1.4		1.5		1.8	ns
t$_{HCKL}$	Input HIGH to LOW (pad to R-Cell input)		1.2		1.4		1.6		1.9	ns
t$_{HPWH}$	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t$_{HPWL}$	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t$_{HCKSW}$	Maximum Skew		0.2		0.2		0.3		0.3	ns
t$_{HP}$	Minimum Period	2.7		3.1		3.6		4.2		ns
f$_{HMAX}$	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t$_{RCKH}$	Input LOW to HIGH (light load) (pad to R-Cell input)		1.6		1.8		2.1		2.5	ns
t$_{RCKL}$	Input HIGH to LOW (light load) (pad to R-Cell input)		1.8		2.0		2.3		2.7	ns
t$_{RCKH}$	Input LOW to HIGH (50% load) (pad to R-Cell input)		1.8		2.1		2.5		2.8	ns
t$_{RCKL}$	Input HIGH to LOW (50% load) (pad to R-Cell input)		2.0		2.2		2.5		3.0	ns
t$_{RCKH}$	Input LOW to HIGH (100% load) (pad to R-Cell input)		1.8		2.1		2.4		2.8	ns
t$_{RCKL}$	Input HIGH to LOW (100% load) (pad to R-Cell input)		2.0		2.2		2.5		3.0	ns
t$_{RPWH}$	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t$_{RPWL}$	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t$_{RCKSW}$	Maximum Skew (light load)		0.5		0.5		0.5		0.7	ns
t$_{RCKSW}$	Maximum Skew (50% load)		0.5		0.6		0.7		0.8	ns
t$_{RCKSW}$	Maximum Skew (100% load)		0.5		0.6		0.7		0.8	ns
TTL Output Module Timing[3]										
t$_{DLH}$	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t$_{DHL}$	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t$_{ENZL}$	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t$_{ENZH}$	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t$_{ENLZ}$	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t$_{ENHZ}$	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Notes:

1. For dual-module macros, use t$_{PD}$ + t$_{RD1}$ + t$_{PDn}$, t$_{RCO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance.   Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

3. Delays based on 35 pF loading, except t$_{ENZL}$ and t$_{ENZH}$. For t$_{ENZL}$ and t$_{ENZH}$, the loading is 5 pF.

Pin Description

CLKA/B   **Clock A and B**

These pins are 3.3 V / 5.0 V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as bidirectional.)

GND   **Ground**

LOW supply voltage.

HCLK   **Dedicated (hardwired) Array Clock**

This pin is the 3.3 V / 5.0 V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O   **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3 V PCI or 5.0 V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC   **No Connection**

This pin is not connected to circuitry within the device.

PRA, I/O   **Probe A**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

PRB, I/O   **Probe B**

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK   **Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI   **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO   **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TMS   **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-2 on page 1-6). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

V$_{CCI}$ **Supply Voltage**

Supply voltage for I/Os. See Table 1-1 on page 1-5.

V$_{CCA}$ **Supply Voltage**

Supply voltage for Array. See Table 1-1 on page 1-5.

V$_{CCR}$ **Supply Voltage**

Supply voltage for input tolerance (required for internal biasing). See Table 1-1 on page 1-5.

84-Pin PLCC	
Pin Number	**A54SX08 Function**
1	V_{CCR}
2	GND
3	V_{CCA}
4	PRA, I/O
5	I/O
6	I/O
7	V_{CCI}
8	I/O
9	I/O
10	I/O
11	TCK, I/O
12	TDI, I/O
13	I/O
14	I/O
15	I/O
16	TMS
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V_{CCI}
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O

84-Pin PLCC	
Pin Number	**A54SX08 Function**
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V_{CCA}
42	GND
43	V_{CCR}
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V_{CCA}
60	V_{CCI}
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V_{CCA}
69	GND
70	I/O

84-Pin PLCC	
Pin Number	**A54SX08 Function**
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	CLKA
84	CLKB

208-Pin PQFP				208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**	**Pin Number**	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
1	GND	GND	GND	37	I/O	I/O	I/O
2	TDI, I/O	TDI, I/O	TDI, I/O	38	I/O	I/O	I/O
3	I/O	I/O	I/O	39	NC	I/O	I/O
4	NC	I/O	I/O	40	V_{CCI}	V_{CCI}	V_{CCI}
5	I/O	I/O	I/O	41	V_{CCA}	V_{CCA}	V_{CCA}
6	NC	I/O	I/O	42	I/O	I/O	I/O
7	I/O	I/O	I/O	43	I/O	I/O	I/O
8	I/O	I/O	I/O	44	I/O	I/O	I/O
9	I/O	I/O	I/O	45	I/O	I/O	I/O
10	I/O	I/O	I/O	46	I/O	I/O	I/O
11	TMS	TMS	TMS	47	I/O	I/O	I/O
12	V_{CCI}	V_{CCI}	V_{CCI}	48	NC	I/O	I/O
13	I/O	I/O	I/O	49	I/O	I/O	I/O
14	NC	I/O	I/O	50	NC	I/O	I/O
15	I/O	I/O	I/O	51	I/O	I/O	I/O
16	I/O	I/O	I/O	52	GND	GND	GND
17	NC	I/O	I/O	53	I/O	I/O	I/O
18	I/O	I/O	I/O	54	I/O	I/O	I/O
19	I/O	I/O	I/O	55	I/O	I/O	I/O
20	NC	I/O	I/O	56	I/O	I/O	I/O
21	I/O	I/O	I/O	57	I/O	I/O	I/O
22	I/O	I/O	I/O	58	I/O	I/O	I/O
23	NC	I/O	I/O	59	I/O	I/O	I/O
24	I/O	I/O	I/O	60	V_{CCI}	V_{CCI}	V_{CCI}
25	V_{CCR}	V_{CCR}	V_{CCR}	61	NC	I/O	I/O
26	GND	GND	GND	62	I/O	I/O	I/O
27	V_{CCA}	V_{CCA}	V_{CCA}	63	I/O	I/O	I/O
28	GND	GND	GND	64	NC	I/O	I/O
29	I/O	I/O	I/O	65*	I/O	I/O	NC*
30	I/O	I/O	I/O	66	I/O	I/O	I/O
31	NC	I/O	I/O	67	NC	I/O	I/O
32	I/O	I/O	I/O	68	I/O	I/O	I/O
33	I/O	I/O	I/O	69	I/O	I/O	I/O
34	I/O	I/O	I/O	70	NC	I/O	I/O
35	NC	I/O	I/O	71	I/O	I/O	I/O
36	I/O	I/O	I/O	72	I/O	I/O	I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

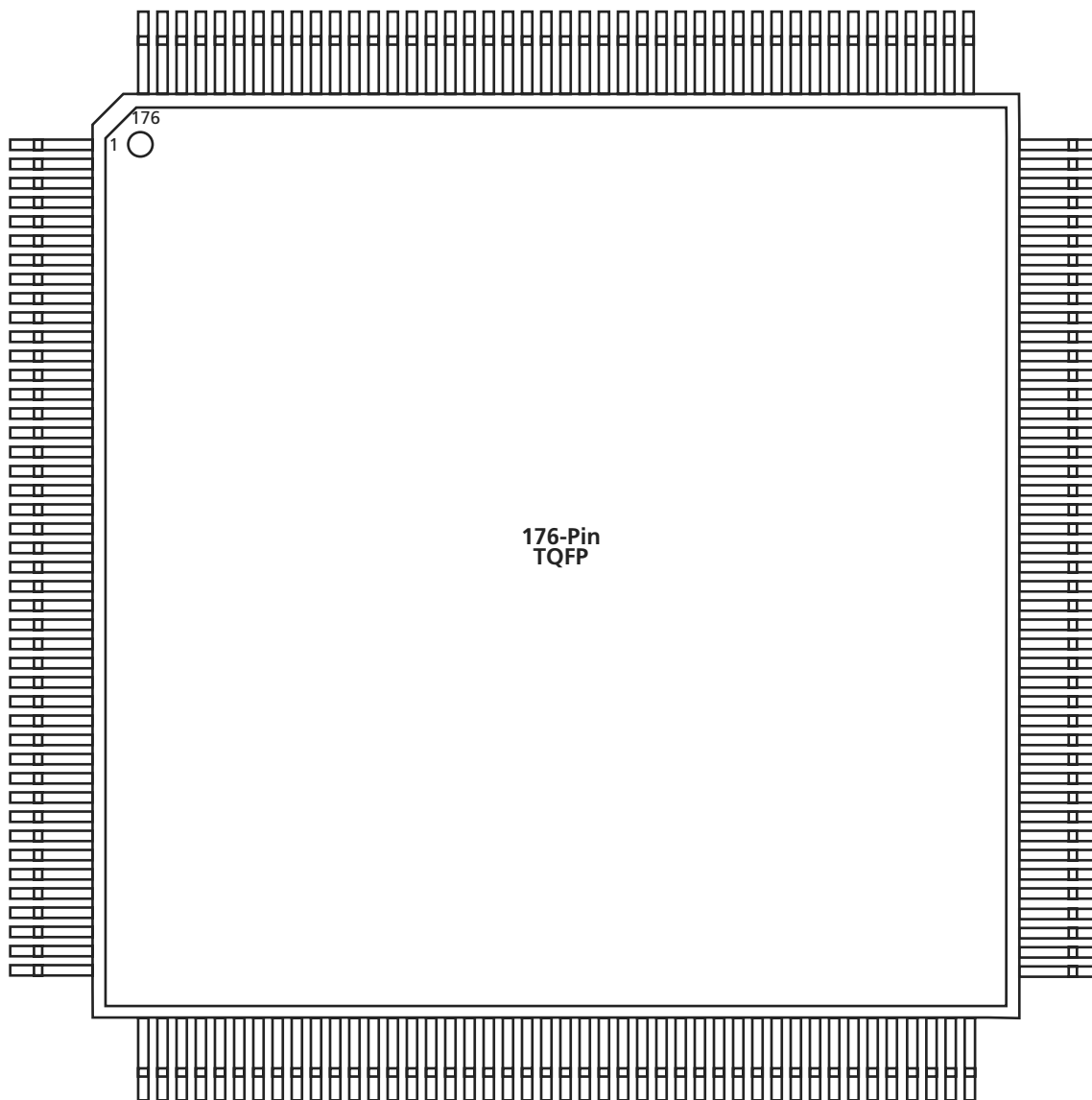| 144-Pin TQFP				144-Pin TQFP			
Pin Number	**A54SX08 Function**	**A54SX16P Function**	**A54SX32 Function**	**Pin Number**	**A54SX08 Function**	**A54SX16P Function**	**A54SX32 Function**
1	GND	GND	GND	37	I/O	I/O	I/O
2	TDI, I/O	TDI, I/O	TDI, I/O	38	I/O	I/O	I/O
3	I/O	I/O	I/O	39	I/O	I/O	I/O
4	I/O	I/O	I/O	40	I/O	I/O	I/O
5	I/O	I/O	I/O	41	I/O	I/O	I/O
6	I/O	I/O	I/O	42	I/O	I/O	I/O
7	I/O	I/O	I/O	43	I/O	I/O	I/O
8	I/O	I/O	I/O	44	V_{CCI}	V_{CCI}	V_{CCI}
9	TMS	TMS	TMS	45	I/O	I/O	I/O
10	V_{CCI}	V_{CCI}	V_{CCI}	46	I/O	I/O	I/O
11	GND	GND	GND	47	I/O	I/O	I/O
12	I/O	I/O	I/O	48	I/O	I/O	I/O
13	I/O	I/O	I/O	49	I/O	I/O	I/O
14	I/O	I/O	I/O	50	I/O	I/O	I/O
15	I/O	I/O	I/O	51	I/O	I/O	I/O
16	I/O	I/O	I/O	52	I/O	I/O	I/O
17	I/O	I/O	I/O	53	I/O	I/O	I/O
18	I/O	I/O	I/O	54	PRB, I/O	PRB, I/O	PRB, I/O
19	V_{CCR}	V_{CCR}	V_{CCR}	55	I/O	I/O	I/O
20	V_{CCA}	V_{CCA}	V_{CCA}	56	V_{CCA}	V_{CCA}	V_{CCA}
21	I/O	I/O	I/O	57	GND	GND	GND
22	I/O	I/O	I/O	58	V_{CCR}	V_{CCR}	V_{CCR}
23	I/O	I/O	I/O	59	I/O	I/O	I/O
24	I/O	I/O	I/O	60	HCLK	HCLK	HCLK
25	I/O	I/O	I/O	61	I/O	I/O	I/O
26	I/O	I/O	I/O	62	I/O	I/O	I/O
27	I/O	I/O	I/O	63	I/O	I/O	I/O
28	GND	GND	GND	64	I/O	I/O	I/O
29	V_{CCI}	V_{CCI}	V_{CCI}	65	I/O	I/O	I/O
30	V_{CCA}	V_{CCA}	V_{CCA}	66	I/O	I/O	I/O
31	I/O	I/O	I/O	67	I/O	I/O	I/O
32	I/O	I/O	I/O	68	V_{CCI}	V_{CCI}	V_{CCI}
33	I/O	I/O	I/O	69	I/O	I/O	I/O
34	I/O	I/O	I/O	70	I/O	I/O	I/O
35	I/O	I/O	I/O	71	TDO, I/O	TDO, I/O	TDO, I/O
36	GND	GND	GND	72	I/O	I/O	I/O

176-Pin TQFP

176-Pin TQFP

Figure 2-4 • **176-Pin TQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

176-Pin TQFP				176-Pin TQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**	**Pin Number**	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
69	HCLK	HCLK	HCLK	103	I/O	I/O	I/O
70	I/O	I/O	I/O	104	I/O	I/O	I/O
71	I/O	I/O	I/O	105	I/O	I/O	I/O
72	I/O	I/O	I/O	106	I/O	I/O	I/O
73	I/O	I/O	I/O	107	I/O	I/O	I/O
74	I/O	I/O	I/O	108	GND	GND	GND
75	I/O	I/O	I/O	109	V_{CCA}	V_{CCA}	V_{CCA}
76	I/O	I/O	I/O	110	GND	GND	GND
77	I/O	I/O	I/O	111	I/O	I/O	I/O
78	I/O	I/O	I/O	112	I/O	I/O	I/O
79	NC	I/O	I/O	113	I/O	I/O	I/O
80	I/O	I/O	I/O	114	I/O	I/O	I/O
81	NC	I/O	I/O	115	I/O	I/O	I/O
82	V_{CCI}	V_{CCI}	V_{CCI}	116	I/O	I/O	I/O
83	I/O	I/O	I/O	117	I/O	I/O	I/O
84	I/O	I/O	I/O	118	NC	I/O	I/O
85	I/O	I/O	I/O	119	I/O	I/O	I/O
86	I/O	I/O	I/O	120	NC	I/O	I/O
87	TDO, I/O	TDO, I/O	TDO, I/O	121	NC	I/O	I/O
88	I/O	I/O	I/O	122	V_{CCA}	V_{CCA}	V_{CCA}
89	GND	GND	GND	123	GND	GND	GND
90	NC	I/O	I/O	124	V_{CCI}	V_{CCI}	V_{CCI}
91	NC	I/O	I/O	125	I/O	I/O	I/O
92	I/O	I/O	I/O	126	I/O	I/O	I/O
93	I/O	I/O	I/O	127	I/O	I/O	I/O
94	I/O	I/O	I/O	128	I/O	I/O	I/O
95	I/O	I/O	I/O	129	I/O	I/O	I/O
96	I/O	I/O	I/O	130	I/O	I/O	I/O
97	I/O	I/O	I/O	131	NC	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}	132	NC	I/O	I/O
99	V_{CCI}	V_{CCI}	V_{CCI}	133	GND	GND	GND
100	I/O	I/O	I/O	134	I/O	I/O	I/O
101	I/O	I/O	I/O	135	I/O	I/O	I/O
102	I/O	I/O	I/O	136	I/O	I/O	I/O

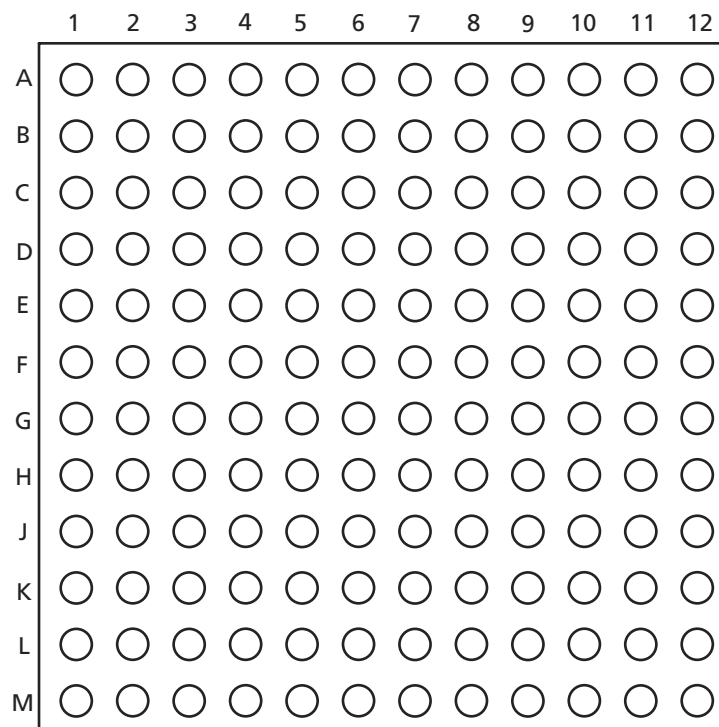| 100-Pin VQFP			100-Pin VQFP			100-Pin VQFP		
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
1	GND	GND	35	V_{CCA}	V_{CCA}	69	GND	GND
2	TDI, I/O	TDI, I/O	36	GND	GND	70	I/O	I/O
3	I/O	I/O	37	V_{CCR}	V_{CCR}	71	I/O	I/O
4	I/O	I/O	38	I/O	I/O	72	I/O	I/O
5	I/O	I/O	39	HCLK	HCLK	73	I/O	I/O
6	I/O	I/O	40	I/O	I/O	74	I/O	I/O
7	TMS	TMS	41	I/O	I/O	75	I/O	I/O
8	V_{CCI}	V_{CCI}	42	I/O	I/O	76	I/O	I/O
9	GND	GND	43	I/O	I/O	77	I/O	I/O
10	I/O	I/O	44	V_{CCI}	V_{CCI}	78	I/O	I/O
11	I/O	I/O	45	I/O	I/O	79	I/O	I/O
12	I/O	I/O	46	I/O	I/O	80	I/O	I/O
13	I/O	I/O	47	I/O	I/O	81	I/O	I/O
14	I/O	I/O	48	I/O	I/O	82	V_{CCI}	V_{CCI}
15	I/O	I/O	49	TDO, I/O	TDO, I/O	83	I/O	I/O
16	I/O	I/O	50	I/O	I/O	84	I/O	I/O
17	I/O	I/O	51	GND	GND	85	I/O	I/O
18	I/O	I/O	52	I/O	I/O	86	I/O	I/O
19	I/O	I/O	53	I/O	I/O	87	CLKA	CLKA
20	V_{CCI}	V_{CCI}	54	I/O	I/O	88	CLKB	CLKB
21	I/O	I/O	55	I/O	I/O	89	V_{CCR}	V_{CCR}
22	I/O	I/O	56	I/O	I/O	90	V_{CCA}	V_{CCA}
23	I/O	I/O	57	V_{CCA}	V_{CCA}	91	GND	GND
24	I/O	I/O	58	V_{CCI}	V_{CCI}	92	PRA, I/O	PRA, I/O
25	I/O	I/O	59	I/O	I/O	93	I/O	I/O
26	I/O	I/O	60	I/O	I/O	94	I/O	I/O
27	I/O	I/O	61	I/O	I/O	95	I/O	I/O
28	I/O	I/O	62	I/O	I/O	96	I/O	I/O
29	I/O	I/O	63	I/O	I/O	97	I/O	I/O
30	I/O	I/O	64	I/O	I/O	98	I/O	I/O
31	I/O	I/O	65	I/O	I/O	99	I/O	I/O
32	I/O	I/O	66	I/O	I/O	100	TCK, I/O	TCK, I/O
33	I/O	I/O	67	V_{CCA}	V_{CCA}			
34	PRB, I/O	PRB, I/O	68	GND	GND			

144-Pin FBGA

Figure 2-8 • **144-Pin FBGA (Top View)**

Note

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