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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	175
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	208-BFCQFP with Tie Bar
Supplier Device Package	208-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx16-1cq208b

Ordering Information

A54SX16 – P 2 PQ G 208

Application (Temperature Range)
- Blank = Commercial (0 to +70°C)
- I = Industrial (–40 to +85°C)
- M = Military (–55 to +125°C)
- PP = Pre-production

Package Lead Count

Lead-Free Packaging
- Blank = Standard Packaging
- G = RoHS Compliant Packaging

Package Type
- BG = Ball Grid Array
- PL = Plastic Leaded Chip Carrier
- PQ = Plastic Quad Flat Pack
- TQ = Thin (1.4 mm) Quad Flat Pack
- VQ = Very Thin (1.0 mm) Quad Flat Pack
- FG = Fine Pitch Ball Grid Array (1.0 mm)

Speed Grade
- Blank = Standard Speed
- –1 = Approximately 15% Faster than Standard
- –2 = Approximately 25% Faster than Standard
- –3 = Approximately 35% Faster than Standard

- Blank = Not PCI Compliant
- P = PCI Compliant

Part Number
- A54SX08 = 12,000 System Gates
- A54SX16 = 24,000 System Gates
- A54SX16P = 24,000 System Gates
- A54SX32 = 48,000 System Gates

Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PLCC 84-Pin	**VQFP 100-Pin**	**PQFP 208-Pin**	**TQFP 144-Pin**	**TQFP 176-Pin**	**PBGA 313-Pin**	**PBGA 329-Pin**	**FBGA 144-Pin**
A54SX08	69	81	130	113	128	–	–	111
A54SX16	–	81	175	–	147	–	–	–
A54SX16P	–	81	175	113	147	–	–	–
A54SX32	–	–	174	113	147	249	249	–

Note: *Package Definitions (Consult your local Actel sales representative for product availability):*
PLCC = Plastic Leaded Chip Carrier
PQFP = Plastic Quad Flat Pack
TQFP = Thin Quad Flat Pack
VQFP = Very Thin Quad Flat Pack
PBGA = Plastic Ball Grid Array
FBGA = Fine Pitch (1.0 mm) Ball Grid Array

SX Family FPGAs

General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX's flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

Logic Module Design

The SX family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.

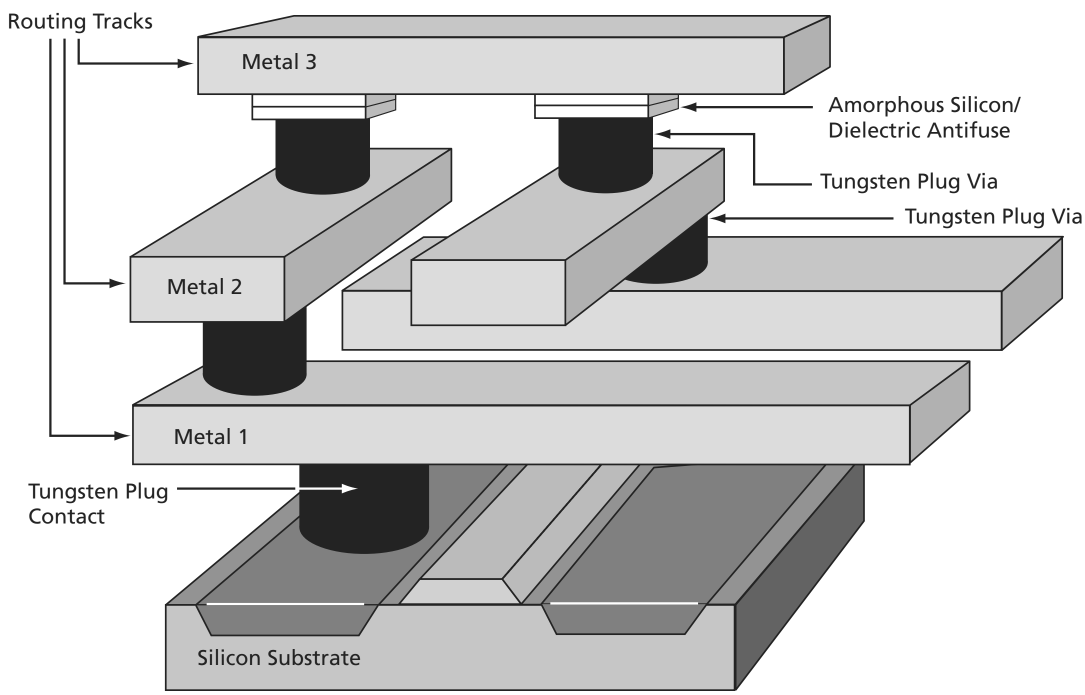

Figure 1-1 • **SX Family Interconnect Elements**

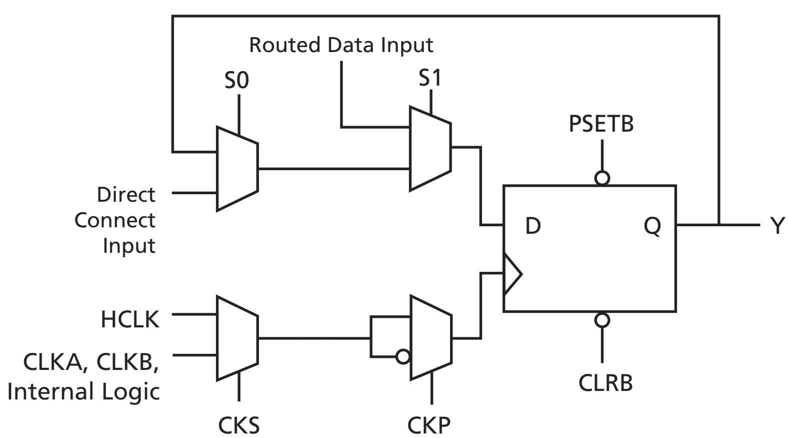

Figure 1-2 • **R-Cell**

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

Boundary Scan Testing (BST)

All SX devices are IEEE 1149.1 compliant. SX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 1-2. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10 kΩ. TMS can be pulled LOW to initiate the test sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

Table 1-2 • **Boundary Scan Pin Functionality**

Program Fuse Blown (Dedicated Test Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated BST pins.	TCK, TDI, TDO are flexible and may be used as I/Os.
No need for pull-up resistor for TMS	Use a pull-up resistor of 10 kΩ on TMS.

Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software by checking the "Reserve JTAG" box in "Device Selection Wizard" (Figure 1-7). JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the Table 1-5 on page 1-8 for detailed specifications.

Figure 1-7 • **Device Selection Wizard**

Development Tool Support

The SX family of FPGAs is fully supported by both the Actel Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the Libero IDE flow diagram (located on the Actel website) for more information.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators, and the simulation results can be cross-probed with Silicon Explorer II, Actel integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Actel Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys®, and Cadence® Design Systems. The Designer software is available for both the Windows® and UNIX® operating systems.

Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-8 on page 1-7 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuitry.

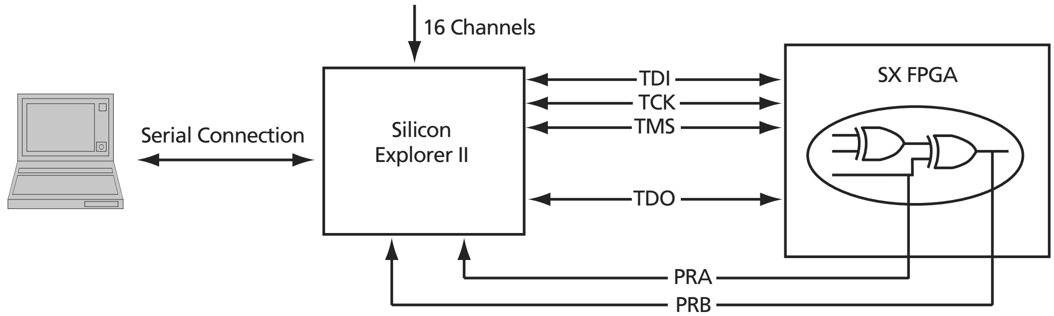

Figure 1-8 • **Probe Setup**

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II are compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an SX device using Silicon Sculptor II are as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming SX devices, refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

3.3 V / 5 V Operating Conditions

Table 1-3 • **Absolute Maximum Ratings**[1]

Symbol	Parameter	Limits	Units
V_{CCR}[2]	DC Supply Voltage[3]	–0.3 to + 6.0	V
V_{CCA}[2]	DC Supply Voltage	–0.3 to + 4.0	V
V_{CCI}[2]	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	–0.3 to + 4.0	V
V_{CCI}[2]	DC Supply Voltage (A54SX16P)	–0.3 to + 6.0	V
V_I	Input Voltage	–0.5 to + 5.5	V
V_O	Output Voltage	–0.5 to + 3.6	V
I_{IO}	I/O Source Sink Current[3]	–30 to + 5.0	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *V_{CCR} in the A54SX16P must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.*
3. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward-bias and can draw excessive current.*

Table 1-4 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to + 70	–40 to + 85	–55 to +125	°C
3.3 V Power Supply Tolerance	±10	±10	±10	$\%V_{CC}$
5.0 V Power Supply Tolerance	±5	±10	±10	$\%V_{CC}$

Note: **Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Table 1-5 • **Electrical Specifications**

		Commercial		Industrial		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{OH}	(I_{OH} = –20 µA) (CMOS) (I_{OH} = –8 mA) (TTL) (I_{OH} = –6 mA) (TTL)	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	V
V_{OL}	(I_{OL}= 20 µA) (CMOS) (I_{OL} = 12 mA) (TTL) (I_{OL} = 8 mA) (TTL)		0.10 0.50		 0.50	V
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		4.0	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See "Evaluating Power in SX Devices" on page 1-16.				

A54SX16P DC Specifications (3.3 V PCI Operation)

Table 1-8 • **A54SX16P DC Specifications (3.3 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		3.0	3.6	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CC}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CC}$		±10	µA
V_{OH}	Output High Voltage	$I_{OUT} = –500$ µA	$0.9V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OUT} = 1500$ µA		$0.1V_{CC}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance[4]			8	pF

Notes:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*
4. *Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].*

Power-Up Sequencing

Table 1-10 • **Power-Up Sequencing**

V_{CCA}	V_{CCR}	V_{CCI}	Power-Up Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Note: *No inputs should be driven (high or low) before completion of power-up.*

Power-Down Sequencing

Table 1-11 • **Power-Down Sequencing**

V_{CCA}	V_{CCR}	V_{CCI}	Power-Down Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Note: *No inputs should be driven (high or low) after the beginning of the power-down sequence.*

Table 1-15 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min.	Units
Plastic Leaded Chip Carrier (PLCC)	84	12	32	22	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Very Thin Quad Flatpack (VQFP)	100	10	38	32	°C/W
Plastic Quad Flat Pack (PQFP) without Heat Spreader	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	14.5	°C/W
Plastic Ball Grid Array (PBGA)	313	3	23	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W

Note: *SX08 does not have a heat spreader.*

Table 1-16 • **Temperature and Voltage Derating Factors***

V_{CCA}	Junction Temperature						
	–55	**–40**	**0**	**25**	**70**	**85**	**125**
3.0	0.75	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.70	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.66	0.69	0.77	0.78	0.87	0.92	1.02

Note: **Normalized to worst-case commercial, T_J = 70°C, V_{CCA} = 3.0 V*

A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH}, the loading is 5 pF.*

A54SX16P Timing Characteristics

Table 1-19 • **A54SX16P Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.9		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 10 pF loading.*

Table 1-19 • **A54SX16P Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL/PCI Output Module Timing										
t_{DLH}	Data-to-Pad LOW to HIGH		1.5		1.7		2.0		2.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.9		2.2		2.4		2.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.3		2.6		3.0		3.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.5		1.7		1.9		2.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.7		3.1		3.5		4.1	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.7		4.4	ns
PCI Output Module Timing[3]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.8		2.0		2.3		2.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.7		2.0		2.2		2.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		0.8		1.0		1.1		1.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.2		1.2		1.5		1.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.0		1.1		1.3		1.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.1		1.3		1.5		1.7	ns
TTL Output Module Timing										
t_{DLH}	Data-to-Pad LOW to HIGH		2.1		2.5		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.0		2.3		2.6		3.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		2.9		3.2		3.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.0		3.5		3.9		4.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.3		2.7		3.1		3.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.7		4.4	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 10 pF loading.*

Table 1-20 • **A54SX32 Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (pad to R-Cell input)		1.9		2.1		2.4		2.8	ns
t_{HCKL}	Input HIGH to LOW (pad to R-Cell input)		1.9		2.1		2.4		2.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)		2.4		2.7		3.0		3.5	ns
t_{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell input)		2.4		2.7		3.1		3.6	ns
t_{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)		2.7		3.0		3.5		4.1	ns
t_{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)		2.7		3.1		3.6		4.2	ns
t_{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)		2.7		3.1		3.5		4.1	ns
t_{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)		2.8		3.2		3.6		4.3	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (light load)		0.85		0.98		1.1		1.3	ns
t_{RCKSW}	Maximum Skew (50% load)		1.23		1.4		1.6		1.9	ns
t_{RCKSW}	Maximum Skew (100% load)		1.30		1.5		1.7		2.0	ns
TTL Output Module Timing[3]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Note:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.*

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V_{CCA}	V_{CCA}	V_{CCA}
80	V_{CCI}	V_{CCI}	V_{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V_{CCA}	V_{CCA}	V_{CCA}
90	V_{CCR}	V_{CCR}	V_{CCR}
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V_{CCI}	V_{CCI}	V_{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
109	GND	GND	GND
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V_{CCI}	V_{CCI}	V_{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	V_{CCR}	V_{CCR}	V_{CCR}
128	GND	GND	GND
129	V_{CCA}	V_{CCA}	V_{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V_{CCI}	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V_{CCI}	V_{CCI}	V_{CCI}
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V_{CCA}	V_{CCA}	V_{CCA}
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V_{CCI}	V_{CCI}	V_{CCI}
33	V_{CCA}	V_{CCA}	V_{CCA}
34	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V_{CCI}	V_{CCI}	V_{CCI}
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V_{CCA}	V_{CCA}	V_{CCA}
67	V_{CCR}	V_{CCR}	V_{CCR}
68	I/O	I/O	I/O

313-Pin PBGA

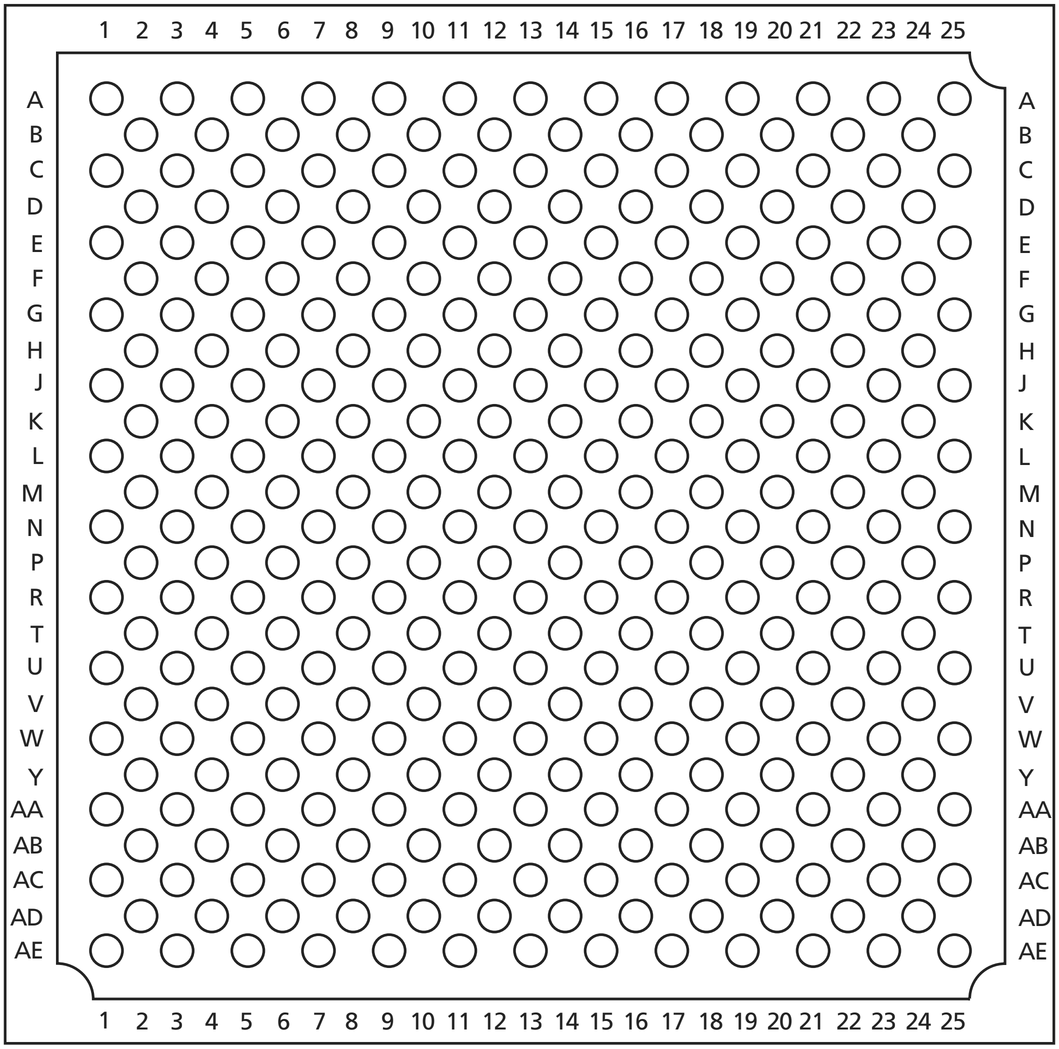

Figure 2-6 • **313-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

329-Pin PBGA

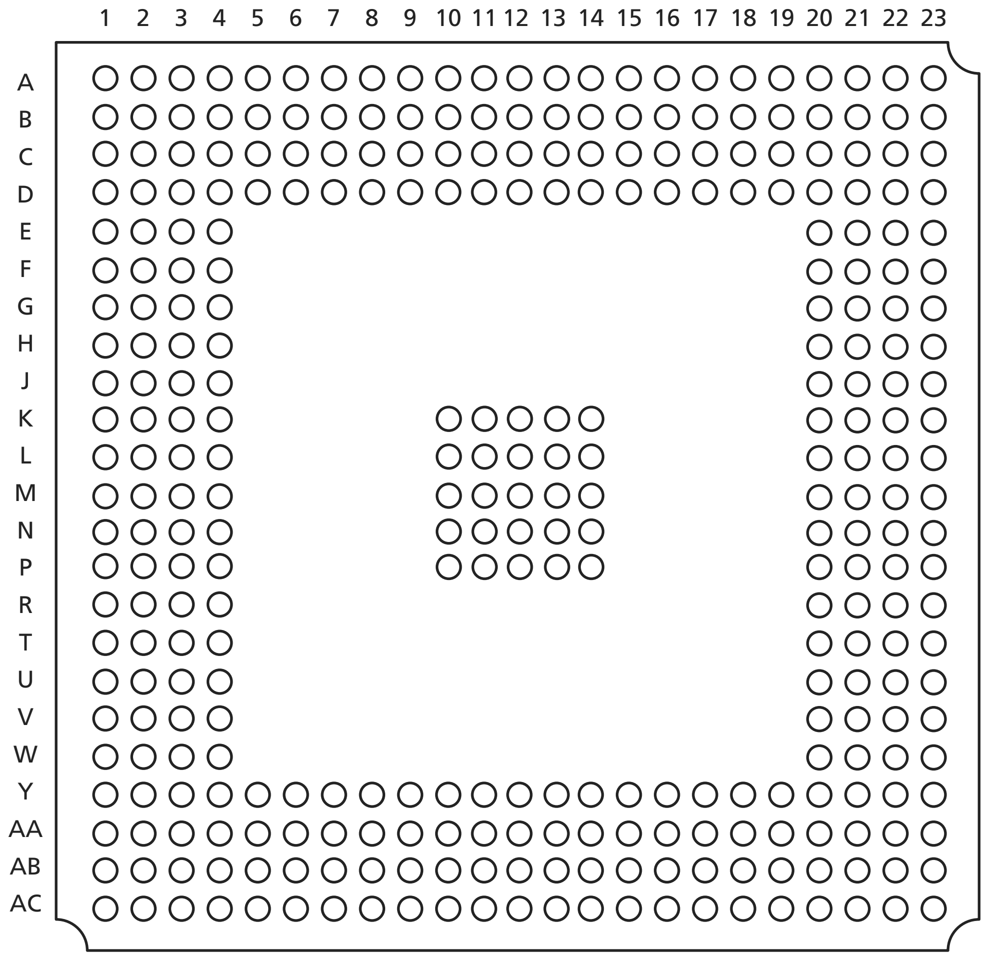

Figure 2-7 • **329-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

329-Pin PBGA	
Pin Number	A54SX32 Function
A1	GND
A2	GND
A3	V_{CCI}
A4	NC
A5	I/O
A6	I/O
A7	V_{CCI}
A8	NC
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	CLKB
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
A20	I/O
A21	NC
A22	V_{CCI}
A23	GND
AA1	V_{CCI}
AA2	I/O
AA3	GND
AA4	I/O
AA5	I/O
AA6	I/O
AA7	I/O
AA8	I/O
AA9	I/O
AA10	I/O
AA11	I/O
AA12	I/O

329-Pin PBGA	
Pin Number	A54SX32 Function
AA13	I/O
AA14	I/O
AA15	I/O
AA16	I/O
AA17	I/O
AA18	I/O
AA19	I/O
AA20	TDO, I/O
AA21	V_{CCI}
AA22	I/O
AA23	V_{CCI}
AB1	I/O
AB2	GND
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AB10	I/O
AB11	PRB, I/O
AB12	I/O
AB13	HCLK
AB14	I/O
AB15	I/O
AB16	I/O
AB17	I/O
AB18	I/O
AB19	I/O
AB20	I/O
AB21	I/O
AB22	GND
AB23	I/O
AC1	GND

329-Pin PBGA	
Pin Number	A54SX32 Function
AC2	V_{CCI}
AC3	NC
AC4	I/O
AC5	I/O
AC6	I/O
AC7	I/O
AC8	I/O
AC9	V_{CCI}
AC10	I/O
AC11	I/O
AC12	I/O
AC13	I/O
AC14	I/O
AC15	NC
AC16	I/O
AC17	I/O
AC18	I/O
AC19	I/O
AC20	I/O
AC21	NC
AC22	V_{CCI}
AC23	GND
B1	V_{CCI}
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	PRA, I/O
B13	CLKA

329-Pin PBGA	
Pin Number	A54SX32 Function
B14	I/O
B15	I/O
B16	I/O
B17	I/O
B18	I/O
B19	I/O
B20	I/O
B21	I/O
B22	GND
B23	V_{CCI}
C1	NC
C2	TDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O
C21	V_{CCI}
C22	GND
C23	NC
D1	I/O
D2	I/O

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