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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	175
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	208-BFCQFP with Tie Bar
Supplier Device Package	208-CQFP (75x75)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a54sx16-1cq208m">https://www.e-xfl.com/product-detail/microsemi/a54sx16-1cq208m</a>

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# SX Family FPGAs

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## General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or “sea-of-modules”), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX’s flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

## SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

### Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

### Logic Module Design

The SX family architecture is described as a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional

flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.

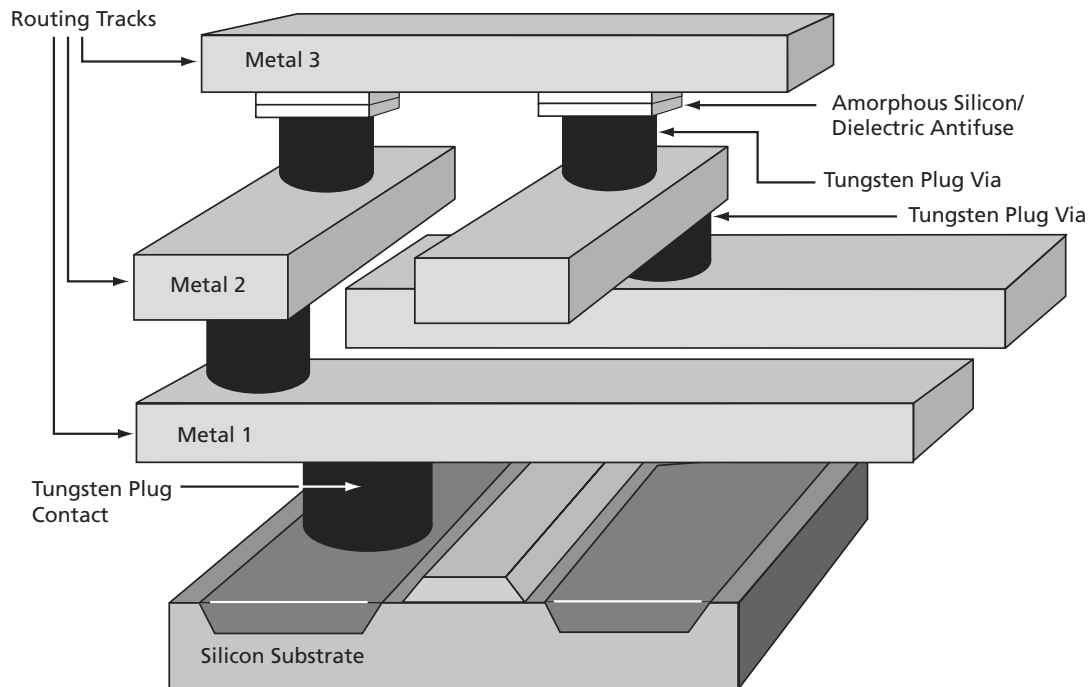


Figure 1-1 • SX Family Interconnect Elements

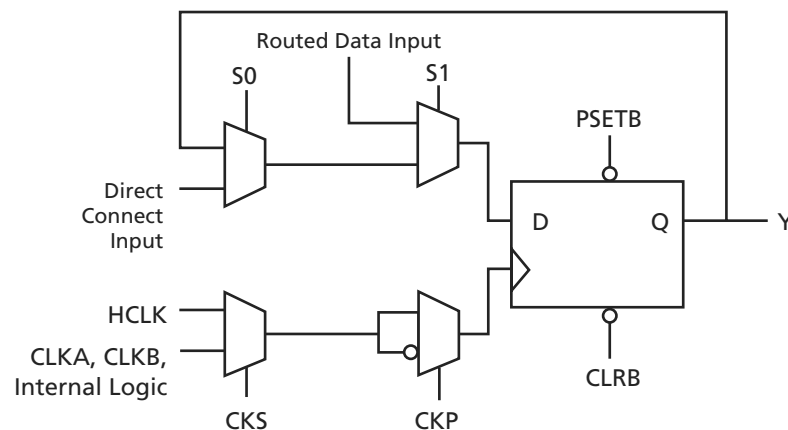


Figure 1-2 • R-Cell

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility

enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

## Boundary Scan Testing (BST)

All SX devices are IEEE 1149.1 compliant. SX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 1-2. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10 kΩ. TMS can be pulled LOW to initiate the test sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

Table 1-2 • Boundary Scan Pin Functionality

Program Fuse Blown (Dedicated Test Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated BST pins.	TCK, TDI, TDO are flexible and may be used as I/Os.
No need for pull-up resistor for TMS	Use a pull-up resistor of 10 kΩ on TMS.

## Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software by checking the "Reserve JTAG" box in "Device Selection Wizard" (Figure 1-7). JTAG pins comply with LVTTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the Table 1-5 on page 1-8 for detailed specifications.

## Development Tool Support

The SX family of FPGAs is fully supported by both the Actel Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, ModelSim® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the Libero IDE flow diagram (located on the Actel website) for more information.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators, and the simulation results can be cross-probed with Silicon Explorer II, Actel integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Actel Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys®, and Cadence® Design Systems. The Designer software is available for both the Windows® and UNIX® operating systems.

## Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-8 on page 1-7 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

## Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuitry.

Figure 1-7 • Device Selection Wizard

## PCI Compliance for the SX Family

The SX family supports 3.3 V and 5.0 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 1-6 • A54SX16P DC Specifications (5.0 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V <sub>CCA</sub>	Supply Voltage for Array		3.0	3.6	V
V <sub>CCR</sub>	Supply Voltage required for Internal Biasing		4.75	5.25	V
V <sub>CCI</sub>	Supply Voltage for I/Os		4.75	5.25	V
V <sub>IH</sub>	Input High Voltage <sup>1</sup>		2.0	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input Low Voltage <sup>1</sup>		-0.5	0.8	V
I <sub>IH</sub>	Input High Leakage Current	V <sub>IN</sub> = 2.7		70	μA
I <sub>IL</sub>	Input Low Leakage Current	V <sub>IN</sub> = 0.5		-70	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> = -2 mA	2.4		V
V <sub>OL</sub>	Output Low Voltage <sup>2</sup>	I <sub>OUT</sub> = 3 mA, 6 mA		0.55	V
C <sub>IN</sub>	Input Pin Capacitance <sup>3</sup>			10	pF
C <sub>CLK</sub>	CLK Pin Capacitance		5	12	pF
C <sub>IDSEL</sub>	IDSEL Pin Capacitance <sup>4</sup>			8	pF

### Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used, AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

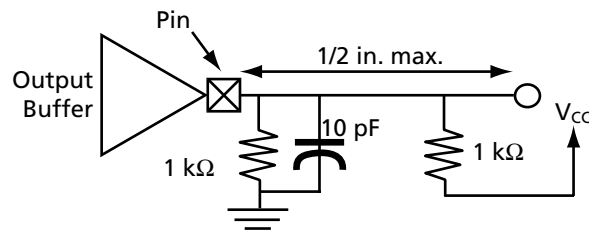
## A54SX16P AC Specifications for (PCI Operation)

Table 1-7 • A54SX16P AC Specifications for (PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4^1$	-44		mA
		$1.4 \leq V_{OUT} < 2.4^1, ^2$	$-44 + (V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}^{1, 3}$		EQ 1-1 on page 1-11	
	(Test Point)	$V_{OUT} = 3.1^3$		-142	mA
$I_{OL(AC)}$	Switching Current High	$V_{OUT} \geq 2.2^1$	95		mA
		$2.2 > V_{OUT} > 0.55^1$	$V_{OUT}/0.023$		
		$0.71 > V_{OUT} > 0^{1, 3}$		EQ 1-2 on page 1-11	mA
	(Test Point)	$V_{OUT} = 0.71^3$		206	mA
$I_{CL}$	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load <sup>4</sup>	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load <sup>4</sup>	1	5	V/ns

### Notes:

1. Refer to the *V<sub>I</sub>* curves in Figure 1-9 on page 1-11. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half-size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maxima (A and B) are provided with the respective diagrams in Figure 1-9 on page 1-11. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.



# A54SX16P AC Specifications (3.3 V PCI Operation)

Table 1-9 • A54SX16P AC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CC}^1$			mA
		$0.3V_{CC} \leq V_{OUT} < 0.9V_{CC}^1$	$-12V_{CC}$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}^{1,2}$	$-17.1 + (V_{CC} - V_{OUT})$	EQ 1-3 on page 1-14	
	(Test Point)	$V_{OUT} = 0.7V_{CC}^2$		$-32V_{CC}$	mA
$I_{OL(AC)}$	Switching Current High	$V_{CC} > V_{OUT} \geq 0.6V_{CC}^1$			mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}^1$	$16V_{CC}$		mA
		$0.18V_{CC} > V_{OUT} > 0^{1,2}$	$26.7V_{OUT}$	EQ 1-4 on page 1-14	mA
	(Test Point)	$V_{OUT} = 0.18V_{CC}^2$		$38V_{CC}$	
$I_{CL}$	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$I_{CH}$	High Clamp Current	$-3 < V_{IN} \leq -1$	$25 + (V_{IN} - V_{OUT} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate <sup>3</sup>	0.2V <sub>CC</sub> to 0.6V <sub>CC</sub> load	1	4	V/ns
$slew_F$	Output Fall Slew Rate <sup>3</sup>	0.6V <sub>CC</sub> to 0.2V <sub>CC</sub> load	1	4	V/ns

## Notes:

1. Refer to the V/I curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.

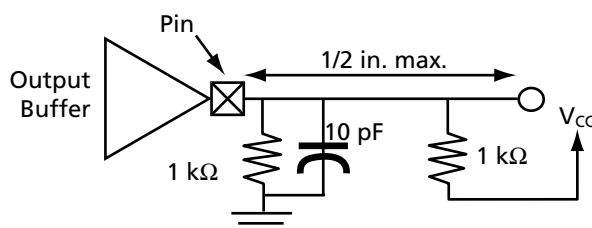


Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.

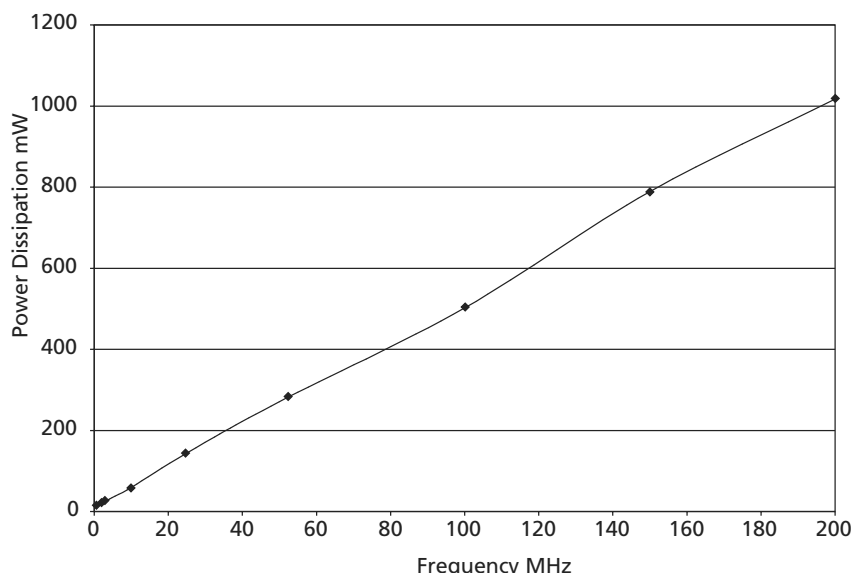


Figure 1-11 • Power Dissipation

## Junction Temperature ( $T_j$ )

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a$$

EQ 1-13

Where:

$T_a$  = Ambient Temperature

$\Delta T$  = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} \times P$$

$P$  = Power calculated from Estimating Power Consumption section

$\theta_{ja}$  = Junction to ambient of package.  $\theta_{ja}$  numbers are located in the "Package Thermal Characteristics" section.

## Package Thermal Characteristics

The device junction to case thermal characteristic is  $\theta_{jc}$ , and the junction to ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

The maximum junction temperature is 150 °C.

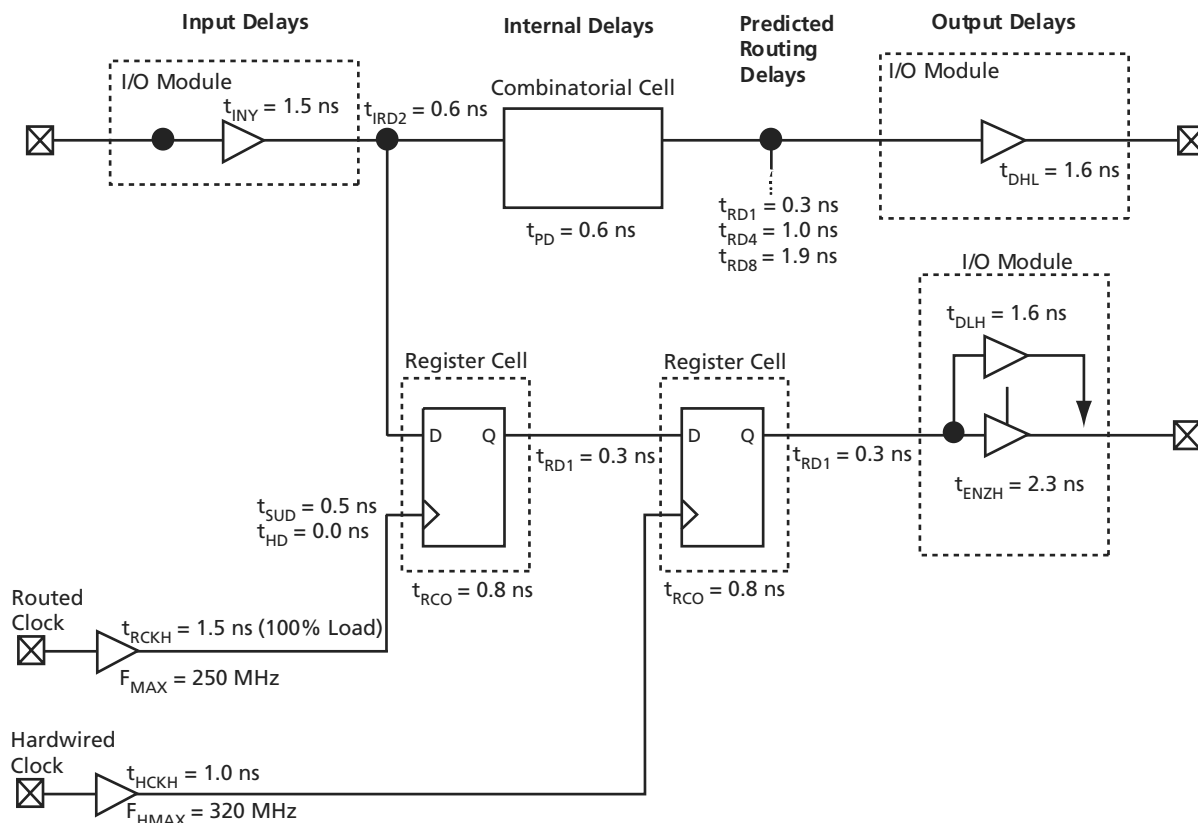
A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ (°C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{28^\circ\text{C/W}} = 2.86 \text{ W}$$

EQ 1-14



# SX Timing Model



**Note:** Values shown for A54SX08-3, worst-case commercial conditions.

Figure 1-12 • SX Timing Model

## Hardwired Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.0 = 1.3 \text{ ns} \end{aligned}$$

EQ 1-15

## Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.0 + 0.8 + 0.3 + 1.6 = 3.7 \text{ ns} \end{aligned}$$

EQ 1-16

## Routed Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.5 = 0.8 \text{ ns} \end{aligned}$$

EQ 1-17

## Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.52 + 0.8 + 0.3 + 1.6 = 4.2 \text{ ns} \end{aligned}$$

EQ 1-18

**Table 1-18 • A54SX16 Timing Characteristics (Continued)**  
**(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t <sub>HCKH</sub>	Input LOW to HIGH (pad to R-Cell input)	1.2		1.4		1.5		1.8		ns
t <sub>HCKL</sub>	Input HIGH to LOW (pad to R-Cell input)	1.2		1.4		1.6		1.9		ns
t <sub>HPWH</sub>	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t <sub>HPWL</sub>	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t <sub>HCKSW</sub>	Maximum Skew	0.2		0.2		0.3		0.3		ns
t <sub>HP</sub>	Minimum Period	2.7		3.1		3.6		4.2		ns
f <sub>HMAX</sub>	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t <sub>RCKH</sub>	Input LOW to HIGH (light load) (pad to R-Cell input)	1.6		1.8		2.1		2.5		ns
t <sub>RCKL</sub>	Input HIGH to LOW (light load) (pad to R-Cell input)	1.8		2.0		2.3		2.7		ns
t <sub>RCKH</sub>	Input LOW to HIGH (50% load) (pad to R-Cell input)	1.8		2.1		2.5		2.8		ns
t <sub>RCKL</sub>	Input HIGH to LOW (50% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t <sub>RCKH</sub>	Input LOW to HIGH (100% load) (pad to R-Cell input)	1.8		2.1		2.4		2.8		ns
t <sub>RCKL</sub>	Input HIGH to LOW (100% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t <sub>RPWH</sub>	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t <sub>RPWL</sub>	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t <sub>RCKSW</sub>	Maximum Skew (light load)	0.5		0.5		0.5		0.7		ns
t <sub>RCKSW</sub>	Maximum Skew (50% load)	0.5		0.6		0.7		0.8		ns
t <sub>RCKSW</sub>	Maximum Skew (100% load)	0.5		0.6		0.7		0.8		ns
TTL Output Module Timing <sup>3</sup>										
t <sub>DLH</sub>	Data-to-Pad LOW to HIGH	1.6		1.9		2.1		2.5		ns
t <sub>DHL</sub>	Data-to-Pad HIGH to LOW	1.6		1.9		2.1		2.5		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	2.1		2.4		2.8		3.2		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	2.3		2.7		3.1		3.6		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	1.4		1.7		1.9		2.2		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	1.3		1.5		1.7		2.0		ns

**Notes:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except  $t_{ENZL}$  and  $t_{ENZH}$ . For  $t_{ENZL}$  and  $t_{ENZH}$ , the loading is 5 pF.

## A54SX16P Timing Characteristics

Table 1-19 • **A54SX16P Timing Characteristics**  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>1</sup>										
t <sub>PD</sub>	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays <sup>2</sup>										
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t <sub>RCO</sub>	Sequential Clock-to-Q	0.9		1.1		1.3		1.4		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t <sub>INYH</sub>	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t <sub>INYL</sub>	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays <sup>2</sup>										
t <sub>IRD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>IRD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

**Note:**

1. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 10 pF loading.

Table 1-19 • A54SX16P Timing Characteristics (Continued)

(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t <sub>HCKH</sub>	Input LOW to HIGH (pad to R-Cell input)	1.2		1.4		1.5		1.8		ns
t <sub>HCKL</sub>	Input HIGH to LOW (pad to R-Cell input)	1.2		1.4		1.6		1.9		ns
t <sub>HPWH</sub>	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t <sub>HPWL</sub>	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t <sub>HCKSW</sub>	Maximum Skew	0.2		0.2		0.3		0.3		ns
t <sub>HP</sub>	Minimum Period	2.7		3.1		3.6		4.2		ns
f <sub>HMAX</sub>	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t <sub>RCKH</sub>	Input LOW to HIGH (light load) (pad to R-Cell input)	1.6		1.8		2.1		2.5		ns
t <sub>RCKL</sub>	Input HIGH to LOW (Light Load) (pad to R-Cell input)	1.8		2.0		2.3		2.7		ns
t <sub>RCKH</sub>	Input LOW to HIGH (50% load) (pad to R-Cell input)	1.8		2.1		2.5		2.8		ns
t <sub>RCKL</sub>	Input HIGH to LOW (50% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t <sub>RCKH</sub>	Input LOW to HIGH (100% load) (pad to R-Cell input)	1.8		2.1		2.4		2.8		ns
t <sub>RCKL</sub>	Input HIGH to LOW (100% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t <sub>RPWH</sub>	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t <sub>RPWL</sub>	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t <sub>RCKSW</sub>	Maximum Skew (light load)	0.5		0.5		0.5		0.7		ns
t <sub>RCKSW</sub>	Maximum Skew (50% load)	0.5		0.6		0.7		0.8		ns
t <sub>RCKSW</sub>	Maximum Skew (100% load)	0.5		0.6		0.7		0.8		ns
TTL Output Module Timing										
t <sub>DLH</sub>	Data-to-Pad LOW to HIGH	2.4		2.8		3.1		3.7		ns
t <sub>DHL</sub>	Data-to-Pad HIGH to LOW	2.3		2.9		3.2		3.8		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	3.0		3.4		3.9		4.6		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	3.3		3.8		4.3		5.0		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	2.3		2.7		3.0		3.5		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	2.8		3.2		3.7		4.3		ns

**Note:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 10 pF loading.



## 208-Pin PQFP

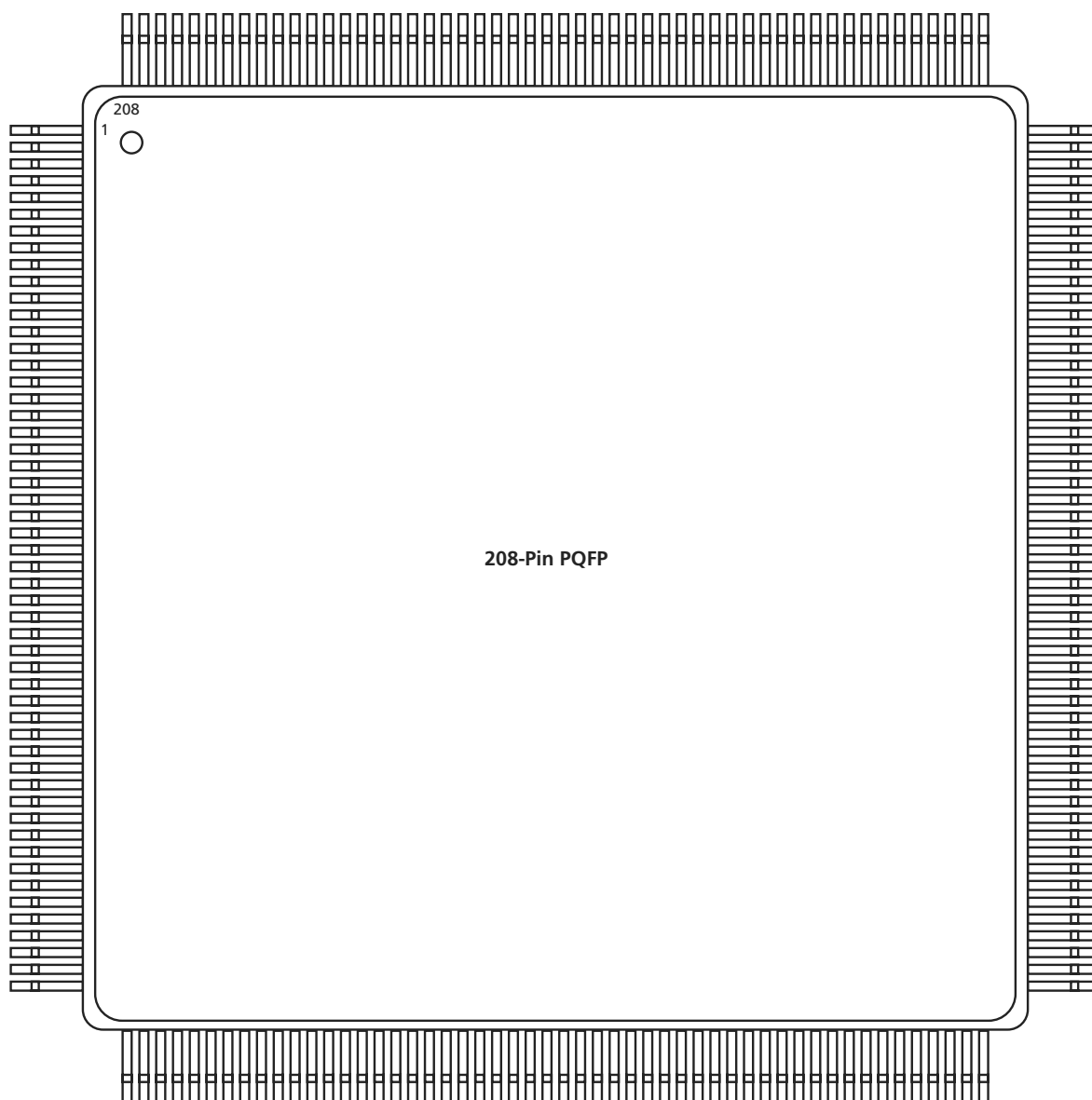


Figure 2-2 • 208-Pin PQFP (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
73	NC	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND
78	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
79	GND	GND	GND
80	V <sub>CCR</sub>	V <sub>CCR</sub>	V <sub>CCR</sub>
81	I/O	I/O	I/O
82	HCLK	HCLK	HCLK
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	NC	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	NC	I/O	I/O
89	I/O	I/O	I/O
90	I/O	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	NC	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	NC	I/O	I/O
98	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	I/O	I/O
107	I/O	I/O	I/O
108	NC	I/O	I/O

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
115	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
116	NC	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	NC	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	NC	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	NC	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	GND	GND	GND
130	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
131	GND	GND	GND
132	V <sub>CCR</sub>	V <sub>CCR</sub>	V <sub>CCR</sub>
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	I/O	I/O	I/O

**Note:** \* Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
145	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
146	GND	GND	GND
147	I/O	I/O	I/O
148	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	NC	I/O	I/O
156	NC	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	NC	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	NC	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	NC	I/O	I/O
177	I/O	I/O	I/O
178	I/O	I/O	I/O
179	I/O	I/O	I/O
180	CLKA	CLKA	CLKA

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
181	CLKB	CLKB	CLKB
182	V <sub>CCR</sub>	V <sub>CCR</sub>	V <sub>CCR</sub>
183	GND	GND	GND
184	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
185	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	NC	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	NC	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	NC	I/O	I/O
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	NC	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
202	NC	I/O	I/O
203	NC	I/O	I/O
204	I/O	I/O	I/O
205	NC	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O

**Note:** \* Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).



176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
33	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
34	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
67	V <sub>CCR</sub>	V <sub>CCR</sub>	V <sub>CCR</sub>
68	I/O	I/O	I/O

100-Pin VQFP		
Pin Number	A545X08 Function	A545X16, A545X16P Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	TMS	TMS
8	V <sub>CCI</sub>	V <sub>CCI</sub>
9	GND	GND
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	V <sub>CCI</sub>	V <sub>CCI</sub>
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	PRB, I/O	PRB, I/O

100-Pin VQFP		
Pin Number	A545X08 Function	A545X16, A545X16P Function
35	V <sub>CCA</sub>	V <sub>CCA</sub>
36	GND	GND
37	V <sub>CCR</sub>	V <sub>CCR</sub>
38	I/O	I/O
39	HCLK	HCLK
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	V <sub>CCI</sub>	V <sub>CCI</sub>
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	TDO, I/O	TDO, I/O
50	I/O	I/O
51	GND	GND
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	V <sub>CCA</sub>	V <sub>CCA</sub>
58	V <sub>CCI</sub>	V <sub>CCI</sub>
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	V <sub>CCA</sub>	V <sub>CCA</sub>
68	GND	GND

100-Pin VQFP		
Pin Number	A545X08 Function	A545X16, A545X16P Function
69	GND	GND
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	V <sub>CCI</sub>	V <sub>CCI</sub>
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	CLKA	CLKA
88	CLKB	CLKB
89	V <sub>CCR</sub>	V <sub>CCR</sub>
90	V <sub>CCA</sub>	V <sub>CCA</sub>
91	GND	GND
92	PRA, I/O	PRA, I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	TCK, I/O	TCK, I/O

313-Pin PBGA		313-Pin PBGA		313-Pin PBGA		313-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
A1	GND	AC5	I/O	B10	I/O	E15	I/O
A3	NC	AC7	I/O	B12	I/O	E17	I/O
A5	I/O	AC9	I/O	B14	I/O	E19	I/O
A7	I/O	AC11	I/O	B16	I/O	E21	I/O
A9	I/O	AC13	V <sub>CCR</sub>	B18	I/O	E23	I/O
A11	I/O	AC15	I/O	B20	I/O	E25	I/O
A13	V <sub>CCR</sub>	AC17	I/O	B22	I/O	F2	I/O
A15	I/O	AC19	I/O	B24	I/O	F4	I/O
A17	I/O	AC21	I/O	C1	TDI, I/O	F6	NC
A19	I/O	AC23	I/O	C3	I/O	F8	I/O
A21	I/O	AC25	NC	C5	NC	F10	NC
A23	NC	AD2	GND	C7	I/O	F12	I/O
A25	GND	AD4	I/O	C9	I/O	F14	I/O
AA1	I/O	AD6	V <sub>CCI</sub>	C11	I/O	F16	NC
AA3	I/O	AD8	I/O	C13	V <sub>CCI</sub>	F18	I/O
AA5	NC	AD10	I/O	C15	I/O	F20	I/O
AA7	I/O	AD12	PRB, I/O	C17	I/O	F22	I/O
AA9	NC	AD14	I/O	C19	V <sub>CCI</sub>	F24	I/O
AA11	I/O	AD16	I/O	C21	I/O	G1	I/O
AA13	I/O	AD18	I/O	C23	I/O	G3	TMS
AA15	I/O	AD20	I/O	C25	NC	G5	I/O
AA17	I/O	AD22	NC	D2	I/O	G7	I/O
AA19	I/O	AD24	I/O	D4	NC	G9	V <sub>CCI</sub>
AA21	I/O	AE1	NC	D6	I/O	G11	I/O
AA23	NC	AE3	I/O	D8	I/O	G13	CLKB
AA25	I/O	AE5	I/O	D10	I/O	G15	I/O
AB2	NC	AE7	I/O	D12	I/O	G17	I/O
AB4	NC	AE9	I/O	D14	I/O	G19	I/O
AB6	I/O	AE11	I/O	D16	I/O	G21	I/O
AB8	I/O	AE13	V <sub>CCA</sub>	D18	I/O	G23	I/O
AB10	I/O	AE15	I/O	D20	I/O	G25	I/O
AB12	I/O	AE17	I/O	D22	I/O	H2	I/O
AB14	I/O	AE19	I/O	D24	NC	H4	I/O
AB16	I/O	AE21	I/O	E1	I/O	H6	I/O
AB18	V <sub>CCI</sub>	AE23	TDO, I/O	E3	NC	H8	I/O
AB20	NC	AE25	GND	E5	I/O	H10	I/O
AB22	I/O	B2	TCK, I/O	E7	I/O	H12	PRA, I/O
AB24	I/O	B4	I/O	E9	I/O	H14	I/O
AC1	I/O	B6	I/O	E11	I/O	H16	I/O
AC3	I/O	B8	I/O	E13	V <sub>CCA</sub>	H18	NC

# 144-Pin FBGA

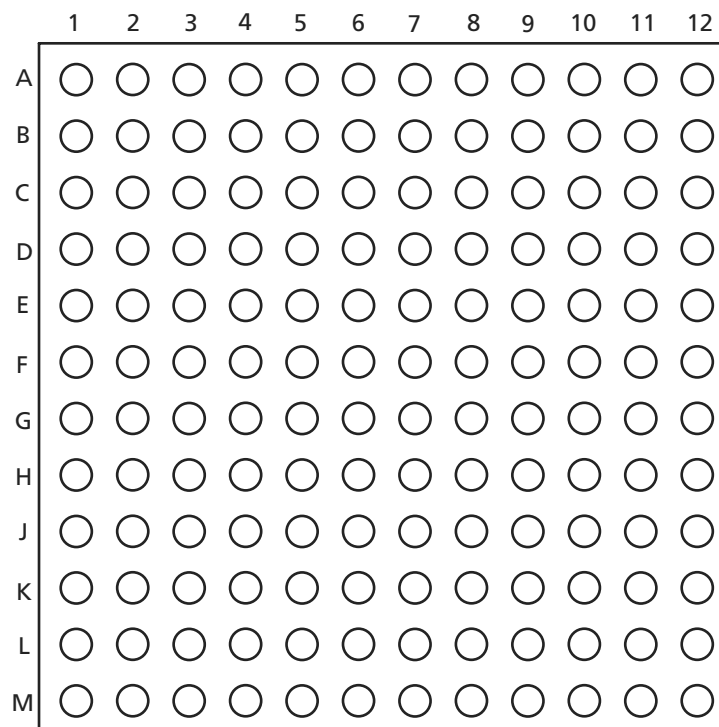


Figure 2-8 • 144-Pin FBGA (Top View)

## Note

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