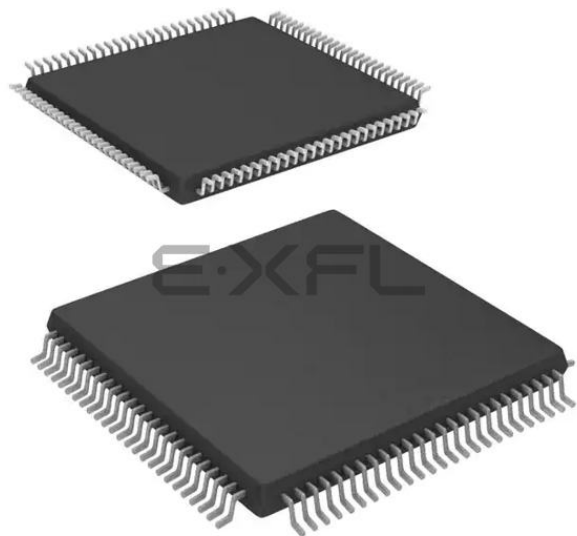




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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                               |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                                      |
| Number of LABs/CLBs            | 1452                                                                                                                                          |
| Number of Logic Elements/Cells | -                                                                                                                                             |
| Total RAM Bits                 | -                                                                                                                                             |
| Number of I/O                  | 81                                                                                                                                            |
| Number of Gates                | 24000                                                                                                                                         |
| Voltage - Supply               | 3V ~ 3.6V, 4.75V ~ 5.25V                                                                                                                      |
| Mounting Type                  | Surface Mount                                                                                                                                 |
| Operating Temperature          | -40°C ~ 85°C (TA)                                                                                                                             |
| Package / Case                 | 100-TQFP                                                                                                                                      |
| Supplier Device Package        | 100-VQFP (14x14)                                                                                                                              |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/microsemi/a54sx16-1vqg100i">https://www.e-xfl.com/product-detail/microsemi/a54sx16-1vqg100i</a> |

## A54SX16P AC Specifications for (PCI Operation)

Table 1-7 • A54SX16P AC Specifications for (PCI Operation)

| Symbol       | Parameter              | Condition                        | Min.                          | Max.                | Units |
|--------------|------------------------|----------------------------------|-------------------------------|---------------------|-------|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 1.4^1$         | -44                           |                     | mA    |
|              |                        | $1.4 \leq V_{OUT} < 2.4^1, ^2$   | $-44 + (V_{OUT} - 1.4)/0.024$ |                     | mA    |
|              |                        | $3.1 < V_{OUT} < V_{CC}^{1, ^3}$ |                               | EQ 1-1 on page 1-11 |       |
|              | (Test Point)           | $V_{OUT} = 3.1^3$                |                               | -142                | mA    |
| $I_{OL(AC)}$ | Switching Current High | $V_{OUT} \geq 2.2^1$             | 95                            |                     | mA    |
|              |                        | $2.2 > V_{OUT} > 0.55^1$         | $V_{OUT}/0.023$               |                     |       |
|              |                        | $0.71 > V_{OUT} > 0^{1, ^3}$     |                               | EQ 1-2 on page 1-11 | mA    |
|              | (Test Point)           | $V_{OUT} = 0.71^3$               |                               | 206                 | mA    |
| $I_{CL}$     | Low Clamp Current      | $-5 < V_{IN} \leq -1$            | $-25 + (V_{IN} + 1)/0.015$    |                     | mA    |
| $slew_R$     | Output Rise Slew Rate  | 0.4 V to 2.4 V load <sup>4</sup> | 1                             | 5                   | V/ns  |
| $slew_F$     | Output Fall Slew Rate  | 2.4 V to 0.4 V load <sup>4</sup> | 1                             | 5                   | V/ns  |

### Notes:

1. Refer to the *V<sub>I</sub>* curves in Figure 1-9 on page 1-11. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half-size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maxima (A and B) are provided with the respective diagrams in Figure 1-9 on page 1-11. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

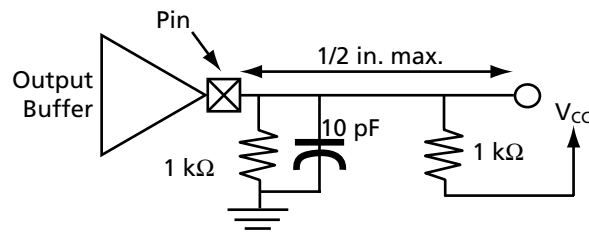


Figure 1-9 shows the 5.0 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

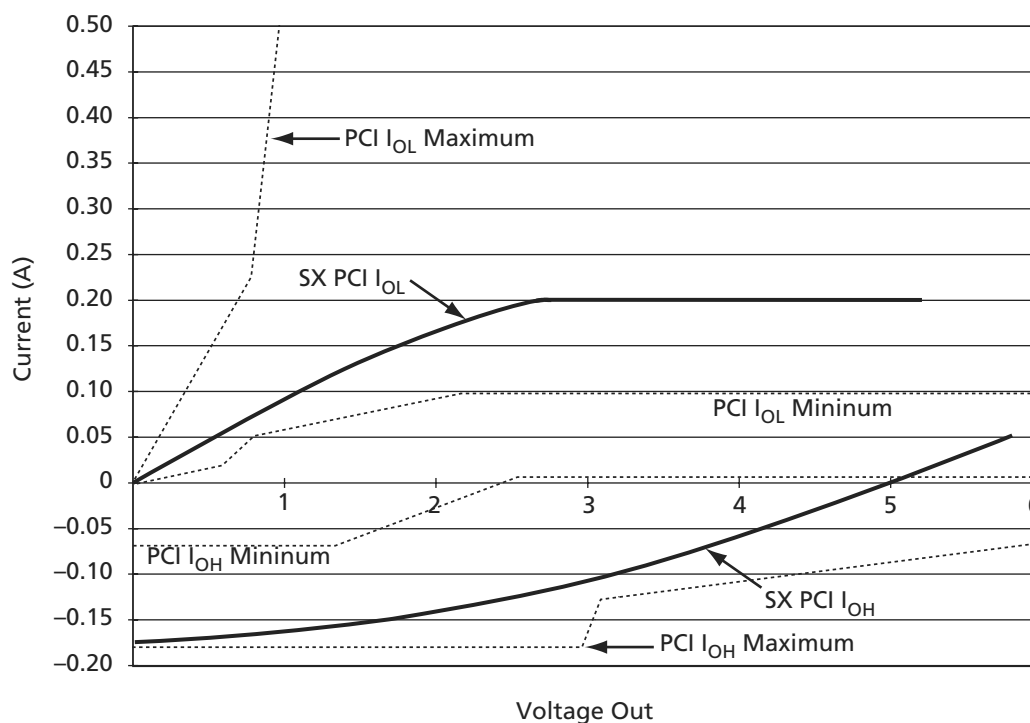


Figure 1-9 • **5.0 V PCI Curve for A54SX16P Device**

$$I_{OH} = 11.9 \times (V_{OUT} - 5.25) \times (V_{OUT} + 2.45)$$

for  $V_{CC} > V_{OUT} > 3.1$  V

EQ 1-1

$$I_{OL} = 78.5 \times V_{OUT} \times (4.4 - V_{OUT})$$

for  $0$  V  $< V_{OUT} < 0.71$  V

EQ 1-2

## A54SX16P DC Specifications (3.3 V PCI Operation)

Table 1-8 • A54SX16P DC Specifications (3.3 V PCI Operation)

| Symbol      | Parameter                                    | Condition              | Min.        | Max.           | Units   |
|-------------|----------------------------------------------|------------------------|-------------|----------------|---------|
| $V_{CCA}$   | Supply Voltage for Array                     |                        | 3.0         | 3.6            | V       |
| $V_{CCR}$   | Supply Voltage required for Internal Biasing |                        | 3.0         | 3.6            | V       |
| $V_{CCI}$   | Supply Voltage for I/Os                      |                        | 3.0         | 3.6            | V       |
| $V_{IH}$    | Input High Voltage                           |                        | $0.5V_{CC}$ | $V_{CC} + 0.5$ | V       |
| $V_{IL}$    | Input Low Voltage                            |                        | -0.5        | $0.3V_{CC}$    | V       |
| $I_{PU}$    | Input Pull-up Voltage <sup>1</sup>           |                        | $0.7V_{CC}$ |                | V       |
| $I_{IL}$    | Input Leakage Current <sup>2</sup>           | $0 < V_{IN} < V_{CC}$  |             | $\pm 10$       | $\mu A$ |
| $V_{OH}$    | Output High Voltage                          | $I_{OUT} = -500 \mu A$ | $0.9V_{CC}$ |                | V       |
| $V_{OL}$    | Output Low Voltage                           | $I_{OUT} = 1500 \mu A$ |             | $0.1V_{CC}$    | V       |
| $C_{IN}$    | Input Pin Capacitance <sup>3</sup>           |                        |             | 10             | pF      |
| $C_{CLK}$   | CLK Pin Capacitance                          |                        | 5           | 12             | pF      |
| $C_{IDSEL}$ | IDSEL Pin Capacitance <sup>4</sup>           |                        |             | 8              | pF      |

### Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

## Power-Up Sequencing

Table 1-10 • Power-Up Sequencing

| V <sub>CCA</sub>          | V <sub>CCR</sub> | V <sub>CCI</sub> | Power-Up Sequence           | Comments                     |
|---------------------------|------------------|------------------|-----------------------------|------------------------------|
| A54SX08, A54SX16, A54SX32 |                  |                  |                             |                              |
| 3.3 V                     | 5.0 V            | 3.3 V            | 5.0 V First<br>3.3 V Second | No possible damage to device |
|                           |                  |                  | 3.3 V First<br>5.0 V Second | Possible damage to device    |
| A54SX16P                  |                  |                  |                             |                              |
| 3.3 V                     | 3.3 V            | 3.3 V            | 3.3 V Only                  | No possible damage to device |
| 3.3 V                     | 5.0 V            | 3.3 V            | 5.0 V First<br>3.3 V Second | No possible damage to device |
|                           |                  |                  | 3.3 V First<br>5.0 V Second | Possible damage to device    |
| 3.3 V                     | 5.0 V            | 5.0 V            | 5.0 V First<br>3.3 V Second | No possible damage to device |
|                           |                  |                  | 3.3 V First<br>5.0 V Second | No possible damage to device |

**Note:** No inputs should be driven (high or low) before completion of power-up.

## Power-Down Sequencing

Table 1-11 • Power-Down Sequencing

| V <sub>CCA</sub>          | V <sub>CCR</sub> | V <sub>CCI</sub> | Power-Down Sequence         | Comments                     |
|---------------------------|------------------|------------------|-----------------------------|------------------------------|
| A54SX08, A54SX16, A54SX32 |                  |                  |                             |                              |
| 3.3 V                     | 5.0 V            | 3.3 V            | 5.0 V First<br>3.3 V Second | Possible damage to device    |
|                           |                  |                  | 3.3 V First<br>5.0 V Second | No possible damage to device |
| A54SX16P                  |                  |                  |                             |                              |
| 3.3 V                     | 3.3 V            | 3.3 V            | 3.3 V Only                  | No possible damage to device |
| 3.3 V                     | 5.0 V            | 3.3 V            | 5.0 V First<br>3.3 V Second | Possible damage to device    |
|                           |                  |                  | 3.3 V First<br>5.0 V Second | No possible damage to device |
| 3.3 V                     | 5.0 V            | 5.0 V            | 5.0 V First<br>3.3 V Second | No possible damage to device |
|                           |                  |                  | 3.3 V First<br>5.0 V Second | No possible damage to device |

**Note:** No inputs should be driven (high or low) after the beginning of the power-down sequence.

**Step 1: Define Terms Used in Formula**

|                                                                         |            |           |
|-------------------------------------------------------------------------|------------|-----------|
| <b>Module</b>                                                           | $V_{CCA}$  | 3.3       |
| Number of logic modules switching at $f_m$ (Used 50%)                   | $m$        | 264       |
| Average logic modules switching rate $f_m$ (MHz) (Guidelines: $f/10$ )  | $f_m$      | 20        |
| Module capacitance $C_{EQM}$ (pF)                                       | $C_{EQM}$  | 4.0       |
| <b>Input Buffer</b>                                                     |            |           |
| Number of input buffers switching at $f_n$                              | $n$        | 1         |
| Average input switching rate $f_n$ (MHz) (Guidelines: $f/5$ )           | $f_n$      | 40        |
| Input buffer capacitance $C_{EQI}$ (pF)                                 | $C_{EQI}$  | 3.4       |
| <b>Output Buffer</b>                                                    |            |           |
| Number of output buffers switching at $f_p$                             | $p$        | 1         |
| Average output buffers switching rate $f_p$ (MHz) (Guidelines: $f/10$ ) | $f_p$      | 20        |
| Output buffers buffer capacitance $C_{EQO}$ (pF)                        | $C_{EQO}$  | 4.7       |
| Output Load capacitance $C_L$ (pF)                                      | $C_L$      | 35        |
| <b>RCLKA</b>                                                            |            |           |
| Number of Clock loads $q_1$                                             | $q_1$      | 528       |
| Capacitance of routed array clock (pF)                                  | $C_{EQCR}$ | 1.6       |
| Average clock rate (MHz)                                                | $f_{q1}$   | 200       |
| Fixed capacitance (pF)                                                  | $r_1$      | 138       |
| <b>RCLKB</b>                                                            |            |           |
| Number of Clock loads $q_2$                                             | $q_2$      | 0         |
| Capacitance of routed array clock (pF)                                  | $C_{EQCR}$ | 1.6       |
| Average clock rate (MHz)                                                | $f_{q2}$   | 0         |
| Fixed capacitance (pF)                                                  | $r_2$      | 138       |
| <b>HCLK</b>                                                             |            |           |
| Number of Clock loads                                                   | $s_1$      | 0         |
| Variable capacitance of dedicated array clock (pF)                      | $C_{EQHV}$ | 0.61<br>5 |
| Fixed capacitance of dedicated array clock (pF)                         | $C_{EQHF}$ | 96        |
| Average clock rate (MHz)                                                | $f_{s1}$   | 0         |

**Step 2: Calculate Dynamic Power Consumption**

|                                                                      |          |
|----------------------------------------------------------------------|----------|
| $V_{CCA} \times V_{CCA}$                                             | 10.89    |
| $m \times f_m \times C_{EQM}$                                        | 0.02112  |
| $n \times f_n \times C_{EQI}$                                        | 0.000136 |
| $p \times f_p \times (C_{EQO} + C_L)$                                | 0.000794 |
| $0.5 (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1})$      | 0.11208  |
| $0.5 (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2})$      | 0        |
| $0.5 (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1})$ | 0        |
| $P_{AC} = 1.461 \text{ W}$                                           |          |

**Step 3: Calculate DC Power Dissipation****DC Power Dissipation**

$$P_{DC} = (I_{\text{standby}}) \times V_{CCA} + (I_{\text{standby}}) \times V_{CCR} + (I_{\text{standby}}) \times V_{CCI} + X \times V_{OL} \times I_{OL} + Y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-12

For a rough estimate of DC Power Dissipation, only use  $P_{DC} = (I_{\text{standby}}) \times V_{CCA}$ . The rest of the formula provides a very small number that can be considered negligible.

$$P_{DC} = (I_{\text{standby}}) \times V_{CCA}$$

$$P_{DC} = .55 \text{ mA} \times 3.3 \text{ V}$$

$$P_{DC} = 0.001815 \text{ W}$$

**Step 4: Calculate Total Power Consumption**

$$P_{\text{Total}} = P_{AC} + P_{DC}$$

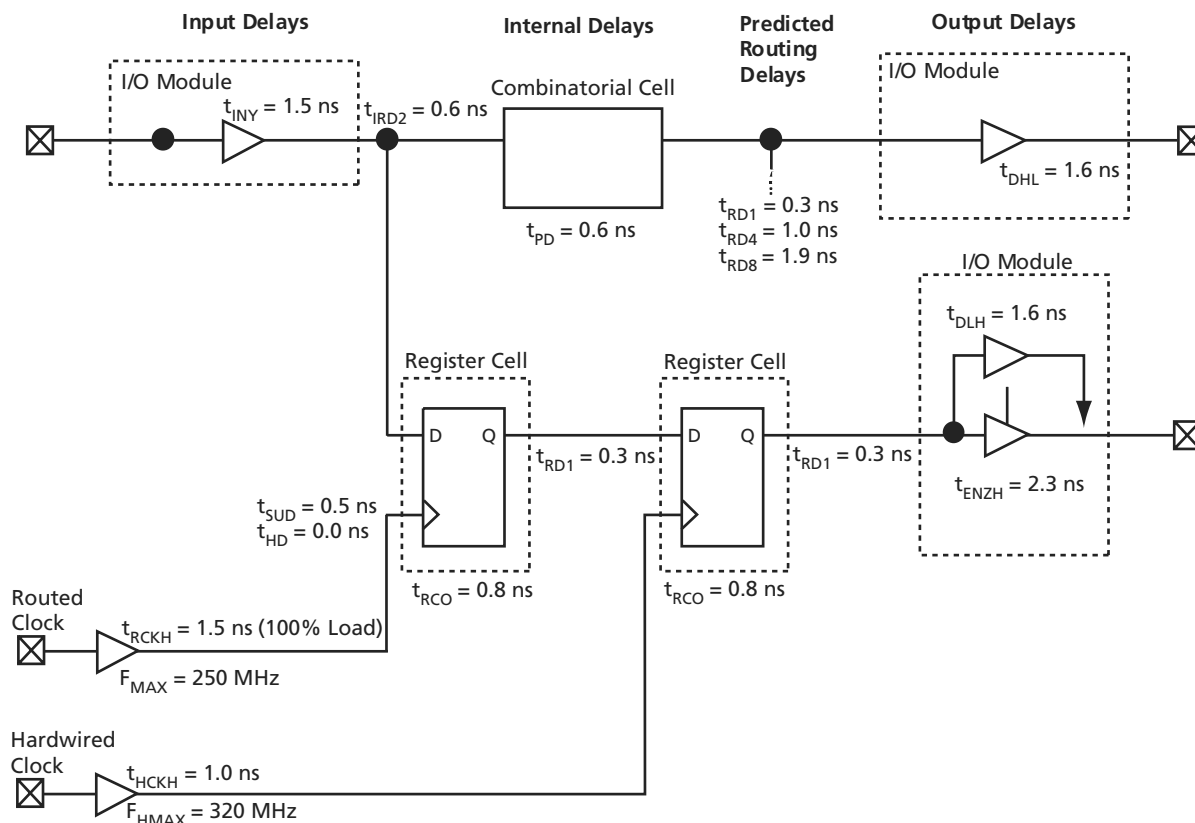
$$P_{\text{Total}} = 1.461 + 0.001815$$

$$P_{\text{Total}} = 1.4628 \text{ W}$$

**Step 5: Compare Estimated Power Consumption against Characterized Power Consumption**

The estimated total power consumption for this design is 1.46 W. The characterized power consumption for this design at 200 MHz is 1.0164 W.

# SX Timing Model



**Note:** Values shown for A54SX08-3, worst-case commercial conditions.

Figure 1-12 • SX Timing Model

## Hardwired Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.0 = 1.3 \text{ ns} \end{aligned}$$

EQ 1-15

## Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.0 + 0.8 + 0.3 + 1.6 = 3.7 \text{ ns} \end{aligned}$$

EQ 1-16

## Routed Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.5 = 0.8 \text{ ns} \end{aligned}$$

EQ 1-17

## Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.52 + 0.8 + 0.3 + 1.6 = 4.2 \text{ ns} \end{aligned}$$

EQ 1-18

## A54SX08 Timing Characteristics

Table 1-17 • A54SX08 Timing Characteristics  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

| Parameter                                          | Description                          | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      |    |
|----------------------------------------------------|--------------------------------------|------------|------|------------|------|------------|------|-------------|------|----|
|                                                    |                                      | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. |    |
| C-Cell Propagation Delays <sup>1</sup>             |                                      |            |      |            |      |            |      |             |      |    |
| t <sub>PD</sub>                                    | Internal Array Module                | 0.6        |      | 0.7        |      | 0.8        |      | 0.9         |      | ns |
| Predicted Routing Delays <sup>2</sup>              |                                      |            |      |            |      |            |      |             |      |    |
| t <sub>DC</sub>                                    | FO = 1 Routing Delay, Direct Connect | 0.1        |      | 0.1        |      | 0.1        |      | 0.1         |      | ns |
| t <sub>FC</sub>                                    | FO = 1 Routing Delay, Fast Connect   | 0.3        |      | 0.4        |      | 0.4        |      | 0.5         |      | ns |
| t <sub>RD1</sub>                                   | FO = 1 Routing Delay                 | 0.3        |      | 0.4        |      | 0.4        |      | 0.5         |      | ns |
| t <sub>RD2</sub>                                   | FO = 2 Routing Delay                 | 0.6        |      | 0.7        |      | 0.8        |      | 0.9         |      | ns |
| t <sub>RD3</sub>                                   | FO = 3 Routing Delay                 | 0.8        |      | 0.9        |      | 1.0        |      | 1.2         |      | ns |
| t <sub>RD4</sub>                                   | FO = 4 Routing Delay                 | 1.0        |      | 1.2        |      | 1.4        |      | 1.6         |      | ns |
| t <sub>RD8</sub>                                   | FO = 8 Routing Delay                 | 1.9        |      | 2.2        |      | 2.5        |      | 2.9         |      | ns |
| t <sub>RD12</sub>                                  | FO = 12 Routing Delay                | 2.8        |      | 3.2        |      | 3.7        |      | 4.3         |      | ns |
| R-Cell Timing                                      |                                      |            |      |            |      |            |      |             |      |    |
| t <sub>RCO</sub>                                   | Sequential Clock-to-Q                | 0.8        |      | 1.1        |      | 1.2        |      | 1.4         |      | ns |
| t <sub>CLR</sub>                                   | Asynchronous Clear-to-Q              | 0.5        |      | 0.6        |      | 0.7        |      | 0.8         |      | ns |
| t <sub>PRESET</sub>                                | Asynchronous Preset-to-Q             | 0.7        |      | 0.8        |      | 0.9        |      | 1.0         |      | ns |
| t <sub>SUD</sub>                                   | Flip-Flop Data Input Set-Up          | 0.5        |      | 0.5        |      | 0.7        |      | 0.8         |      | ns |
| t <sub>HD</sub>                                    | Flip-Flop Data Input Hold            | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | ns |
| t <sub>WASYN</sub>                                 | Asynchronous Pulse Width             | 1.4        |      | 1.6        |      | 1.8        |      | 2.1         |      | ns |
| Input Module Propagation Delays                    |                                      |            |      |            |      |            |      |             |      |    |
| t <sub>INYH</sub>                                  | Input Data Pad-to-Y HIGH             | 1.5        |      | 1.7        |      | 1.9        |      | 2.2         |      | ns |
| t <sub>INYL</sub>                                  | Input Data Pad-to-Y LOW              | 1.5        |      | 1.7        |      | 1.9        |      | 2.2         |      | ns |
| Input Module Predicted Routing Delays <sup>2</sup> |                                      |            |      |            |      |            |      |             |      |    |
| t <sub>IRD1</sub>                                  | FO = 1 Routing Delay                 | 0.3        |      | 0.4        |      | 0.4        |      | 0.5         |      | ns |
| t <sub>IRD2</sub>                                  | FO = 2 Routing Delay                 | 0.6        |      | 0.7        |      | 0.8        |      | 0.9         |      | ns |
| t <sub>IRD3</sub>                                  | FO = 3 Routing Delay                 | 0.8        |      | 0.9        |      | 1.0        |      | 1.2         |      | ns |
| t <sub>IRD4</sub>                                  | FO = 4 Routing Delay                 | 1.0        |      | 1.2        |      | 1.4        |      | 1.6         |      | ns |
| t <sub>IRD8</sub>                                  | FO = 8 Routing Delay                 | 1.9        |      | 2.2        |      | 2.5        |      | 2.9         |      | ns |
| t <sub>IRD12</sub>                                 | FO = 12 Routing Delay                | 2.8        |      | 3.2        |      | 3.7        |      | 4.3         |      | ns |

**Note:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**Table 1-18 • A54SX16 Timing Characteristics (Continued)**  
**(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

| Parameter                                 | Description                                             | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | Units |
|-------------------------------------------|---------------------------------------------------------|------------|------|------------|------|------------|------|-------------|------|-------|
|                                           |                                                         | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. |       |
| Dedicated (Hardwired) Array Clock Network |                                                         |            |      |            |      |            |      |             |      |       |
| t <sub>HCKH</sub>                         | Input LOW to HIGH (pad to R-Cell input)                 | 1.2        |      | 1.4        |      | 1.5        |      | 1.8         |      | ns    |
| t <sub>HCKL</sub>                         | Input HIGH to LOW (pad to R-Cell input)                 | 1.2        |      | 1.4        |      | 1.6        |      | 1.9         |      | ns    |
| t <sub>HPWH</sub>                         | Minimum Pulse Width HIGH                                | 1.4        |      | 1.6        |      | 1.8        |      | 2.1         |      | ns    |
| t <sub>HPWL</sub>                         | Minimum Pulse Width LOW                                 | 1.4        |      | 1.6        |      | 1.8        |      | 2.1         |      | ns    |
| t <sub>HCKSW</sub>                        | Maximum Skew                                            | 0.2        |      | 0.2        |      | 0.3        |      | 0.3         |      | ns    |
| t <sub>HP</sub>                           | Minimum Period                                          | 2.7        |      | 3.1        |      | 3.6        |      | 4.2         |      | ns    |
| f <sub>HMAX</sub>                         | Maximum Frequency                                       | 350        |      | 320        |      | 280        |      | 240         |      | MHz   |
| Routed Array Clock Networks               |                                                         |            |      |            |      |            |      |             |      |       |
| t <sub>RCKH</sub>                         | Input LOW to HIGH (light load)<br>(pad to R-Cell input) | 1.6        |      | 1.8        |      | 2.1        |      | 2.5         |      | ns    |
| t <sub>RCKL</sub>                         | Input HIGH to LOW (light load)<br>(pad to R-Cell input) | 1.8        |      | 2.0        |      | 2.3        |      | 2.7         |      | ns    |
| t <sub>RCKH</sub>                         | Input LOW to HIGH (50% load)<br>(pad to R-Cell input)   | 1.8        |      | 2.1        |      | 2.5        |      | 2.8         |      | ns    |
| t <sub>RCKL</sub>                         | Input HIGH to LOW (50% load)<br>(pad to R-Cell input)   | 2.0        |      | 2.2        |      | 2.5        |      | 3.0         |      | ns    |
| t <sub>RCKH</sub>                         | Input LOW to HIGH (100% load)<br>(pad to R-Cell input)  | 1.8        |      | 2.1        |      | 2.4        |      | 2.8         |      | ns    |
| t <sub>RCKL</sub>                         | Input HIGH to LOW (100% load)<br>(pad to R-Cell input)  | 2.0        |      | 2.2        |      | 2.5        |      | 3.0         |      | ns    |
| t <sub>RPWH</sub>                         | Min. Pulse Width HIGH                                   | 2.1        |      | 2.4        |      | 2.7        |      | 3.2         |      | ns    |
| t <sub>RPWL</sub>                         | Min. Pulse Width LOW                                    | 2.1        |      | 2.4        |      | 2.7        |      | 3.2         |      | ns    |
| t <sub>RCKSW</sub>                        | Maximum Skew (light load)                               | 0.5        |      | 0.5        |      | 0.5        |      | 0.7         |      | ns    |
| t <sub>RCKSW</sub>                        | Maximum Skew (50% load)                                 | 0.5        |      | 0.6        |      | 0.7        |      | 0.8         |      | ns    |
| t <sub>RCKSW</sub>                        | Maximum Skew (100% load)                                | 0.5        |      | 0.6        |      | 0.7        |      | 0.8         |      | ns    |
| TTL Output Module Timing <sup>3</sup>     |                                                         |            |      |            |      |            |      |             |      |       |
| t <sub>DLH</sub>                          | Data-to-Pad LOW to HIGH                                 | 1.6        |      | 1.9        |      | 2.1        |      | 2.5         |      | ns    |
| t <sub>DHL</sub>                          | Data-to-Pad HIGH to LOW                                 | 1.6        |      | 1.9        |      | 2.1        |      | 2.5         |      | ns    |
| t <sub>ENZL</sub>                         | Enable-to-Pad, Z to L                                   | 2.1        |      | 2.4        |      | 2.8        |      | 3.2         |      | ns    |
| t <sub>ENZH</sub>                         | Enable-to-Pad, Z to H                                   | 2.3        |      | 2.7        |      | 3.1        |      | 3.6         |      | ns    |
| t <sub>ENLZ</sub>                         | Enable-to-Pad, L to Z                                   | 1.4        |      | 1.7        |      | 1.9        |      | 2.2         |      | ns    |
| t <sub>ENHZ</sub>                         | Enable-to-Pad, H to Z                                   | 1.3        |      | 1.5        |      | 1.7        |      | 2.0         |      | ns    |

**Notes:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except  $t_{ENZL}$  and  $t_{ENZH}$ . For  $t_{ENZL}$  and  $t_{ENZH}$ , the loading is 5 pF.

Table 1-19 • A54SX16P Timing Characteristics (Continued)

(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

| Parameter                                 | Description                                             | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | Units |
|-------------------------------------------|---------------------------------------------------------|------------|------|------------|------|------------|------|-------------|------|-------|
|                                           |                                                         | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. |       |
| Dedicated (Hardwired) Array Clock Network |                                                         |            |      |            |      |            |      |             |      |       |
| t <sub>HCKH</sub>                         | Input LOW to HIGH (pad to R-Cell input)                 | 1.2        |      | 1.4        |      | 1.5        |      | 1.8         |      | ns    |
| t <sub>HCKL</sub>                         | Input HIGH to LOW (pad to R-Cell input)                 | 1.2        |      | 1.4        |      | 1.6        |      | 1.9         |      | ns    |
| t <sub>HPWH</sub>                         | Minimum Pulse Width HIGH                                | 1.4        |      | 1.6        |      | 1.8        |      | 2.1         |      | ns    |
| t <sub>HPWL</sub>                         | Minimum Pulse Width LOW                                 | 1.4        |      | 1.6        |      | 1.8        |      | 2.1         |      | ns    |
| t <sub>HCKSW</sub>                        | Maximum Skew                                            | 0.2        |      | 0.2        |      | 0.3        |      | 0.3         |      | ns    |
| t <sub>HP</sub>                           | Minimum Period                                          | 2.7        |      | 3.1        |      | 3.6        |      | 4.2         |      | ns    |
| f <sub>HMAX</sub>                         | Maximum Frequency                                       | 350        |      | 320        |      | 280        |      | 240         |      | MHz   |
| Routed Array Clock Networks               |                                                         |            |      |            |      |            |      |             |      |       |
| t <sub>RCKH</sub>                         | Input LOW to HIGH (light load)<br>(pad to R-Cell input) | 1.6        |      | 1.8        |      | 2.1        |      | 2.5         |      | ns    |
| t <sub>RCKL</sub>                         | Input HIGH to LOW (Light Load)<br>(pad to R-Cell input) | 1.8        |      | 2.0        |      | 2.3        |      | 2.7         |      | ns    |
| t <sub>RCKH</sub>                         | Input LOW to HIGH (50% load)<br>(pad to R-Cell input)   | 1.8        |      | 2.1        |      | 2.5        |      | 2.8         |      | ns    |
| t <sub>RCKL</sub>                         | Input HIGH to LOW (50% load)<br>(pad to R-Cell input)   | 2.0        |      | 2.2        |      | 2.5        |      | 3.0         |      | ns    |
| t <sub>RCKH</sub>                         | Input LOW to HIGH (100% load)<br>(pad to R-Cell input)  | 1.8        |      | 2.1        |      | 2.4        |      | 2.8         |      | ns    |
| t <sub>RCKL</sub>                         | Input HIGH to LOW (100% load)<br>(pad to R-Cell input)  | 2.0        |      | 2.2        |      | 2.5        |      | 3.0         |      | ns    |
| t <sub>RPWH</sub>                         | Min. Pulse Width HIGH                                   | 2.1        |      | 2.4        |      | 2.7        |      | 3.2         |      | ns    |
| t <sub>RPWL</sub>                         | Min. Pulse Width LOW                                    | 2.1        |      | 2.4        |      | 2.7        |      | 3.2         |      | ns    |
| t <sub>RCKSW</sub>                        | Maximum Skew (light load)                               | 0.5        |      | 0.5        |      | 0.5        |      | 0.7         |      | ns    |
| t <sub>RCKSW</sub>                        | Maximum Skew (50% load)                                 | 0.5        |      | 0.6        |      | 0.7        |      | 0.8         |      | ns    |
| t <sub>RCKSW</sub>                        | Maximum Skew (100% load)                                | 0.5        |      | 0.6        |      | 0.7        |      | 0.8         |      | ns    |
| TTL Output Module Timing                  |                                                         |            |      |            |      |            |      |             |      |       |
| t <sub>DLH</sub>                          | Data-to-Pad LOW to HIGH                                 | 2.4        |      | 2.8        |      | 3.1        |      | 3.7         |      | ns    |
| t <sub>DHL</sub>                          | Data-to-Pad HIGH to LOW                                 | 2.3        |      | 2.9        |      | 3.2        |      | 3.8         |      | ns    |
| t <sub>ENZL</sub>                         | Enable-to-Pad, Z to L                                   | 3.0        |      | 3.4        |      | 3.9        |      | 4.6         |      | ns    |
| t <sub>ENZH</sub>                         | Enable-to-Pad, Z to H                                   | 3.3        |      | 3.8        |      | 4.3        |      | 5.0         |      | ns    |
| t <sub>ENLZ</sub>                         | Enable-to-Pad, L to Z                                   | 2.3        |      | 2.7        |      | 3.0        |      | 3.5         |      | ns    |
| t <sub>ENHZ</sub>                         | Enable-to-Pad, H to Z                                   | 2.8        |      | 3.2        |      | 3.7        |      | 4.3         |      | ns    |

**Note:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 10 pF loading.

Table 1-19 • A54SX16P Timing Characteristics (Continued)

(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

| Parameter                             | Description             | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | Units |
|---------------------------------------|-------------------------|------------|------|------------|------|------------|------|-------------|------|-------|
|                                       |                         | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. |       |
| TTL/PCI Output Module Timing          |                         |            |      |            |      |            |      |             |      |       |
| t <sub>DLH</sub>                      | Data-to-Pad LOW to HIGH | 1.5        |      | 1.7        |      | 2.0        |      | 2.3         |      | ns    |
| t <sub>DHL</sub>                      | Data-to-Pad HIGH to LOW | 1.9        |      | 2.2        |      | 2.4        |      | 2.9         |      | ns    |
| t <sub>ENZL</sub>                     | Enable-to-Pad, Z to L   | 2.3        |      | 2.6        |      | 3.0        |      | 3.5         |      | ns    |
| t <sub>ENZH</sub>                     | Enable-to-Pad, Z to H   | 1.5        |      | 1.7        |      | 1.9        |      | 2.3         |      | ns    |
| t <sub>ENLZ</sub>                     | Enable-to-Pad, L to Z   | 2.7        |      | 3.1        |      | 3.5        |      | 4.1         |      | ns    |
| t <sub>ENHZ</sub>                     | Enable-to-Pad, H to Z   | 2.9        |      | 3.3        |      | 3.7        |      | 4.4         |      | ns    |
| PCI Output Module Timing <sup>3</sup> |                         |            |      |            |      |            |      |             |      |       |
| t <sub>DLH</sub>                      | Data-to-Pad LOW to HIGH | 1.8        |      | 2.0        |      | 2.3        |      | 2.7         |      | ns    |
| t <sub>DHL</sub>                      | Data-to-Pad HIGH to LOW | 1.7        |      | 2.0        |      | 2.2        |      | 2.6         |      | ns    |
| t <sub>ENZL</sub>                     | Enable-to-Pad, Z to L   | 0.8        |      | 1.0        |      | 1.1        |      | 1.3         |      | ns    |
| t <sub>ENZH</sub>                     | Enable-to-Pad, Z to H   | 1.2        |      | 1.2        |      | 1.5        |      | 1.8         |      | ns    |
| t <sub>ENLZ</sub>                     | Enable-to-Pad, L to Z   | 1.0        |      | 1.1        |      | 1.3        |      | 1.5         |      | ns    |
| t <sub>ENHZ</sub>                     | Enable-to-Pad, H to Z   | 1.1        |      | 1.3        |      | 1.5        |      | 1.7         |      | ns    |
| TTL Output Module Timing              |                         |            |      |            |      |            |      |             |      |       |
| t <sub>DLH</sub>                      | Data-to-Pad LOW to HIGH | 2.1        |      | 2.5        |      | 2.8        |      | 3.3         |      | ns    |
| t <sub>DHL</sub>                      | Data-to-Pad HIGH to LOW | 2.0        |      | 2.3        |      | 2.6        |      | 3.1         |      | ns    |
| t <sub>ENZL</sub>                     | Enable-to-Pad, Z to L   | 2.5        |      | 2.9        |      | 3.2        |      | 3.8         |      | ns    |
| t <sub>ENZH</sub>                     | Enable-to-Pad, Z to H   | 3.0        |      | 3.5        |      | 3.9        |      | 4.6         |      | ns    |
| t <sub>ENLZ</sub>                     | Enable-to-Pad, L to Z   | 2.3        |      | 2.7        |      | 3.1        |      | 3.6         |      | ns    |
| t <sub>ENHZ</sub>                     | Enable-to-Pad, H to Z   | 2.9        |      | 3.3        |      | 3.7        |      | 4.4         |      | ns    |

**Note:**

1. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 10 pF loading.

| 208-Pin PQFP |                     |                                  |                     |
|--------------|---------------------|----------------------------------|---------------------|
| Pin Number   | A54SX08<br>Function | A54SX16,<br>A54SX16P<br>Function | A54SX32<br>Function |
| 1            | GND                 | GND                              | GND                 |
| 2            | TDI, I/O            | TDI, I/O                         | TDI, I/O            |
| 3            | I/O                 | I/O                              | I/O                 |
| 4            | NC                  | I/O                              | I/O                 |
| 5            | I/O                 | I/O                              | I/O                 |
| 6            | NC                  | I/O                              | I/O                 |
| 7            | I/O                 | I/O                              | I/O                 |
| 8            | I/O                 | I/O                              | I/O                 |
| 9            | I/O                 | I/O                              | I/O                 |
| 10           | I/O                 | I/O                              | I/O                 |
| 11           | TMS                 | TMS                              | TMS                 |
| 12           | V <sub>CCI</sub>    | V <sub>CCI</sub>                 | V <sub>CCI</sub>    |
| 13           | I/O                 | I/O                              | I/O                 |
| 14           | NC                  | I/O                              | I/O                 |
| 15           | I/O                 | I/O                              | I/O                 |
| 16           | I/O                 | I/O                              | I/O                 |
| 17           | NC                  | I/O                              | I/O                 |
| 18           | I/O                 | I/O                              | I/O                 |
| 19           | I/O                 | I/O                              | I/O                 |
| 20           | NC                  | I/O                              | I/O                 |
| 21           | I/O                 | I/O                              | I/O                 |
| 22           | I/O                 | I/O                              | I/O                 |
| 23           | NC                  | I/O                              | I/O                 |
| 24           | I/O                 | I/O                              | I/O                 |
| 25           | V <sub>CCR</sub>    | V <sub>CCR</sub>                 | V <sub>CCR</sub>    |
| 26           | GND                 | GND                              | GND                 |
| 27           | V <sub>CCA</sub>    | V <sub>CCA</sub>                 | V <sub>CCA</sub>    |
| 28           | GND                 | GND                              | GND                 |
| 29           | I/O                 | I/O                              | I/O                 |
| 30           | I/O                 | I/O                              | I/O                 |
| 31           | NC                  | I/O                              | I/O                 |
| 32           | I/O                 | I/O                              | I/O                 |
| 33           | I/O                 | I/O                              | I/O                 |
| 34           | I/O                 | I/O                              | I/O                 |
| 35           | NC                  | I/O                              | I/O                 |
| 36           | I/O                 | I/O                              | I/O                 |

| 208-Pin PQFP |                     |                                  |                     |
|--------------|---------------------|----------------------------------|---------------------|
| Pin Number   | A54SX08<br>Function | A54SX16,<br>A54SX16P<br>Function | A54SX32<br>Function |
| 37           | I/O                 | I/O                              | I/O                 |
| 38           | I/O                 | I/O                              | I/O                 |
| 39           | NC                  | I/O                              | I/O                 |
| 40           | V <sub>CCI</sub>    | V <sub>CCI</sub>                 | V <sub>CCI</sub>    |
| 41           | V <sub>CCA</sub>    | V <sub>CCA</sub>                 | V <sub>CCA</sub>    |
| 42           | I/O                 | I/O                              | I/O                 |
| 43           | I/O                 | I/O                              | I/O                 |
| 44           | I/O                 | I/O                              | I/O                 |
| 45           | I/O                 | I/O                              | I/O                 |
| 46           | I/O                 | I/O                              | I/O                 |
| 47           | I/O                 | I/O                              | I/O                 |
| 48           | NC                  | I/O                              | I/O                 |
| 49           | I/O                 | I/O                              | I/O                 |
| 50           | NC                  | I/O                              | I/O                 |
| 51           | I/O                 | I/O                              | I/O                 |
| 52           | GND                 | GND                              | GND                 |
| 53           | I/O                 | I/O                              | I/O                 |
| 54           | I/O                 | I/O                              | I/O                 |
| 55           | I/O                 | I/O                              | I/O                 |
| 56           | I/O                 | I/O                              | I/O                 |
| 57           | I/O                 | I/O                              | I/O                 |
| 58           | I/O                 | I/O                              | I/O                 |
| 59           | I/O                 | I/O                              | I/O                 |
| 60           | V <sub>CCI</sub>    | V <sub>CCI</sub>                 | V <sub>CCI</sub>    |
| 61           | NC                  | I/O                              | I/O                 |
| 62           | I/O                 | I/O                              | I/O                 |
| 63           | I/O                 | I/O                              | I/O                 |
| 64           | NC                  | I/O                              | I/O                 |
| 65*          | I/O                 | I/O                              | NC*                 |
| 66           | I/O                 | I/O                              | I/O                 |
| 67           | NC                  | I/O                              | I/O                 |
| 68           | I/O                 | I/O                              | I/O                 |
| 69           | I/O                 | I/O                              | I/O                 |
| 70           | NC                  | I/O                              | I/O                 |
| 71           | I/O                 | I/O                              | I/O                 |
| 72           | I/O                 | I/O                              | I/O                 |

**Note:** \* Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

| 208-Pin PQFP |                  |                            |                  |
|--------------|------------------|----------------------------|------------------|
| Pin Number   | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 73           | NC               | I/O                        | I/O              |
| 74           | I/O              | I/O                        | I/O              |
| 75           | NC               | I/O                        | I/O              |
| 76           | PRB, I/O         | PRB, I/O                   | PRB, I/O         |
| 77           | GND              | GND                        | GND              |
| 78           | V <sub>CCA</sub> | V <sub>CCA</sub>           | V <sub>CCA</sub> |
| 79           | GND              | GND                        | GND              |
| 80           | V <sub>CCR</sub> | V <sub>CCR</sub>           | V <sub>CCR</sub> |
| 81           | I/O              | I/O                        | I/O              |
| 82           | HCLK             | HCLK                       | HCLK             |
| 83           | I/O              | I/O                        | I/O              |
| 84           | I/O              | I/O                        | I/O              |
| 85           | NC               | I/O                        | I/O              |
| 86           | I/O              | I/O                        | I/O              |
| 87           | I/O              | I/O                        | I/O              |
| 88           | NC               | I/O                        | I/O              |
| 89           | I/O              | I/O                        | I/O              |
| 90           | I/O              | I/O                        | I/O              |
| 91           | NC               | I/O                        | I/O              |
| 92           | I/O              | I/O                        | I/O              |
| 93           | I/O              | I/O                        | I/O              |
| 94           | NC               | I/O                        | I/O              |
| 95           | I/O              | I/O                        | I/O              |
| 96           | I/O              | I/O                        | I/O              |
| 97           | NC               | I/O                        | I/O              |
| 98           | V <sub>CCI</sub> | V <sub>CCI</sub>           | V <sub>CCI</sub> |
| 99           | I/O              | I/O                        | I/O              |
| 100          | I/O              | I/O                        | I/O              |
| 101          | I/O              | I/O                        | I/O              |
| 102          | I/O              | I/O                        | I/O              |
| 103          | TDO, I/O         | TDO, I/O                   | TDO, I/O         |
| 104          | I/O              | I/O                        | I/O              |
| 105          | GND              | GND                        | GND              |
| 106          | NC               | I/O                        | I/O              |
| 107          | I/O              | I/O                        | I/O              |
| 108          | NC               | I/O                        | I/O              |

| 208-Pin PQFP |                  |                            |                  |
|--------------|------------------|----------------------------|------------------|
| Pin Number   | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 109          | I/O              | I/O                        | I/O              |
| 110          | I/O              | I/O                        | I/O              |
| 111          | I/O              | I/O                        | I/O              |
| 112          | I/O              | I/O                        | I/O              |
| 113          | I/O              | I/O                        | I/O              |
| 114          | V <sub>CCA</sub> | V <sub>CCA</sub>           | V <sub>CCA</sub> |
| 115          | V <sub>CCI</sub> | V <sub>CCI</sub>           | V <sub>CCI</sub> |
| 116          | NC               | I/O                        | I/O              |
| 117          | I/O              | I/O                        | I/O              |
| 118          | I/O              | I/O                        | I/O              |
| 119          | NC               | I/O                        | I/O              |
| 120          | I/O              | I/O                        | I/O              |
| 121          | I/O              | I/O                        | I/O              |
| 122          | NC               | I/O                        | I/O              |
| 123          | I/O              | I/O                        | I/O              |
| 124          | I/O              | I/O                        | I/O              |
| 125          | NC               | I/O                        | I/O              |
| 126          | I/O              | I/O                        | I/O              |
| 127          | I/O              | I/O                        | I/O              |
| 128          | I/O              | I/O                        | I/O              |
| 129          | GND              | GND                        | GND              |
| 130          | V <sub>CCA</sub> | V <sub>CCA</sub>           | V <sub>CCA</sub> |
| 131          | GND              | GND                        | GND              |
| 132          | V <sub>CCR</sub> | V <sub>CCR</sub>           | V <sub>CCR</sub> |
| 133          | I/O              | I/O                        | I/O              |
| 134          | I/O              | I/O                        | I/O              |
| 135          | NC               | I/O                        | I/O              |
| 136          | I/O              | I/O                        | I/O              |
| 137          | I/O              | I/O                        | I/O              |
| 138          | NC               | I/O                        | I/O              |
| 139          | I/O              | I/O                        | I/O              |
| 140          | I/O              | I/O                        | I/O              |
| 141          | NC               | I/O                        | I/O              |
| 142          | I/O              | I/O                        | I/O              |
| 143          | NC               | I/O                        | I/O              |
| 144          | I/O              | I/O                        | I/O              |

**Note:** \* Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

## 144-Pin TQFP

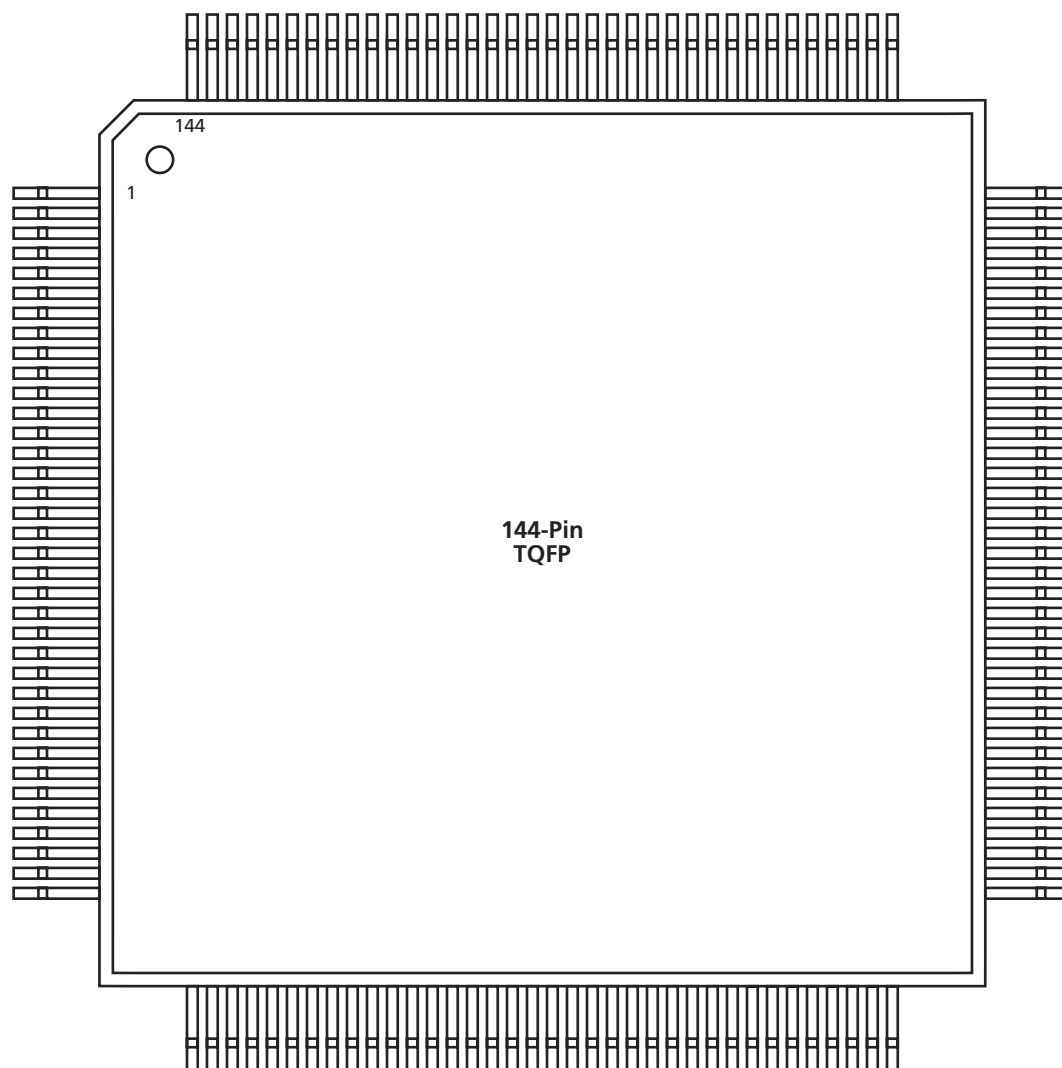


Figure 2-3 • 144-Pin TQFP (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 144-Pin TQFP |                  |                   |                  |
|--------------|------------------|-------------------|------------------|
| Pin Number   | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 73           | GND              | GND               | GND              |
| 74           | I/O              | I/O               | I/O              |
| 75           | I/O              | I/O               | I/O              |
| 76           | I/O              | I/O               | I/O              |
| 77           | I/O              | I/O               | I/O              |
| 78           | I/O              | I/O               | I/O              |
| 79           | V <sub>CCA</sub> | V <sub>CCA</sub>  | V <sub>CCA</sub> |
| 80           | V <sub>CCI</sub> | V <sub>CCI</sub>  | V <sub>CCI</sub> |
| 81           | GND              | GND               | GND              |
| 82           | I/O              | I/O               | I/O              |
| 83           | I/O              | I/O               | I/O              |
| 84           | I/O              | I/O               | I/O              |
| 85           | I/O              | I/O               | I/O              |
| 86           | I/O              | I/O               | I/O              |
| 87           | I/O              | I/O               | I/O              |
| 88           | I/O              | I/O               | I/O              |
| 89           | V <sub>CCA</sub> | V <sub>CCA</sub>  | V <sub>CCA</sub> |
| 90           | V <sub>CCR</sub> | V <sub>CCR</sub>  | V <sub>CCR</sub> |
| 91           | I/O              | I/O               | I/O              |
| 92           | I/O              | I/O               | I/O              |
| 93           | I/O              | I/O               | I/O              |
| 94           | I/O              | I/O               | I/O              |
| 95           | I/O              | I/O               | I/O              |
| 96           | I/O              | I/O               | I/O              |
| 97           | I/O              | I/O               | I/O              |
| 98           | V <sub>CCA</sub> | V <sub>CCA</sub>  | V <sub>CCA</sub> |
| 99           | GND              | GND               | GND              |
| 100          | I/O              | I/O               | I/O              |
| 101          | GND              | GND               | GND              |
| 102          | V <sub>CCI</sub> | V <sub>CCI</sub>  | V <sub>CCI</sub> |
| 103          | I/O              | I/O               | I/O              |
| 104          | I/O              | I/O               | I/O              |
| 105          | I/O              | I/O               | I/O              |
| 106          | I/O              | I/O               | I/O              |
| 107          | I/O              | I/O               | I/O              |
| 108          | I/O              | I/O               | I/O              |

| 144-Pin TQFP |                  |                   |                  |
|--------------|------------------|-------------------|------------------|
| Pin Number   | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 109          | GND              | GND               | GND              |
| 110          | I/O              | I/O               | I/O              |
| 111          | I/O              | I/O               | I/O              |
| 112          | I/O              | I/O               | I/O              |
| 113          | I/O              | I/O               | I/O              |
| 114          | I/O              | I/O               | I/O              |
| 115          | V <sub>CCI</sub> | V <sub>CCI</sub>  | V <sub>CCI</sub> |
| 116          | I/O              | I/O               | I/O              |
| 117          | I/O              | I/O               | I/O              |
| 118          | I/O              | I/O               | I/O              |
| 119          | I/O              | I/O               | I/O              |
| 120          | I/O              | I/O               | I/O              |
| 121          | I/O              | I/O               | I/O              |
| 122          | I/O              | I/O               | I/O              |
| 123          | I/O              | I/O               | I/O              |
| 124          | I/O              | I/O               | I/O              |
| 125          | CLKA             | CLKA              | CLKA             |
| 126          | CLKB             | CLKB              | CLKB             |
| 127          | V <sub>CCR</sub> | V <sub>CCR</sub>  | V <sub>CCR</sub> |
| 128          | GND              | GND               | GND              |
| 129          | V <sub>CCA</sub> | V <sub>CCA</sub>  | V <sub>CCA</sub> |
| 130          | I/O              | I/O               | I/O              |
| 131          | PRA, I/O         | PRA, I/O          | PRA, I/O         |
| 132          | I/O              | I/O               | I/O              |
| 133          | I/O              | I/O               | I/O              |
| 134          | I/O              | I/O               | I/O              |
| 135          | I/O              | I/O               | I/O              |
| 136          | I/O              | I/O               | I/O              |
| 137          | I/O              | I/O               | I/O              |
| 138          | I/O              | I/O               | I/O              |
| 139          | I/O              | I/O               | I/O              |
| 140          | V <sub>CCI</sub> | V <sub>CCI</sub>  | V <sub>CCI</sub> |
| 141          | I/O              | I/O               | I/O              |
| 142          | I/O              | I/O               | I/O              |
| 143          | I/O              | I/O               | I/O              |
| 144          | TCK, I/O         | TCK, I/O          | TCK, I/O         |

## 176-Pin TQFP

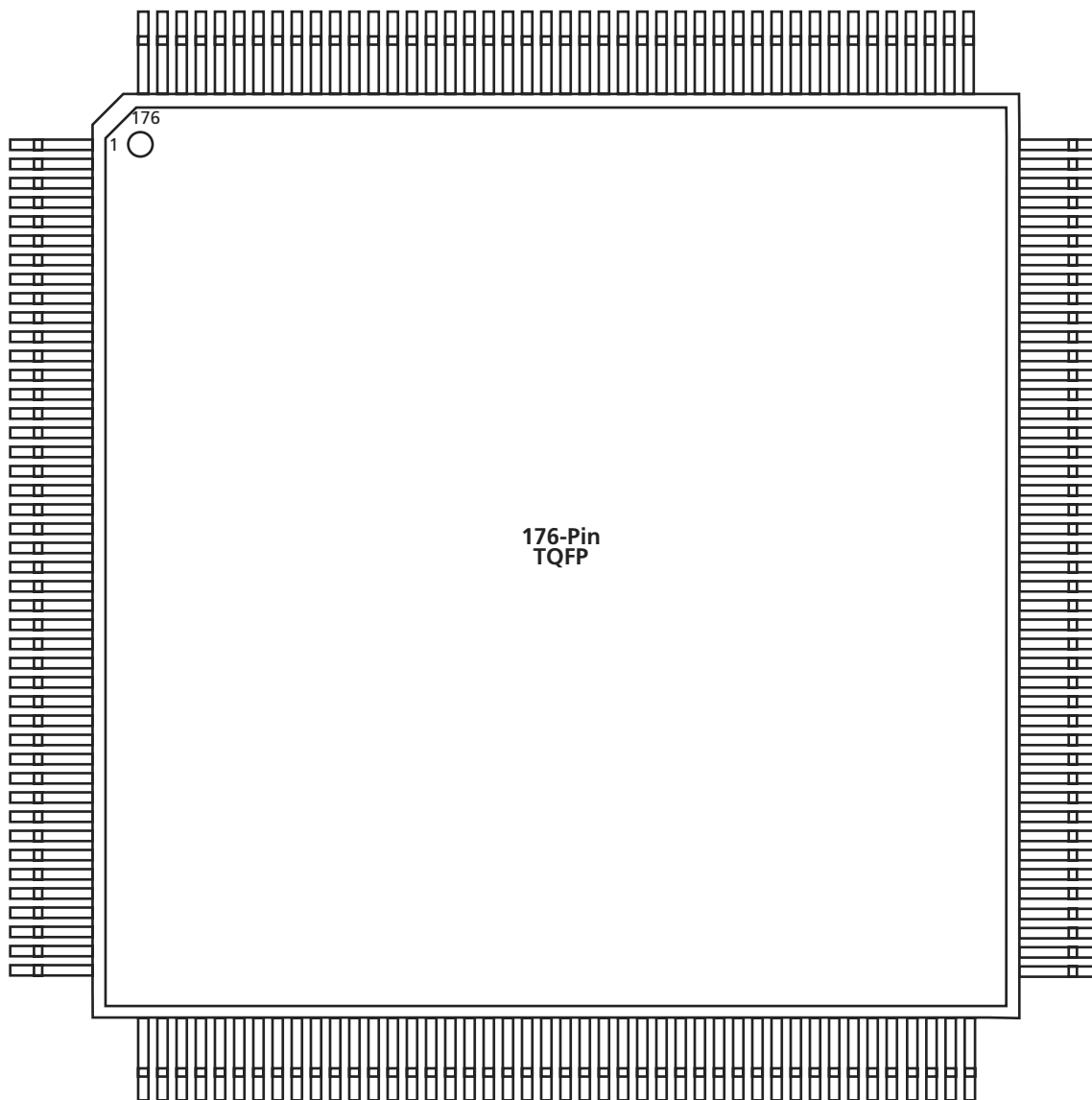


Figure 2-4 • 176-Pin TQFP (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 176-Pin TQFP |                     |                                  |                     |
|--------------|---------------------|----------------------------------|---------------------|
| Pin Number   | A54SX08<br>Function | A54SX16,<br>A54SX16P<br>Function | A54SX32<br>Function |
| 1            | GND                 | GND                              | GND                 |
| 2            | TDI, I/O            | TDI, I/O                         | TDI, I/O            |
| 3            | NC                  | I/O                              | I/O                 |
| 4            | I/O                 | I/O                              | I/O                 |
| 5            | I/O                 | I/O                              | I/O                 |
| 6            | I/O                 | I/O                              | I/O                 |
| 7            | I/O                 | I/O                              | I/O                 |
| 8            | I/O                 | I/O                              | I/O                 |
| 9            | I/O                 | I/O                              | I/O                 |
| 10           | TMS                 | TMS                              | TMS                 |
| 11           | V <sub>CCI</sub>    | V <sub>CCI</sub>                 | V <sub>CCI</sub>    |
| 12           | NC                  | I/O                              | I/O                 |
| 13           | I/O                 | I/O                              | I/O                 |
| 14           | I/O                 | I/O                              | I/O                 |
| 15           | I/O                 | I/O                              | I/O                 |
| 16           | I/O                 | I/O                              | I/O                 |
| 17           | I/O                 | I/O                              | I/O                 |
| 18           | I/O                 | I/O                              | I/O                 |
| 19           | I/O                 | I/O                              | I/O                 |
| 20           | I/O                 | I/O                              | I/O                 |
| 21           | GND                 | GND                              | GND                 |
| 22           | V <sub>CCA</sub>    | V <sub>CCA</sub>                 | V <sub>CCA</sub>    |
| 23           | GND                 | GND                              | GND                 |
| 24           | I/O                 | I/O                              | I/O                 |
| 25           | I/O                 | I/O                              | I/O                 |
| 26           | I/O                 | I/O                              | I/O                 |
| 27           | I/O                 | I/O                              | I/O                 |
| 28           | I/O                 | I/O                              | I/O                 |
| 29           | I/O                 | I/O                              | I/O                 |
| 30           | I/O                 | I/O                              | I/O                 |
| 31           | I/O                 | I/O                              | I/O                 |
| 32           | V <sub>CCI</sub>    | V <sub>CCI</sub>                 | V <sub>CCI</sub>    |
| 33           | V <sub>CCA</sub>    | V <sub>CCA</sub>                 | V <sub>CCA</sub>    |
| 34           | I/O                 | I/O                              | I/O                 |

| 176-Pin TQFP |                     |                                  |                     |
|--------------|---------------------|----------------------------------|---------------------|
| Pin Number   | A54SX08<br>Function | A54SX16,<br>A54SX16P<br>Function | A54SX32<br>Function |
| 35           | I/O                 | I/O                              | I/O                 |
| 36           | I/O                 | I/O                              | I/O                 |
| 37           | I/O                 | I/O                              | I/O                 |
| 38           | I/O                 | I/O                              | I/O                 |
| 39           | I/O                 | I/O                              | I/O                 |
| 40           | NC                  | I/O                              | I/O                 |
| 41           | I/O                 | I/O                              | I/O                 |
| 42           | NC                  | I/O                              | I/O                 |
| 43           | I/O                 | I/O                              | I/O                 |
| 44           | GND                 | GND                              | GND                 |
| 45           | I/O                 | I/O                              | I/O                 |
| 46           | I/O                 | I/O                              | I/O                 |
| 47           | I/O                 | I/O                              | I/O                 |
| 48           | I/O                 | I/O                              | I/O                 |
| 49           | I/O                 | I/O                              | I/O                 |
| 50           | I/O                 | I/O                              | I/O                 |
| 51           | I/O                 | I/O                              | I/O                 |
| 52           | V <sub>CCI</sub>    | V <sub>CCI</sub>                 | V <sub>CCI</sub>    |
| 53           | I/O                 | I/O                              | I/O                 |
| 54           | NC                  | I/O                              | I/O                 |
| 55           | I/O                 | I/O                              | I/O                 |
| 56           | I/O                 | I/O                              | I/O                 |
| 57           | NC                  | I/O                              | I/O                 |
| 58           | I/O                 | I/O                              | I/O                 |
| 59           | I/O                 | I/O                              | I/O                 |
| 60           | I/O                 | I/O                              | I/O                 |
| 61           | I/O                 | I/O                              | I/O                 |
| 62           | I/O                 | I/O                              | I/O                 |
| 63           | I/O                 | I/O                              | I/O                 |
| 64           | PRB, I/O            | PRB, I/O                         | PRB, I/O            |
| 65           | GND                 | GND                              | GND                 |
| 66           | V <sub>CCA</sub>    | V <sub>CCA</sub>                 | V <sub>CCA</sub>    |
| 67           | V <sub>CCR</sub>    | V <sub>CCR</sub>                 | V <sub>CCR</sub>    |
| 68           | I/O                 | I/O                              | I/O                 |

| 100-Pin VQFP |                  |                            |
|--------------|------------------|----------------------------|
| Pin Number   | A54SX08 Function | A54SX16, A54SX16P Function |
| 1            | GND              | GND                        |
| 2            | TDI, I/O         | TDI, I/O                   |
| 3            | I/O              | I/O                        |
| 4            | I/O              | I/O                        |
| 5            | I/O              | I/O                        |
| 6            | I/O              | I/O                        |
| 7            | TMS              | TMS                        |
| 8            | V <sub>CCI</sub> | V <sub>CCI</sub>           |
| 9            | GND              | GND                        |
| 10           | I/O              | I/O                        |
| 11           | I/O              | I/O                        |
| 12           | I/O              | I/O                        |
| 13           | I/O              | I/O                        |
| 14           | I/O              | I/O                        |
| 15           | I/O              | I/O                        |
| 16           | I/O              | I/O                        |
| 17           | I/O              | I/O                        |
| 18           | I/O              | I/O                        |
| 19           | I/O              | I/O                        |
| 20           | V <sub>CCI</sub> | V <sub>CCI</sub>           |
| 21           | I/O              | I/O                        |
| 22           | I/O              | I/O                        |
| 23           | I/O              | I/O                        |
| 24           | I/O              | I/O                        |
| 25           | I/O              | I/O                        |
| 26           | I/O              | I/O                        |
| 27           | I/O              | I/O                        |
| 28           | I/O              | I/O                        |
| 29           | I/O              | I/O                        |
| 30           | I/O              | I/O                        |
| 31           | I/O              | I/O                        |
| 32           | I/O              | I/O                        |
| 33           | I/O              | I/O                        |
| 34           | PRB, I/O         | PRB, I/O                   |

| 100-Pin VQFP |                  |                            |
|--------------|------------------|----------------------------|
| Pin Number   | A54SX08 Function | A54SX16, A54SX16P Function |
| 35           | V <sub>CCA</sub> | V <sub>CCA</sub>           |
| 36           | GND              | GND                        |
| 37           | V <sub>CCR</sub> | V <sub>CCR</sub>           |
| 38           | I/O              | I/O                        |
| 39           | HCLK             | HCLK                       |
| 40           | I/O              | I/O                        |
| 41           | I/O              | I/O                        |
| 42           | I/O              | I/O                        |
| 43           | I/O              | I/O                        |
| 44           | V <sub>CCI</sub> | V <sub>CCI</sub>           |
| 45           | I/O              | I/O                        |
| 46           | I/O              | I/O                        |
| 47           | I/O              | I/O                        |
| 48           | I/O              | I/O                        |
| 49           | TDO, I/O         | TDO, I/O                   |
| 50           | I/O              | I/O                        |
| 51           | GND              | GND                        |
| 52           | I/O              | I/O                        |
| 53           | I/O              | I/O                        |
| 54           | I/O              | I/O                        |
| 55           | I/O              | I/O                        |
| 56           | I/O              | I/O                        |
| 57           | V <sub>CCA</sub> | V <sub>CCA</sub>           |
| 58           | V <sub>CCI</sub> | V <sub>CCI</sub>           |
| 59           | I/O              | I/O                        |
| 60           | I/O              | I/O                        |
| 61           | I/O              | I/O                        |
| 62           | I/O              | I/O                        |
| 63           | I/O              | I/O                        |
| 64           | I/O              | I/O                        |
| 65           | I/O              | I/O                        |
| 66           | I/O              | I/O                        |
| 67           | V <sub>CCA</sub> | V <sub>CCA</sub>           |
| 68           | GND              | GND                        |

| 100-Pin VQFP |                  |                            |
|--------------|------------------|----------------------------|
| Pin Number   | A54SX08 Function | A54SX16, A54SX16P Function |
| 69           | GND              | GND                        |
| 70           | I/O              | I/O                        |
| 71           | I/O              | I/O                        |
| 72           | I/O              | I/O                        |
| 73           | I/O              | I/O                        |
| 74           | I/O              | I/O                        |
| 75           | I/O              | I/O                        |
| 76           | I/O              | I/O                        |
| 77           | I/O              | I/O                        |
| 78           | I/O              | I/O                        |
| 79           | I/O              | I/O                        |
| 80           | I/O              | I/O                        |
| 81           | I/O              | I/O                        |
| 82           | V <sub>CCI</sub> | V <sub>CCI</sub>           |
| 83           | I/O              | I/O                        |
| 84           | I/O              | I/O                        |
| 85           | I/O              | I/O                        |
| 86           | I/O              | I/O                        |
| 87           | CLKA             | CLKA                       |
| 88           | CLKB             | CLKB                       |
| 89           | V <sub>CCR</sub> | V <sub>CCR</sub>           |
| 90           | V <sub>CCA</sub> | V <sub>CCA</sub>           |
| 91           | GND              | GND                        |
| 92           | PRA, I/O         | PRA, I/O                   |
| 93           | I/O              | I/O                        |
| 94           | I/O              | I/O                        |
| 95           | I/O              | I/O                        |
| 96           | I/O              | I/O                        |
| 97           | I/O              | I/O                        |
| 98           | I/O              | I/O                        |
| 99           | I/O              | I/O                        |
| 100          | TCK, I/O         | TCK, I/O                   |

| 313-Pin PBGA |                  | 313-Pin PBGA |                  | 313-Pin PBGA |                  | 313-Pin PBGA |                  |
|--------------|------------------|--------------|------------------|--------------|------------------|--------------|------------------|
| Pin Number   | A54SX32 Function | Pin Number   | A54SX32 Function | Pin Number   | A54SX32 Function | Pin Number   | A54SX32 Function |
| H20          | I/O              | L25          | I/O              | R5           | I/O              | V10          | I/O              |
| H22          | V <sub>CCI</sub> | M2           | I/O              | R7           | I/O              | V12          | I/O              |
| H24          | I/O              | M4           | I/O              | R9           | I/O              | V14          | I/O              |
| J1           | I/O              | M6           | I/O              | R11          | I/O              | V16          | NC               |
| J3           | I/O              | M8           | I/O              | R13          | GND              | V18          | I/O              |
| J5           | I/O              | M10          | I/O              | R15          | I/O              | V20          | I/O              |
| J7           | NC               | M12          | GND              | R17          | I/O              | V22          | V <sub>CCA</sub> |
| J9           | I/O              | M14          | GND              | R19          | I/O              | V24          | V <sub>CCI</sub> |
| J11          | I/O              | M16          | V <sub>CCI</sub> | R21          | I/O              | W1           | I/O              |
| J13          | CLKA             | M18          | I/O              | R23          | I/O              | W3           | I/O              |
| J15          | I/O              | M20          | I/O              | R25          | I/O              | W5           | I/O              |
| J17          | I/O              | M22          | I/O              | T2           | I/O              | W7           | NC               |
| J19          | I/O              | M24          | I/O              | T4           | I/O              | W9           | I/O              |
| J21          | GND              | N1           | I/O              | T6           | I/O              | W11          | I/O              |
| J23          | I/O              | N3           | V <sub>CCA</sub> | T8           | I/O              | W13          | V <sub>CCI</sub> |
| J25          | I/O              | N5           | V <sub>CCR</sub> | T10          | I/O              | W15          | I/O              |
| K2           | I/O              | N7           | I/O              | T12          | I/O              | W17          | I/O              |
| K4           | I/O              | N9           | V <sub>CCI</sub> | T14          | HCLK             | W19          | I/O              |
| K6           | I/O              | N11          | GND              | T16          | I/O              | W21          | I/O              |
| K8           | V <sub>CCI</sub> | N13          | GND              | T18          | I/O              | W23          | I/O              |
| K10          | I/O              | N15          | GND              | T20          | I/O              | W25          | I/O              |
| K12          | I/O              | N17          | I/O              | T22          | I/O              | Y2           | I/O              |
| K14          | I/O              | N19          | I/O              | T24          | I/O              | Y4           | I/O              |
| K16          | I/O              | N21          | I/O              | U1           | I/O              | Y6           | I/O              |
| K18          | I/O              | N23          | V <sub>CCR</sub> | U3           | I/O              | Y8           | I/O              |
| K20          | V <sub>CCA</sub> | N25          | V <sub>CCA</sub> | U5           | V <sub>CCI</sub> | Y10          | I/O              |
| K22          | I/O              | P2           | I/O              | U7           | I/O              | Y12          | I/O              |
| K24          | I/O              | P4           | I/O              | U9           | I/O              | Y14          | I/O              |
| L1           | I/O              | P6           | I/O              | U11          | I/O              | Y16          | I/O              |
| L3           | I/O              | P8           | I/O              | U13          | I/O              | Y18          | I/O              |
| L5           | I/O              | P10          | I/O              | U15          | I/O              | Y20          | NC               |
| L7           | I/O              | P12          | GND              | U17          | I/O              | Y22          | I/O              |
| L9           | I/O              | P14          | GND              | U19          | I/O              | Y24          | NC               |
| L11          | I/O              | P16          | I/O              | U21          | I/O              |              |                  |
| L13          | GND              | P18          | I/O              | U23          | I/O              |              |                  |
| L15          | I/O              | P20          | NC               | U25          | I/O              |              |                  |
| L17          | I/O              | P22          | I/O              | V2           | V <sub>CCA</sub> |              |                  |
| L19          | I/O              | P24          | I/O              | V4           | I/O              |              |                  |
| L21          | I/O              | R1           | I/O              | V6           | I/O              |              |                  |
| L23          | I/O              | R3           | I/O              | V8           | I/O              |              |                  |

## 329-Pin PBGA

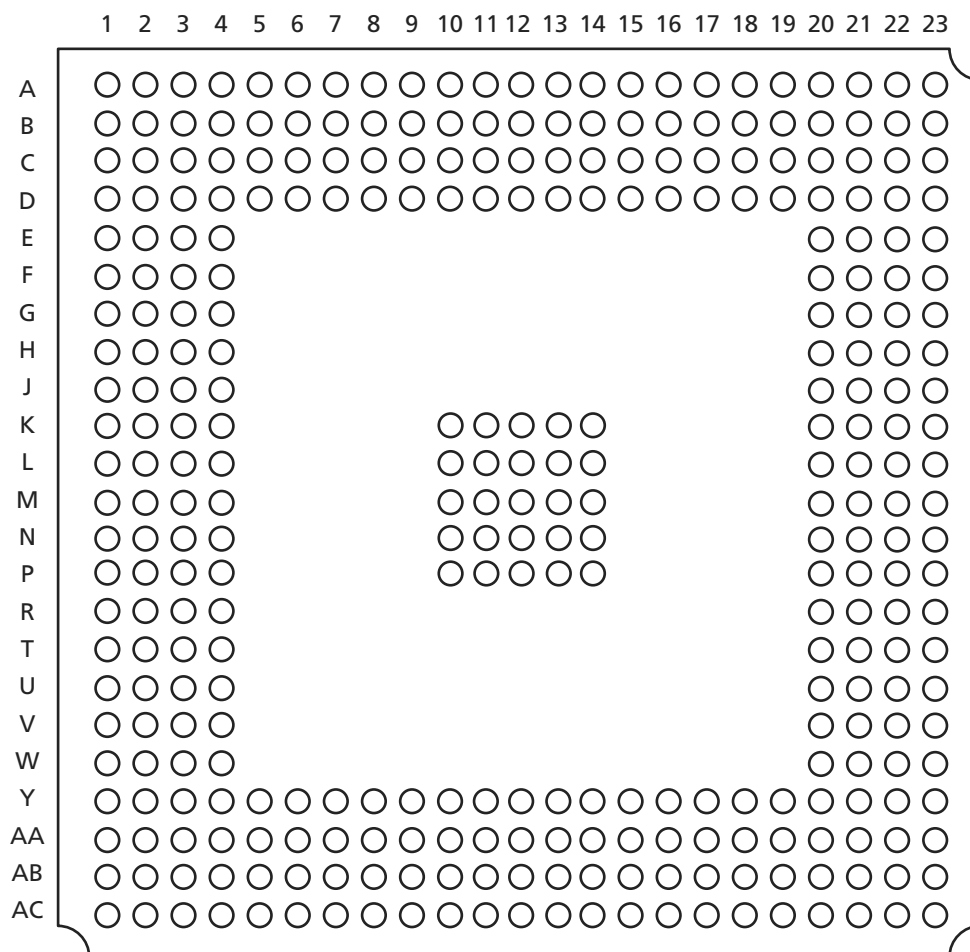


Figure 2-7 • 329-Pin PBGA (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

# 144-Pin FBGA

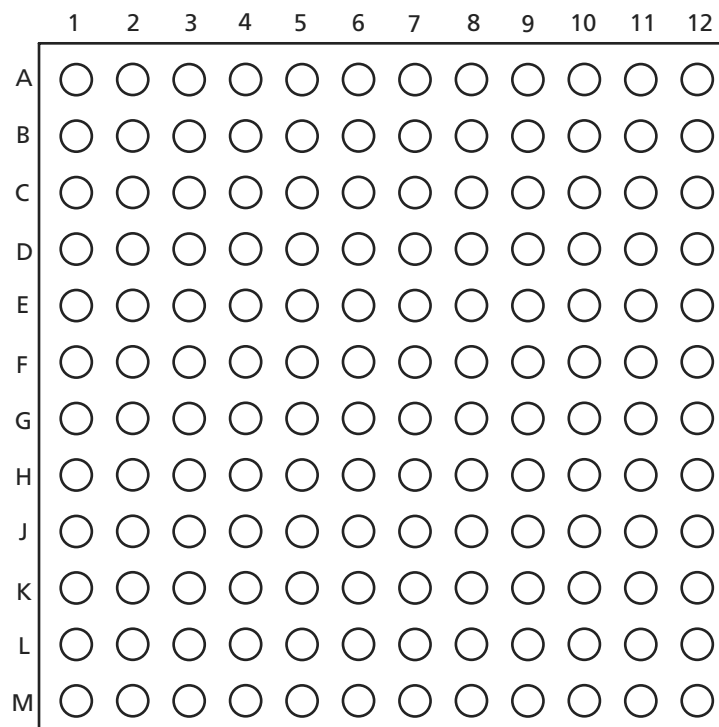


Figure 2-8 • 144-Pin FBGA (Top View)

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.