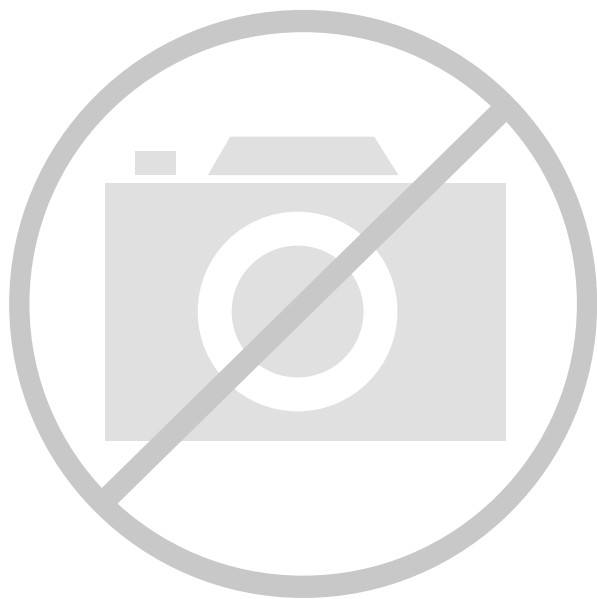




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	147
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx16-2tq176i

Chip Architecture

The SX family chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *clusters*. There are two types of *clusters*: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (Figure 1-4). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

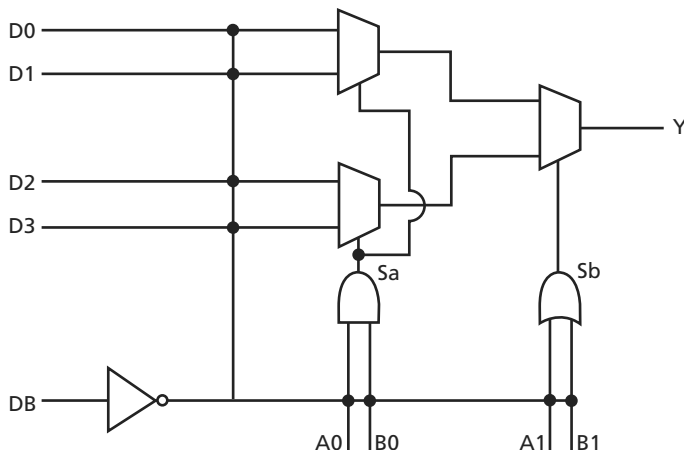


Figure 1-3 • C-Cell

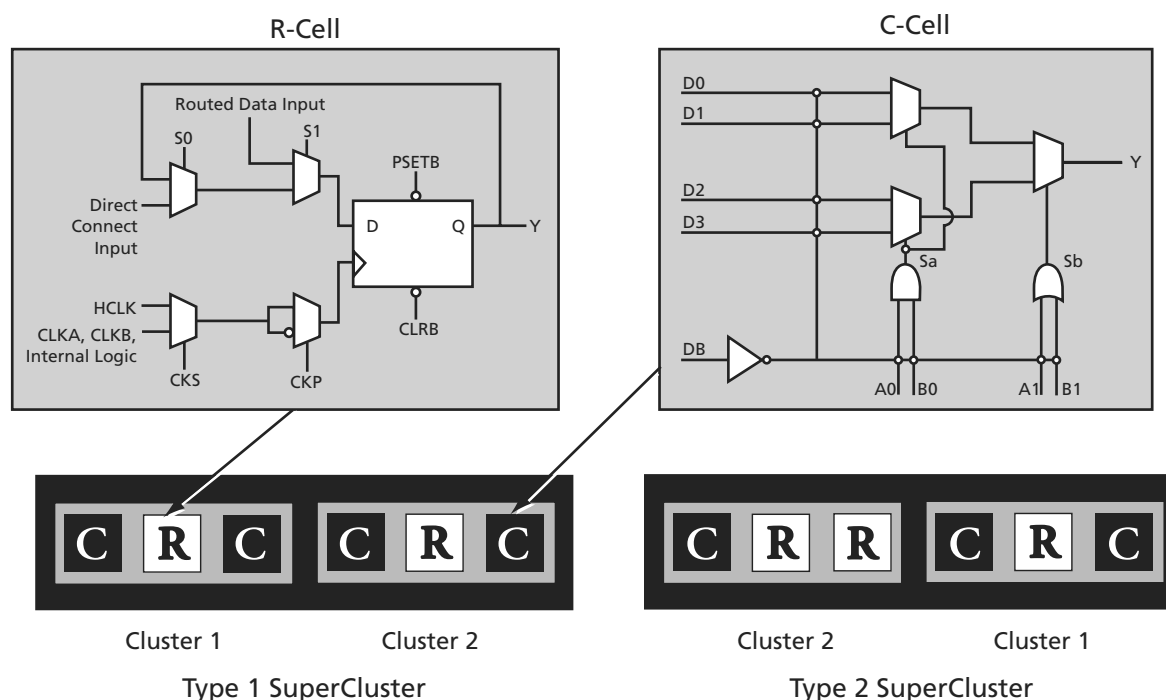


Figure 1-4 • Cluster Organization

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

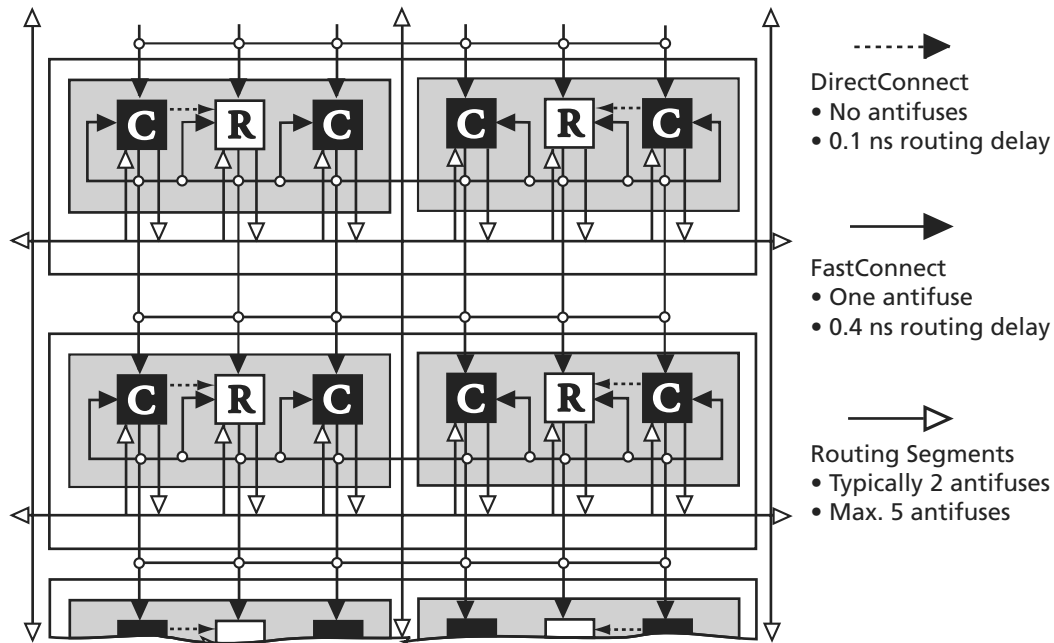


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

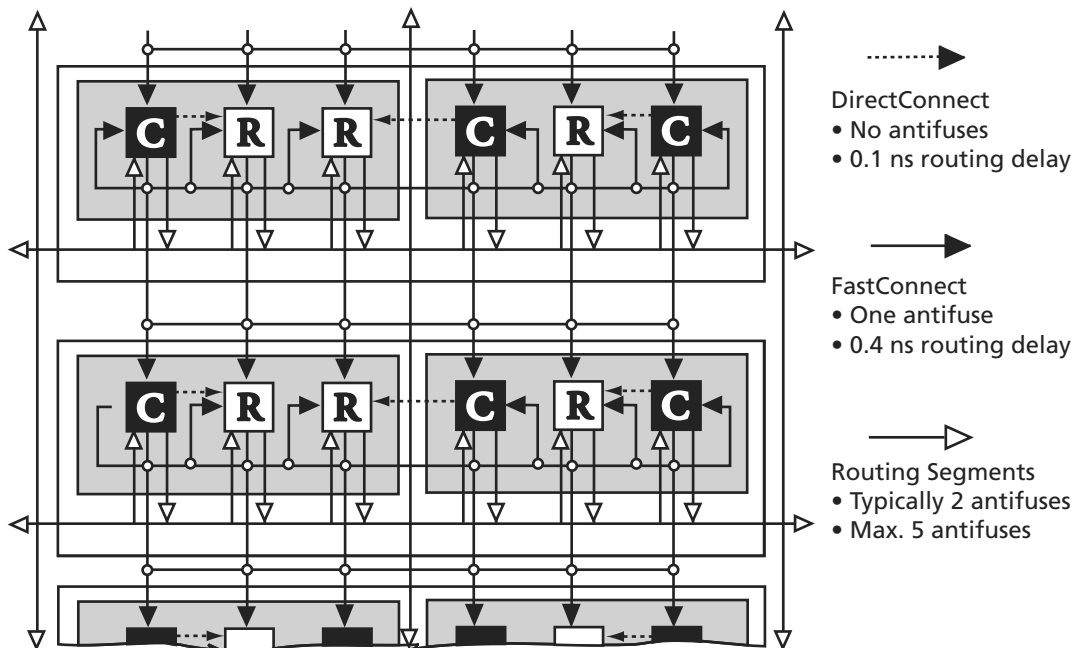


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

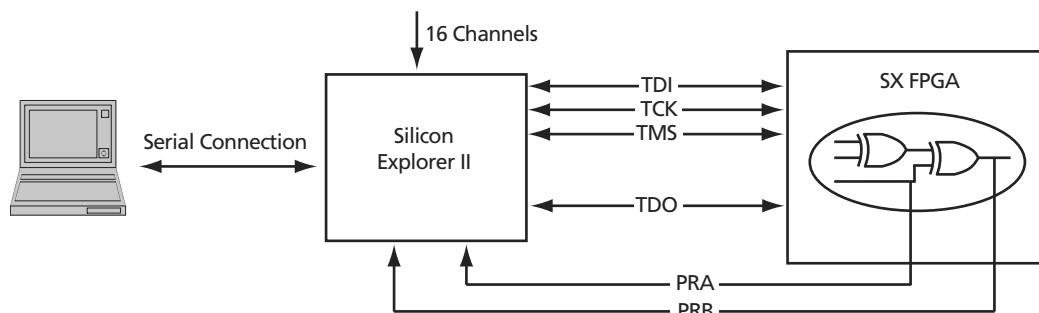


Figure 1-8 • Probe Setup

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II are compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an SX device using Silicon Sculptor II are as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming SX devices, refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

3.3 V / 5 V Operating Conditions

Table 1-3 • Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
V_{CCR}^2	DC Supply Voltage ³	-0.3 to + 6.0	V
V_{CCA}^2	DC Supply Voltage	-0.3 to + 4.0	V
V_{CCI}^2	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	-0.3 to + 4.0	V
V_{CCI}^2	DC Supply Voltage (A54SX16P)	-0.3 to + 6.0	V
V_I	Input Voltage	-0.5 to + 5.5	V
V_O	Output Voltage	-0.5 to + 3.6	V
I_{IO}	I/O Source Sink Current ³	-30 to + 5.0	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.
2. V_{CCR} in the A54SX16P must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.
3. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than $V_{CC} + 0.5$ V or less than $GND - 0.5$ V, the internal protection diodes will forward-bias and can draw excessive current.

Table 1-4 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to + 70	–40 to + 85	–55 to +125	°C
3.3 V Power Supply Tolerance	±10	±10	±10	%V _{CC}
5.0 V Power Supply Tolerance	±5	±10	±10	%V _{CC}

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Table 1-5 • Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V _{OH}	(I _{OH} = –20 μ A) (CMOS) (I _{OH} = –8 mA) (TTL) (I _{OH} = –6 mA) (TTL)	(V _{CCI} – 0.1) 2.4	V _{CCI} V _{CCI}	(V _{CCI} – 0.1) 2.4	V _{CCI} V _{CCI}	V
V _{OL}	(I _{OL} = 20 μ A) (CMOS) (I _{OL} = 12 mA) (TTL) (I _{OL} = 8 mA) (TTL)		0.10 0.50		0.50	V
V _{IL}			0.8		0.8	V
V _{IH}		2.0		2.0		V
t _R , t _F	Input Transition Time t _R , t _F		50		50	ns
C _{IO}	C _{IO} I/O Capacitance		10		10	pF
I _{CC}	Standby Current, I _{CC}		4.0		4.0	mA
I _{CC(D)}	I _{CC(D)} I _{Dynamic} V _{CC} Supply Current	See "Evaluating Power in SX Devices" on page 1-16.				

Figure 1-9 shows the 5.0 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

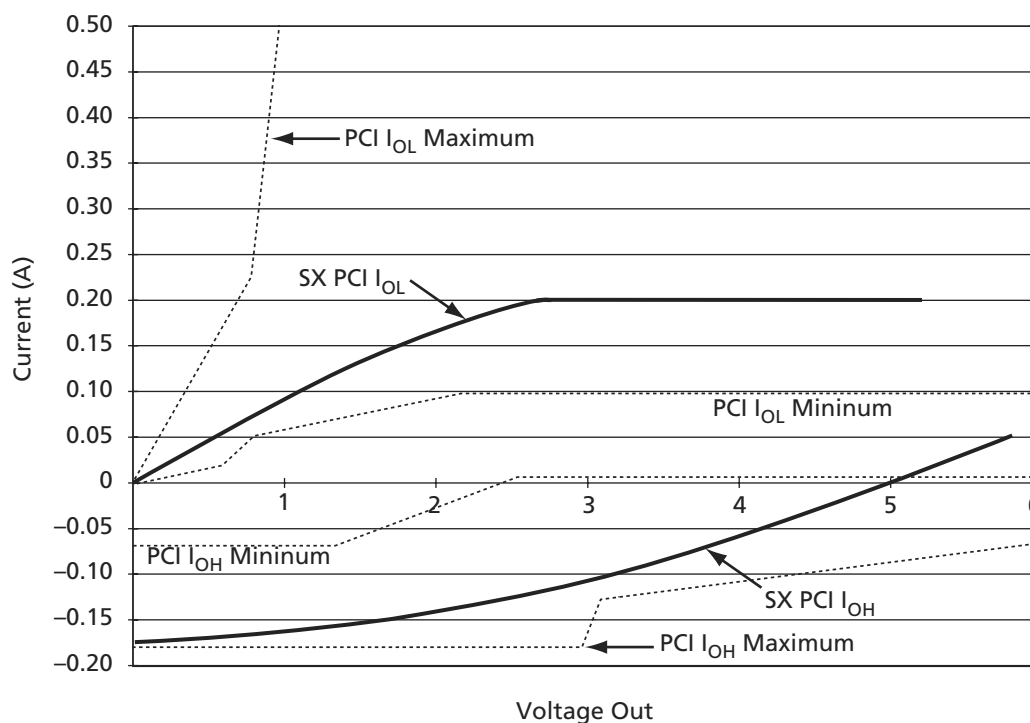


Figure 1-9 • 5.0 V PCI Curve for A54SX16P Device

$$I_{OH} = 11.9 \times (V_{OUT} - 5.25) \times (V_{OUT} + 2.45)$$

for $V_{CC} > V_{OUT} > 3.1$ V

EQ 1-1

$$I_{OL} = 78.5 \times V_{OUT} \times (4.4 - V_{OUT})$$

for 0 V $< V_{OUT} < 0.71$ V

EQ 1-2

A54SX16P DC Specifications (3.3 V PCI Operation)

Table 1-8 • A54SX16P DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		3.0	3.6	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CC}$	V
I_{PU}	Input Pull-up Voltage ¹		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current ²	$0 < V_{IN} < V_{CC}$		± 10	μA
V_{OH}	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OUT} = 1500 \mu A$		$0.1V_{CC}$	V
C_{IN}	Input Pin Capacitance ³			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance ⁴			8	pF

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

Step 1: Define Terms Used in Formula

Module	V_{CCA}	3.3
Number of logic modules switching at f_m (Used 50%)	m	264
Average logic modules switching rate f_m (MHz) (Guidelines: $f/10$)	f_m	20
Module capacitance C_{EQM} (pF)	C_{EQM}	4.0
Input Buffer		
Number of input buffers switching at f_n	n	1
Average input switching rate f_n (MHz) (Guidelines: $f/5$)	f_n	40
Input buffer capacitance C_{EQI} (pF)	C_{EQI}	3.4
Output Buffer		
Number of output buffers switching at f_p	p	1
Average output buffers switching rate f_p (MHz) (Guidelines: $f/10$)	f_p	20
Output buffers buffer capacitance C_{EQO} (pF)	C_{EQO}	4.7
Output Load capacitance C_L (pF)	C_L	35
RCLKA		
Number of Clock loads q_1	q_1	528
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q1}	200
Fixed capacitance (pF)	r_1	138
RCLKB		
Number of Clock loads q_2	q_2	0
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q2}	0
Fixed capacitance (pF)	r_2	138
HCLK		
Number of Clock loads	s_1	0
Variable capacitance of dedicated array clock (pF)	C_{EQHV}	0.61 5
Fixed capacitance of dedicated array clock (pF)	C_{EQHF}	96
Average clock rate (MHz)	f_{s1}	0

Step 2: Calculate Dynamic Power Consumption

$V_{CCA} \times V_{CCA}$	10.89
$m \times f_m \times C_{EQM}$	0.02112
$n \times f_n \times C_{EQI}$	0.000136
$p \times f_p \times (C_{EQO} + C_L)$	0.000794
$0.5 (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1})$	0.11208
$0.5 (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2})$	0
$0.5 (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1})$	0
$P_{AC} = 1.461 \text{ W}$	

Step 3: Calculate DC Power Dissipation**DC Power Dissipation**

$$P_{DC} = (I_{\text{standby}}) \times V_{CCA} + (I_{\text{standby}}) \times V_{CCR} + (I_{\text{standby}}) \times V_{CCI} + X \times V_{OL} \times I_{OL} + Y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-12

For a rough estimate of DC Power Dissipation, only use $P_{DC} = (I_{\text{standby}}) \times V_{CCA}$. The rest of the formula provides a very small number that can be considered negligible.

$$P_{DC} = (I_{\text{standby}}) \times V_{CCA}$$

$$P_{DC} = .55 \text{ mA} \times 3.3 \text{ V}$$

$$P_{DC} = 0.001815 \text{ W}$$

Step 4: Calculate Total Power Consumption

$$P_{\text{Total}} = P_{AC} + P_{DC}$$

$$P_{\text{Total}} = 1.461 + 0.001815$$

$$P_{\text{Total}} = 1.4628 \text{ W}$$

Step 5: Compare Estimated Power Consumption against Characterized Power Consumption

The estimated total power consumption for this design is 1.46 W. The characterized power consumption for this design at 200 MHz is 1.0164 W.

Table 1-15 • Package Thermal Characteristics

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min.	Units
Plastic Leaded Chip Carrier (PLCC)	84	12	32	22	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Very Thin Quad Flatpack (VQFP)	100	10	38	32	°C/W
Plastic Quad Flat Pack (PQFP) without Heat Spreader	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	14.5	°C/W
Plastic Ball Grid Array (PBGA)	313	3	23	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W

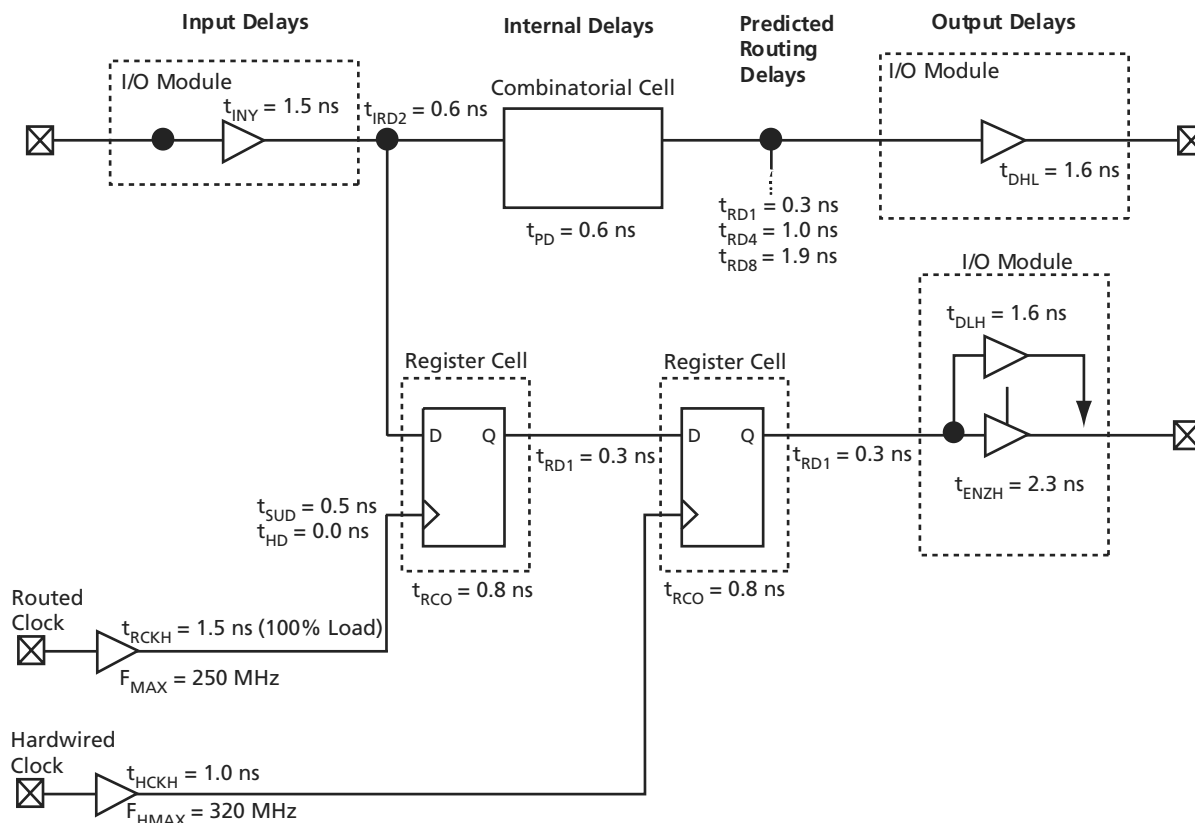
Note: SX08 does not have a heat spreader.

Table 1-16 • Temperature and Voltage Derating Factors*

V_{CCA}	Junction Temperature						
	-55	-40	0	25	70	85	125
3.0	0.75	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.70	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.66	0.69	0.77	0.78	0.87	0.92	1.02

Note: *Normalized to worst-case commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 3.0\text{ V}$

SX Timing Model



Note: Values shown for A54SX08-3, worst-case commercial conditions.

Figure 1-12 • SX Timing Model

Hardwired Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.0 = 1.3 \text{ ns} \end{aligned}$$

EQ 1-15

Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.0 + 0.8 + 0.3 + 1.6 = 3.7 \text{ ns} \end{aligned}$$

EQ 1-16

Routed Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.5 = 0.8 \text{ ns} \end{aligned}$$

EQ 1-17

Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.52 + 0.8 + 0.3 + 1.6 = 4.2 \text{ ns} \end{aligned}$$

EQ 1-18

Table 1-17 • A54SX08 Timing Characteristics (Continued)

(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t _{HCKH}	Input LOW to HIGH (pad to R-Cell input)	1.0		1.1		1.3		1.5		ns
t _{HCKL}	Input HIGH to LOW (pad to R-Cell input)	1.0		1.2		1.4		1.6		ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew	0.1		0.2		0.2		0.2		ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t _{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)	1.3		1.5		1.7		2.0		ns
t _{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell Input)	1.4		1.6		1.8		2.1		ns
t _{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)	1.4		1.7		1.9		2.2		ns
t _{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)	1.5		1.7		2.0		2.3		ns
t _{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)	1.5		1.7		1.9		2.2		ns
t _{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)	1.5		1.8		2.0		2.3		ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (light load)	0.1		0.2		0.2		0.2		ns
t _{RCKSW}	Maximum Skew (50% load)	0.3		0.3		0.4		0.4		ns
t _{RCKSW}	Maximum Skew (100% load)	0.3		0.3		0.4		0.4		ns
TTL Output Module Timing1										
t _{DLH}	Data-to-Pad LOW to HIGH	1.6		1.9		2.1		2.5		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.6		1.9		2.1		2.5		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.8		3.2		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3		2.7		3.1		3.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	1.4		1.7		1.9		2.2		ns

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics**
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ¹										
t _{PD}	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays ²										
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{RD2}	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t _{RD3}	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t _{RD4}	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{RD8}	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t _{RD12}	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t _{RCO}	Sequential Clock-to-Q	0.8		1.1		1.2		1.4		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t _{INYH}	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t _{INYL}	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays ²										
t _{IRD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{IRD2}	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t _{IRD3}	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t _{IRD4}	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{IRD8}	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t _{IRD12}	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} , the loading is 5 pF.

A54SX16P Timing Characteristics

Table 1-19 • **A54SX16P Timing Characteristics**
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ¹										
t _{PD}	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays ²										
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{RD2}	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t _{RD3}	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t _{RD4}	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{RD8}	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t _{RD12}	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t _{RCO}	Sequential Clock-to-Q	0.9		1.1		1.3		1.4		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t _{INYH}	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t _{INYL}	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays ²										
t _{IRD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{IRD2}	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t _{IRD3}	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t _{IRD4}	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{IRD8}	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t _{IRD12}	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 10 pF loading.

A54SX32 Timing Characteristics

Table 1-20 • **A54SX32 Timing Characteristics**
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ¹										
t _{PD}	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays ²										
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{RD2}	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t _{RD3}	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{RD4}	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t _{RD8}	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t _{RD12}	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns
R-Cell Timing										
t _{RCO}	Sequential Clock-to-Q	0.8		1.1		1.3		1.4		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t _{INYH}	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t _{INYL}	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays ²										
t _{IRD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{IRD2}	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t _{IRD3}	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{IRD4}	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t _{IRD8}	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t _{IRD12}	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} the loading is 5 pF.

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
73	NC	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND
78	V _{CCA}	V _{CCA}	V _{CCA}
79	GND	GND	GND
80	V _{CCR}	V _{CCR}	V _{CCR}
81	I/O	I/O	I/O
82	HCLK	HCLK	HCLK
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	NC	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	NC	I/O	I/O
89	I/O	I/O	I/O
90	I/O	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	NC	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	NC	I/O	I/O
98	V _{CCI}	V _{CCI}	V _{CCI}
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	I/O	I/O
107	I/O	I/O	I/O
108	NC	I/O	I/O

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	V _{CCA}	V _{CCA}	V _{CCA}
115	V _{CCI}	V _{CCI}	V _{CCI}
116	NC	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	NC	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	NC	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	NC	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	GND	GND	GND
130	V _{CCA}	V _{CCA}	V _{CCA}
131	GND	GND	GND
132	V _{CCR}	V _{CCR}	V _{CCR}
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	I/O	I/O	I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
145	V _{CCA}	V _{CCA}	V _{CCA}
146	GND	GND	GND
147	I/O	I/O	I/O
148	V _{CCI}	V _{CCI}	V _{CCI}
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	NC	I/O	I/O
156	NC	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	V _{CCI}	V _{CCI}	V _{CCI}
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	NC	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	NC	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	NC	I/O	I/O
177	I/O	I/O	I/O
178	I/O	I/O	I/O
179	I/O	I/O	I/O
180	CLKA	CLKA	CLKA

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
181	CLKB	CLKB	CLKB
182	V _{CCR}	V _{CCR}	V _{CCR}
183	GND	GND	GND
184	V _{CCA}	V _{CCA}	V _{CCA}
185	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	NC	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	NC	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	NC	I/O	I/O
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	NC	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	V _{CCI}	V _{CCI}	V _{CCI}
202	NC	I/O	I/O
203	NC	I/O	I/O
204	I/O	I/O	I/O
205	NC	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V _{CCA}	V _{CCA}	V _{CCA}
80	V _{CCI}	V _{CCI}	V _{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V _{CCA}	V _{CCA}	V _{CCA}
90	V _{CCR}	V _{CCR}	V _{CCR}
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V _{CCI}	V _{CCI}	V _{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
109	GND	GND	GND
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V _{CCI}	V _{CCI}	V _{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	V _{CCR}	V _{CCR}	V _{CCR}
128	GND	GND	GND
129	V _{CCA}	V _{CCA}	V _{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

176-Pin TQFP

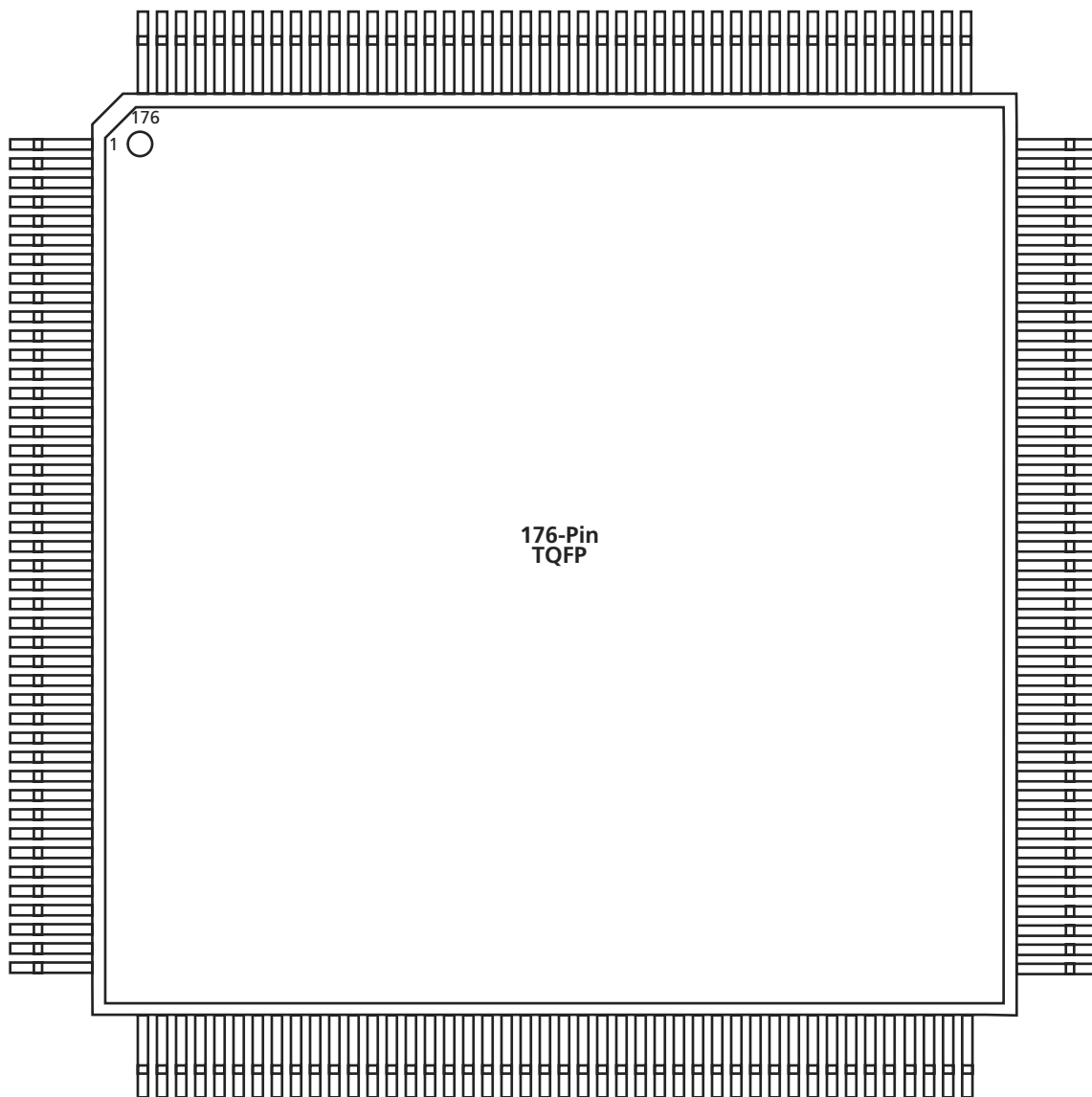


Figure 2-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V _{CCI}	V _{CCI}	V _{CCI}
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V _{CCA}	V _{CCA}	V _{CCA}
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V _{CCI}	V _{CCI}	V _{CCI}
33	V _{CCA}	V _{CCA}	V _{CCA}
34	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V _{CCI}	V _{CCI}	V _{CCI}
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V _{CCA}	V _{CCA}	V _{CCA}
67	V _{CCR}	V _{CCR}	V _{CCR}
68	I/O	I/O	I/O

100-Pin VQFP		
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	TMS	TMS
8	V _{CCI}	V _{CCI}
9	GND	GND
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	V _{CCI}	V _{CCI}
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	PRB, I/O	PRB, I/O

100-Pin VQFP		
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
35	V _{CCA}	V _{CCA}
36	GND	GND
37	V _{CCR}	V _{CCR}
38	I/O	I/O
39	HCLK	HCLK
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	V _{CCI}	V _{CCI}
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	TDO, I/O	TDO, I/O
50	I/O	I/O
51	GND	GND
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	V _{CCA}	V _{CCA}
58	V _{CCI}	V _{CCI}
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	V _{CCA}	V _{CCA}
68	GND	GND

100-Pin VQFP		
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
69	GND	GND
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	V _{CCI}	V _{CCI}
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	CLKA	CLKA
88	CLKB	CLKB
89	V _{CCR}	V _{CCR}
90	V _{CCA}	V _{CCA}
91	GND	GND
92	PRA, I/O	PRA, I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	TCK, I/O	TCK, I/O

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function
D3	I/O	F22	I/O	K20	I/O	N11	GND
D4	TCK, I/O	F23	I/O	K21	I/O	N12	GND
D5	I/O	G1	I/O	K22	I/O	N13	GND
D6	I/O	G2	I/O	K23	I/O	N14	GND
D7	I/O	G3	I/O	L1	I/O	N20	NC
D8	I/O	G4	I/O	L2	I/O	N21	I/O
D9	I/O	G20	I/O	L3	I/O	N22	I/O
D10	I/O	G21	I/O	L4	V _{CCR}	N23	I/O
D11	V _{CCA}	G22	I/O	L10	GND	P1	I/O
D12	V _{CCR}	G23	GND	L11	GND	P2	I/O
D13	I/O	H1	I/O	L12	GND	P3	I/O
D14	I/O	H2	I/O	L13	GND	P4	I/O
D15	I/O	H3	I/O	L14	GND	P10	GND
D16	I/O	H4	I/O	L20	V _{CCR}	P11	GND
D17	I/O	H20	V _{CCA}	L21	I/O	P12	GND
D18	I/O	H21	I/O	L22	I/O	P13	GND
D19	I/O	H22	I/O	L23	NC	P14	GND
D20	I/O	H23	I/O	M1	I/O	P20	I/O
D21	I/O	J1	NC	M2	I/O	P21	I/O
D22	I/O	J2	I/O	M3	I/O	P22	I/O
D23	I/O	J3	I/O	M4	V _{CCA}	P23	I/O
E1	V _{CCI}	J4	I/O	M10	GND	R1	I/O
E2	I/O	J20	I/O	M11	GND	R2	I/O
E3	I/O	J21	I/O	M12	GND	R3	I/O
E4	I/O	J22	I/O	M13	GND	R4	I/O
E20	I/O	J23	I/O	M14	GND	R20	I/O
E21	I/O	K1	I/O	M20	V _{CCA}	R21	I/O
E22	I/O	K2	I/O	M21	I/O	R22	I/O
E23	I/O	K3	I/O	M22	I/O	R23	I/O
F1	I/O	K4	I/O	M23	V _{CCI}	T1	I/O
F2	TMS	K10	GND	N1	I/O	T2	I/O
F3	I/O	K11	GND	N2	I/O	T3	I/O
F4	I/O	K12	GND	N3	I/O	T4	I/O
F20	I/O	K13	GND	N4	I/O	T20	I/O
F21	I/O	K14	GND	N10	GND	T21	I/O