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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.
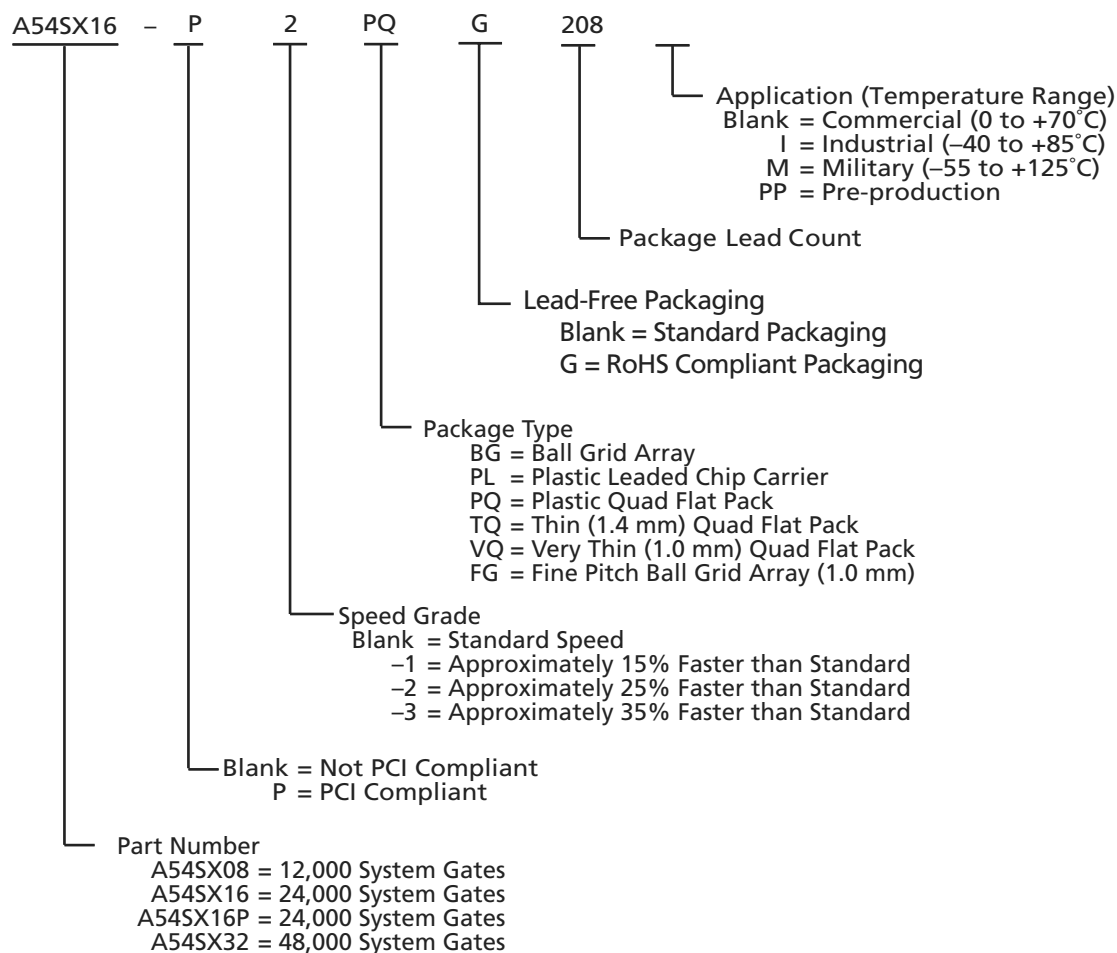
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx16-vq100i

Ordering Information

```
A54SX16   –   P   2   PQ   G   208
```

Application (Temperature Range)
Blank = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
PP = Pre-production

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
BG = Ball Grid Array
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flat Pack
TQ = Thin (1.4 mm) Quad Flat Pack
VQ = Very Thin (1.0 mm) Quad Flat Pack
FG = Fine Pitch Ball Grid Array (1.0 mm)

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% Faster than Standard
–2 = Approximately 25% Faster than Standard
–3 = Approximately 35% Faster than Standard

Blank = Not PCI Compliant
P = PCI Compliant

Part Number
A54SX08 = 12,000 System Gates
A54SX16 = 24,000 System Gates
A54SX16P = 24,000 System Gates
A54SX32 = 48,000 System Gates

Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PLCC 84-Pin	VQFP 100-Pin	PQFP 208-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 313-Pin	PBGA 329-Pin	FBGA 144-Pin
A54SX08	69	81	130	113	128	–	–	111
A54SX16	–	81	175	–	147	–	–	–
A54SX16P	–	81	175	113	147	–	–	–
A54SX32	–	–	174	113	147	249	249	–

Note: *Package Definitions (Consult your local Actel sales representative for product availability):*
PLCC = Plastic Leaded Chip Carrier
PQFP = Plastic Quad Flat Pack
TQFP = Thin Quad Flat Pack
VQFP = Very Thin Quad Flat Pack
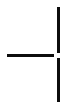*PBGA = Plastic Ball Grid Array*
FBGA = Fine Pitch (1.0 mm) Ball Grid Array

Table of Contents

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.
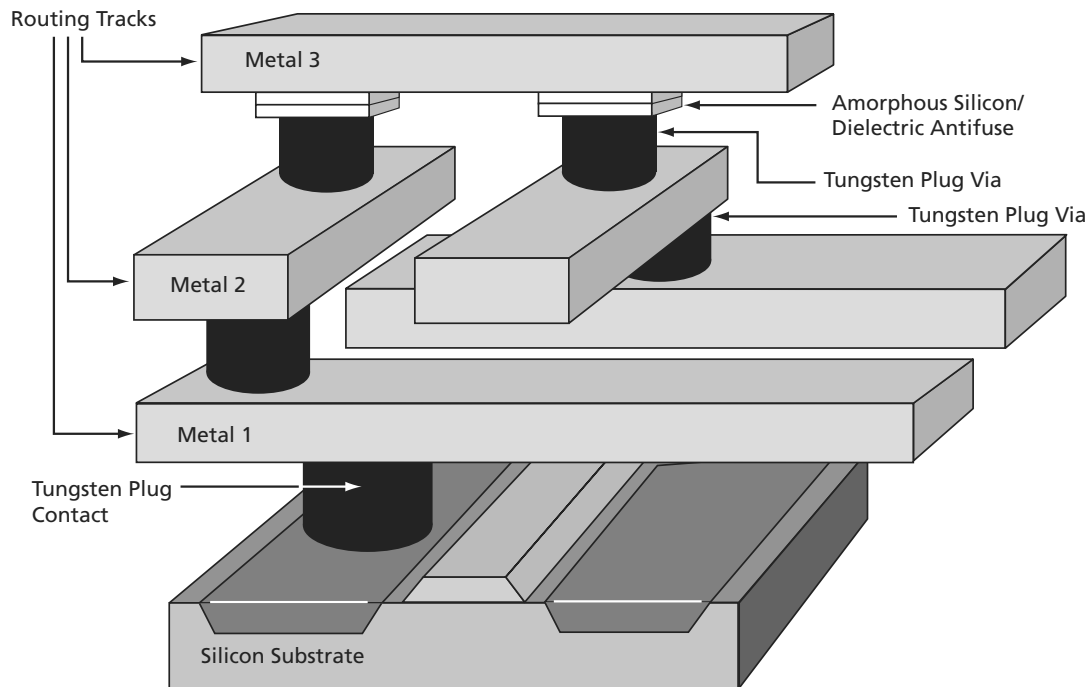

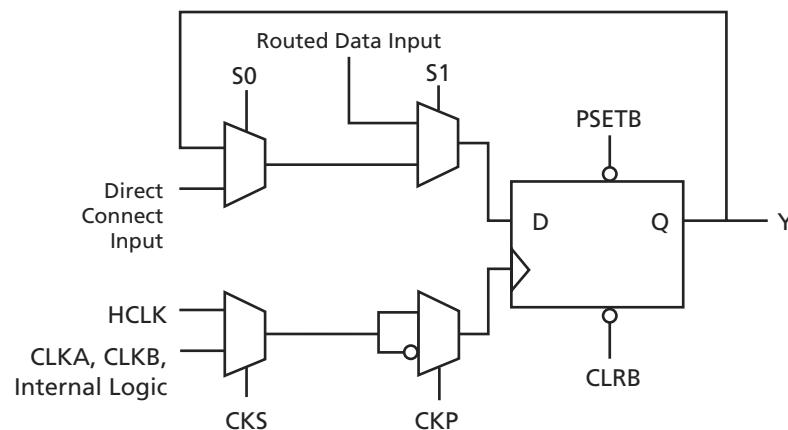*Figure 1-1* • **SX Family Interconnect Elements**

Figure 1-2 • **R-Cell**

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

The Actel high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hardwired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

Other Architectural Features

Technology

The Actel SX family is implemented on a high-voltage twin-well CMOS process using 0.35 µ design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25 Ω with a capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin.

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

Power Requirements

The SX family supports 3.3 V operation and is designed to tolerate 5.0 V inputs. (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest power architecture on the market.

Table 1-1 • **Supply Voltages**

Device	V$_{CCA}$	V$_{CCI}$	V$_{CCR}$	Maximum Input Tolerance	Maximum Output Drive
A54SX08 A54SX16 A54SX32	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
A54SX16-P*	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V

Note: *A54SX16-P has three different entries because it is capable of both a 3.3 V and a 5.0 V drive.*
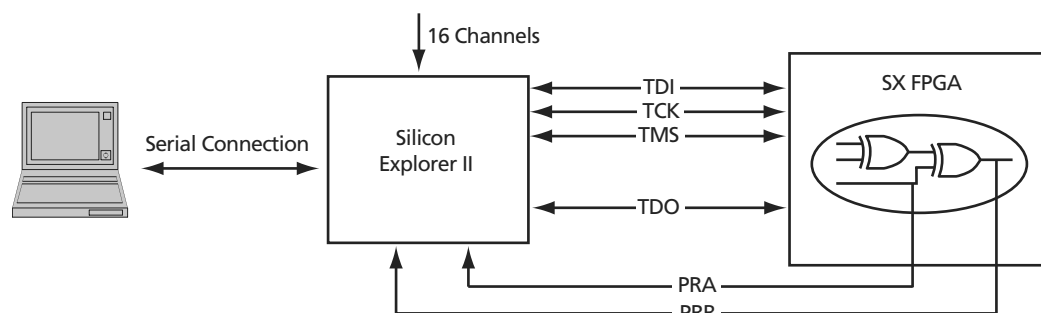
Figure 1-8 • **Probe Setup**

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II are compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an SX device using Silicon Sculptor II are as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming SX devices, refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

3.3 V / 5 V Operating Conditions

Table 1-3 • **Absolute Maximum Ratings[1]**

Symbol	Parameter	Limits	Units
V_{CCR}[2]	DC Supply Voltage[3]	–0.3 to + 6.0	V
V_{CCA}[2]	DC Supply Voltage	–0.3 to + 4.0	V
V_{CCI}[2]	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	–0.3 to + 4.0	V
V_{CCI}[2]	DC Supply Voltage (A54SX16P)	–0.3 to + 6.0	V
V_I	Input Voltage	–0.5 to + 5.5	V
V_O	Output Voltage	–0.5 to + 3.6	V
I_{IO}	I/O Source Sink Current[3]	–30 to + 5.0	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*

2. *V_{CCR} in the A54SX16P must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.*

3. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward-bias and can draw excessive current.*

Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{Total} = P_{DC} + P_{AC}$$

EQ 1-5

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • **Standby Power**

I_{CC}	V_{CC}	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + xV_{OL} \times I_{OL} + y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-6

AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

EQ 1-7

$$P_{AC} = V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + (n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + (0.5 \times (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + (0.5 \times (q2 \times CEQCR \times f_{q2}) + (r2 \times f_{q2}))RCLKB + (0.5 \times (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]$$

EQ 1-8

Definition of Terms Used in Formula

m	=	Number of logic modules switching at f_m
n	=	Number of input buffers switching at f_n
p	=	Number of output buffers switching at f_p
q_1	=	Number of clock loads on the first routed array clock
q_2	=	Number of clock loads on the second routed array clock
x	=	Number of I/Os at logic low
y	=	Number of I/Os at logic high
r_1	=	Fixed capacitance due to first routed array clock
r_2	=	Fixed capacitance due to second routed array clock
s_1	=	Number of clock loads on the dedicated array clock
C_{EQM}	=	Equivalent capacitance of logic modules in pF
C_{EQI}	=	Equivalent capacitance of input buffers in pF
C_{EQO}	=	Equivalent capacitance of output buffers in pF
C_{EQCR}	=	Equivalent capacitance of routed array clock in pF
C_{EQHV}	=	Variable capacitance of dedicated array clock
C_{EQHF}	=	Fixed capacitance of dedicated array clock
C_L	=	Output lead capacitance in pF
f_m	=	Average logic module switching rate in MHz
f_n	=	Average input buffer switching rate in MHz
f_p	=	Average output buffer switching rate in MHz
f_{q1}	=	Average first routed array clock rate in MHz
f_{q2}	=	Average second routed array clock rate in MHz
f_{s1}	=	Average dedicated array clock rate in MHz

Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.
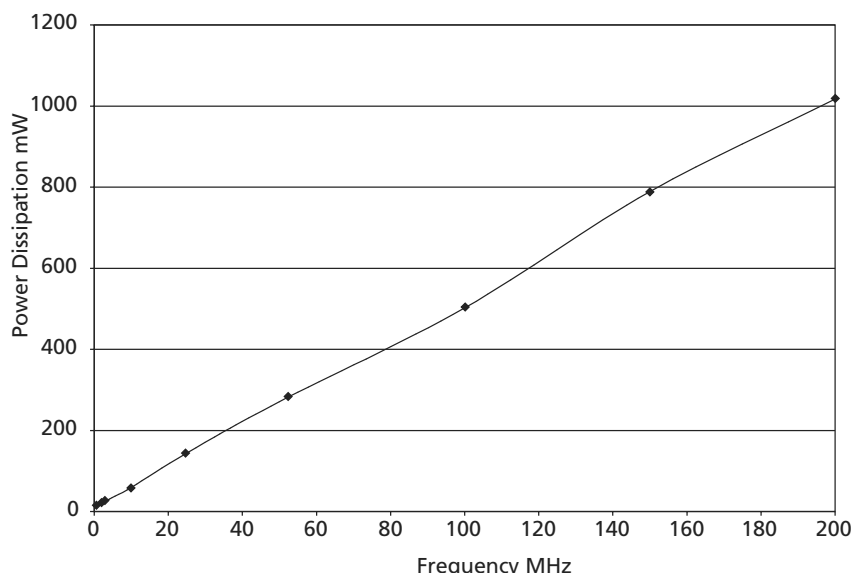
Figure 1-11 • **Power Dissipation**

Junction Temperature (T$_J$)

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

Junction Temperature = $\Delta T + T_a$

EQ 1-13

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} \times P$

P = Power calculated from Estimating Power Consumption section

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150 °C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\ (\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{28\text{°C/W}} = 2.86\ \text{W}$$

EQ 1-14

Register Cell Timing Characteristics
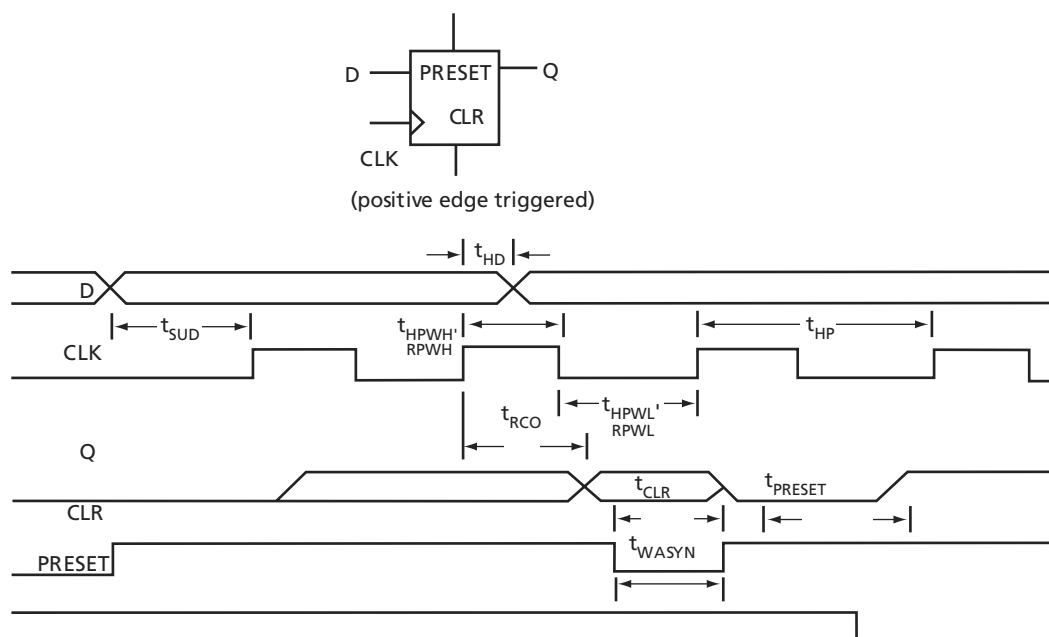
Figure 1-17 • **Flip-Flops**

Timing Characteristics

Timing characteristics for SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO = 24) routing delays in the datasheet specifications section.

Timing Derating

SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	'–3' Speed Min.	'–3' Speed Max.	'–2' Speed Min.	'–2' Speed Max.	'–1' Speed Min.	'–1' Speed Max.	'Std' Speed Min.	'Std' Speed Max.	Units
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance.   Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH}, the loading is 5 pF.*

A54SX16P Timing Characteristics

Table 1-19 • **A54SX16P Timing Characteristics**
   (Worst-Case Commercial Conditions, V$_{CCR}$ = 4.75 V, V$_{CCA}$,V$_{CCI}$ = 3.0 V, T$_J$ = 70°C)

Parameter	Description	'–3' Speed Min.	'–3' Speed Max.	'–2' Speed Min.	'–2' Speed Max.	'–1' Speed Min.	'–1' Speed Max.	'Std' Speed Min.	'Std' Speed Max.	Units
C-Cell Propagation Delays[1]										
t$_{PD}$	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t$_{DC}$	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t$_{FC}$	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t$_{RD1}$	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t$_{RD2}$	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t$_{RD3}$	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t$_{RD4}$	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t$_{RD8}$	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t$_{RD12}$	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t$_{RCO}$	Sequential Clock-to-Q		0.9		1.1		1.3		1.4	ns
t$_{CLR}$	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t$_{PRESET}$	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t$_{SUD}$	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t$_{HD}$	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t$_{WASYN}$	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t$_{INYH}$	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t$_{INYL}$	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t$_{IRD1}$	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t$_{IRD2}$	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t$_{IRD3}$	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t$_{IRD4}$	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t$_{IRD8}$	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t$_{IRD12}$	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t$_{PD}$ + t$_{RD1}$ + t$_{PDn}$, t$_{RCO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

3. *Delays based on 10 pF loading.*

Package Pin Assignments

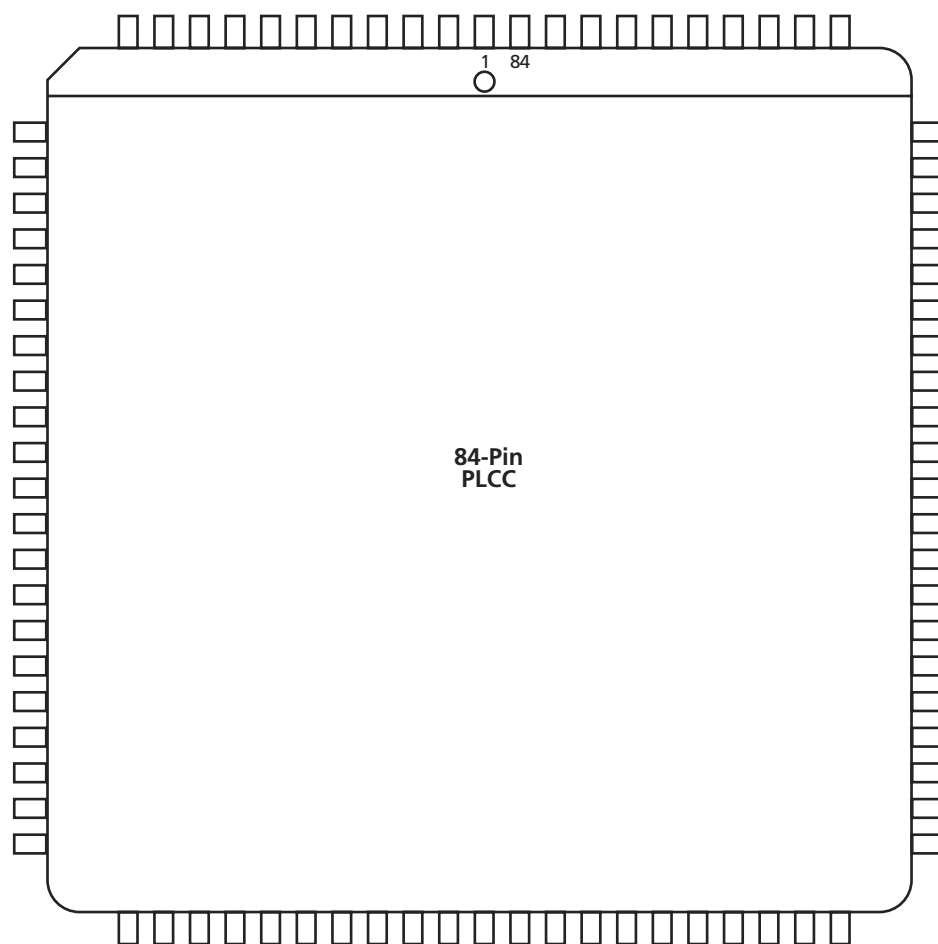## 84-Pin PLCC

Figure 2-1 • **84-Pin PLCC (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at
http://www.actel.com/products/rescenter/package/index.html.

208-Pin PQFP				208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function	Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND	37	I/O	I/O	I/O
2	TDI, I/O	TDI, I/O	TDI, I/O	38	I/O	I/O	I/O
3	I/O	I/O	I/O	39	NC	I/O	I/O
4	NC	I/O	I/O	40	V_{CCI}	V_{CCI}	V_{CCI}
5	I/O	I/O	I/O	41	V_{CCA}	V_{CCA}	V_{CCA}
6	NC	I/O	I/O	42	I/O	I/O	I/O
7	I/O	I/O	I/O	43	I/O	I/O	I/O
8	I/O	I/O	I/O	44	I/O	I/O	I/O
9	I/O	I/O	I/O	45	I/O	I/O	I/O
10	I/O	I/O	I/O	46	I/O	I/O	I/O
11	TMS	TMS	TMS	47	I/O	I/O	I/O
12	V_{CCI}	V_{CCI}	V_{CCI}	48	NC	I/O	I/O
13	I/O	I/O	I/O	49	I/O	I/O	I/O
14	NC	I/O	I/O	50	NC	I/O	I/O
15	I/O	I/O	I/O	51	I/O	I/O	I/O
16	I/O	I/O	I/O	52	GND	GND	GND
17	NC	I/O	I/O	53	I/O	I/O	I/O
18	I/O	I/O	I/O	54	I/O	I/O	I/O
19	I/O	I/O	I/O	55	I/O	I/O	I/O
20	NC	I/O	I/O	56	I/O	I/O	I/O
21	I/O	I/O	I/O	57	I/O	I/O	I/O
22	I/O	I/O	I/O	58	I/O	I/O	I/O
23	NC	I/O	I/O	59	I/O	I/O	I/O
24	I/O	I/O	I/O	60	V_{CCI}	V_{CCI}	V_{CCI}
25	V_{CCR}	V_{CCR}	V_{CCR}	61	NC	I/O	I/O
26	GND	GND	GND	62	I/O	I/O	I/O
27	V_{CCA}	V_{CCA}	V_{CCA}	63	I/O	I/O	I/O
28	GND	GND	GND	64	NC	I/O	I/O
29	I/O	I/O	I/O	65*	I/O	I/O	NC*
30	I/O	I/O	I/O	66	I/O	I/O	I/O
31	NC	I/O	I/O	67	NC	I/O	I/O
32	I/O	I/O	I/O	68	I/O	I/O	I/O
33	I/O	I/O	I/O	69	I/O	I/O	I/O
34	I/O	I/O	I/O	70	NC	I/O	I/O
35	NC	I/O	I/O	71	I/O	I/O	I/O
36	I/O	I/O	I/O	72	I/O	I/O	I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

144-Pin TQFP

Figure 2-3 • **144-Pin TQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at
http://www.actel.com/products/rescenter/package/index.html.

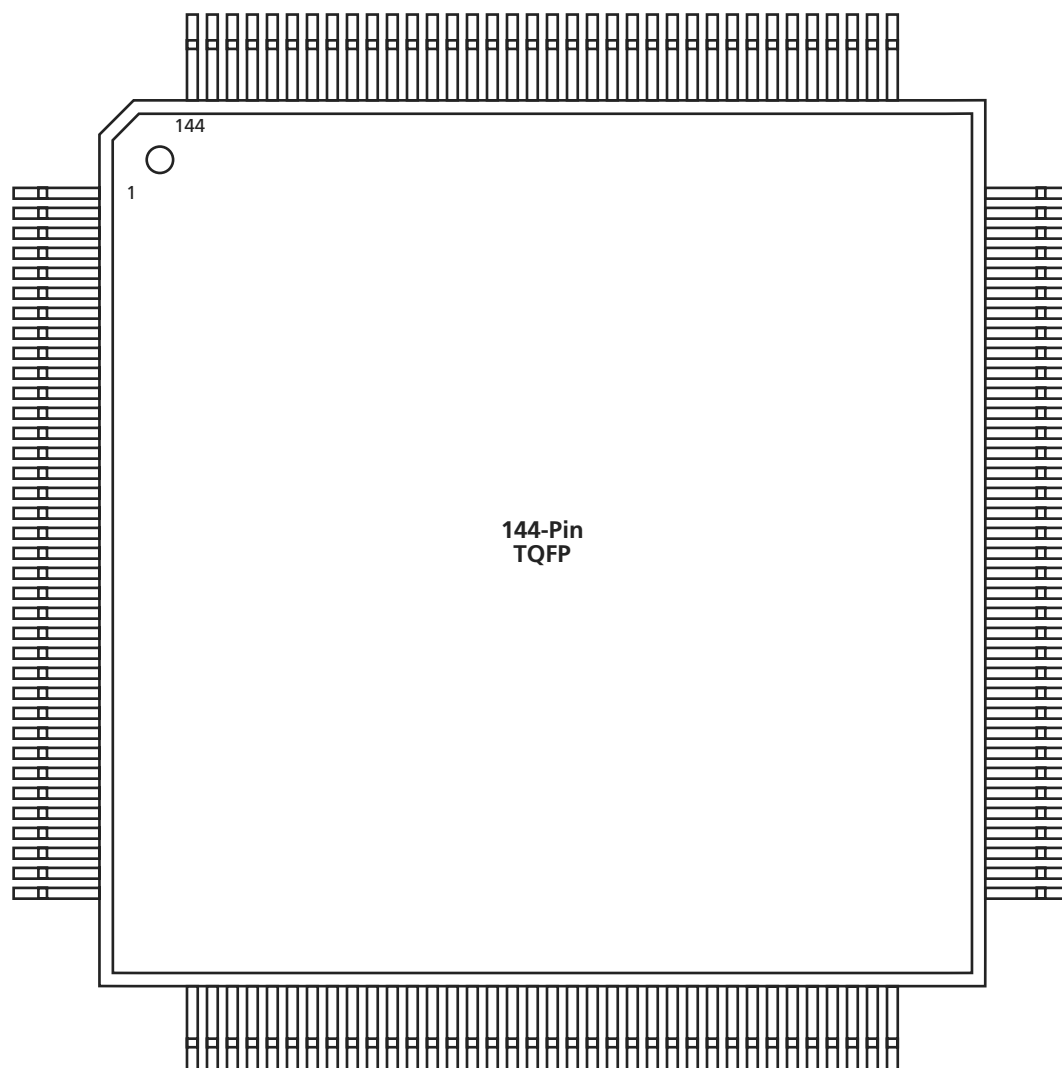| 144-Pin TQFP				144-Pin TQFP			
Pin Number	**A54SX08 Function**	**A54SX16P Function**	**A54SX32 Function**	**Pin Number**	**A54SX08 Function**	**A54SX16P Function**	**A54SX32 Function**
1	GND	GND	GND	37	I/O	I/O	I/O
2	TDI, I/O	TDI, I/O	TDI, I/O	38	I/O	I/O	I/O
3	I/O	I/O	I/O	39	I/O	I/O	I/O
4	I/O	I/O	I/O	40	I/O	I/O	I/O
5	I/O	I/O	I/O	41	I/O	I/O	I/O
6	I/O	I/O	I/O	42	I/O	I/O	I/O
7	I/O	I/O	I/O	43	I/O	I/O	I/O
8	I/O	I/O	I/O	44	V_{CCI}	V_{CCI}	V_{CCI}
9	TMS	TMS	TMS	45	I/O	I/O	I/O
10	V_{CCI}	V_{CCI}	V_{CCI}	46	I/O	I/O	I/O
11	GND	GND	GND	47	I/O	I/O	I/O
12	I/O	I/O	I/O	48	I/O	I/O	I/O
13	I/O	I/O	I/O	49	I/O	I/O	I/O
14	I/O	I/O	I/O	50	I/O	I/O	I/O
15	I/O	I/O	I/O	51	I/O	I/O	I/O
16	I/O	I/O	I/O	52	I/O	I/O	I/O
17	I/O	I/O	I/O	53	I/O	I/O	I/O
18	I/O	I/O	I/O	54	PRB, I/O	PRB, I/O	PRB, I/O
19	V_{CCR}	V_{CCR}	V_{CCR}	55	I/O	I/O	I/O
20	V_{CCA}	V_{CCA}	V_{CCA}	56	V_{CCA}	V_{CCA}	V_{CCA}
21	I/O	I/O	I/O	57	GND	GND	GND
22	I/O	I/O	I/O	58	V_{CCR}	V_{CCR}	V_{CCR}
23	I/O	I/O	I/O	59	I/O	I/O	I/O
24	I/O	I/O	I/O	60	HCLK	HCLK	HCLK
25	I/O	I/O	I/O	61	I/O	I/O	I/O
26	I/O	I/O	I/O	62	I/O	I/O	I/O
27	I/O	I/O	I/O	63	I/O	I/O	I/O
28	GND	GND	GND	64	I/O	I/O	I/O
29	V_{CCI}	V_{CCI}	V_{CCI}	65	I/O	I/O	I/O
30	V_{CCA}	V_{CCA}	V_{CCA}	66	I/O	I/O	I/O
31	I/O	I/O	I/O	67	I/O	I/O	I/O
32	I/O	I/O	I/O	68	V_{CCI}	V_{CCI}	V_{CCI}
33	I/O	I/O	I/O	69	I/O	I/O	I/O
34	I/O	I/O	I/O	70	I/O	I/O	I/O
35	I/O	I/O	I/O	71	TDO, I/O	TDO, I/O	TDO, I/O
36	GND	GND	GND	72	I/O	I/O	I/O

100-Pin VQFP

Figure 2-5 • **100-Pin VQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.
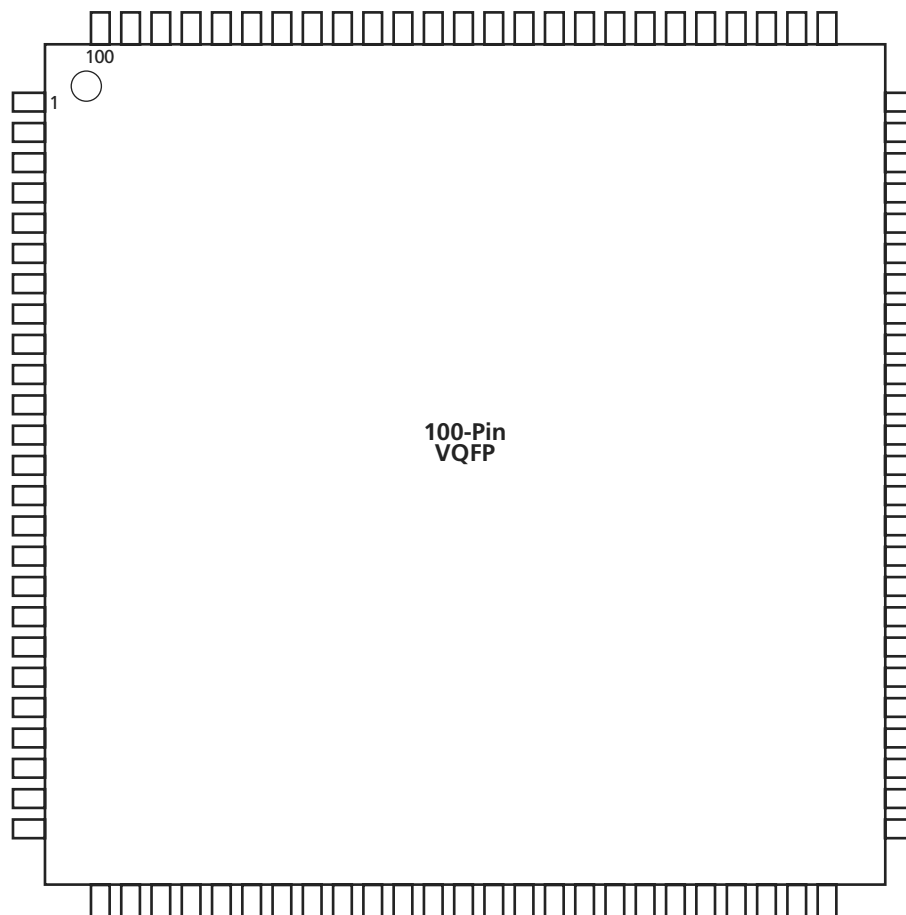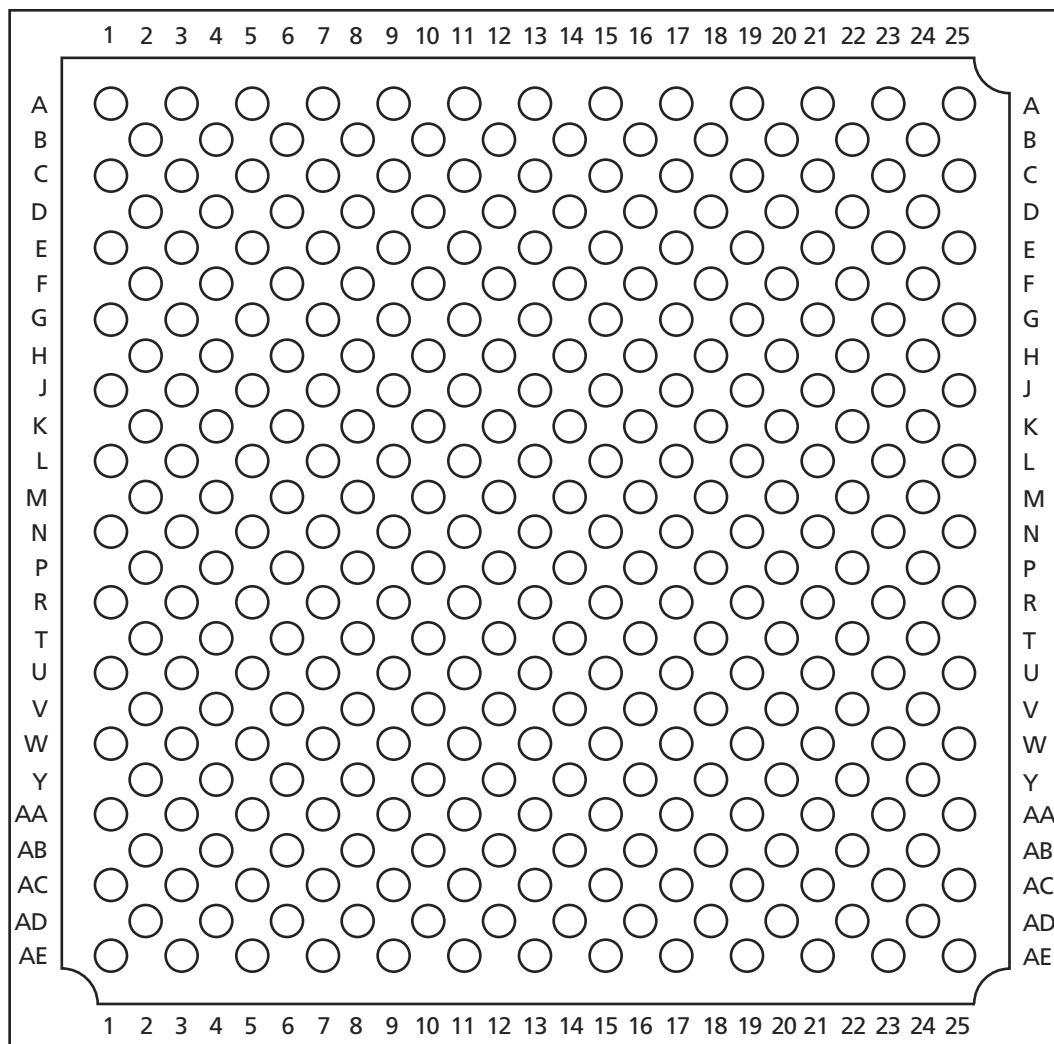
313-Pin PBGA

Figure 2-6 • **313-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

313-Pin PBGA	
Pin Number	A54SX32 Function
A1	GND
A3	NC
A5	I/O
A7	I/O
A9	I/O
A11	I/O
A13	V_{CCR}
A15	I/O
A17	I/O
A19	I/O
A21	I/O
A23	NC
A25	GND
AA1	I/O
AA3	I/O
AA5	NC
AA7	I/O
AA9	NC
AA11	I/O
AA13	I/O
AA15	I/O
AA17	I/O
AA19	I/O
AA21	I/O
AA23	NC
AA25	I/O
AB2	NC
AB4	NC
AB6	I/O
AB8	I/O
AB10	I/O
AB12	I/O
AB14	I/O
AB16	I/O
AB18	V_{CCI}
AB20	NC
AB22	I/O
AB24	I/O
AC1	I/O
AC3	I/O

313-Pin PBGA	
Pin Number	A54SX32 Function
AC5	I/O
AC7	I/O
AC9	I/O
AC11	I/O
AC13	V_{CCR}
AC15	I/O
AC17	I/O
AC19	I/O
AC21	I/O
AC23	I/O
AC25	NC
AD2	GND
AD4	I/O
AD6	V_{CCI}
AD8	I/O
AD10	I/O
AD12	PRB, I/O
AD14	I/O
AD16	I/O
AD18	I/O
AD20	I/O
AD22	NC
AD24	I/O
AE1	NC
AE3	I/O
AE5	I/O
AE7	I/O
AE9	I/O
AE11	I/O
AE13	V_{CCA}
AE15	I/O
AE17	I/O
AE19	I/O
AE21	I/O
AE23	TDO, I/O
AE25	GND
B2	TCK, I/O
B4	I/O
B6	I/O
B8	I/O

313-Pin PBGA	
Pin Number	A54SX32 Function
B10	I/O
B12	I/O
B14	I/O
B16	I/O
B18	I/O
B20	I/O
B22	I/O
B24	I/O
C1	TDI, I/O
C3	I/O
C5	NC
C7	I/O
C9	I/O
C11	I/O
C13	V_{CCI}
C15	I/O
C17	I/O
C19	V_{CCI}
C21	I/O
C23	I/O
C25	NC
D2	I/O
D4	NC
D6	I/O
D8	I/O
D10	I/O
D12	I/O
D14	I/O
D16	I/O
D18	I/O
D20	I/O
D22	I/O
D24	NC
E1	I/O
E3	NC
E5	I/O
E7	I/O
E9	I/O
E11	I/O
E13	V_{CCA}

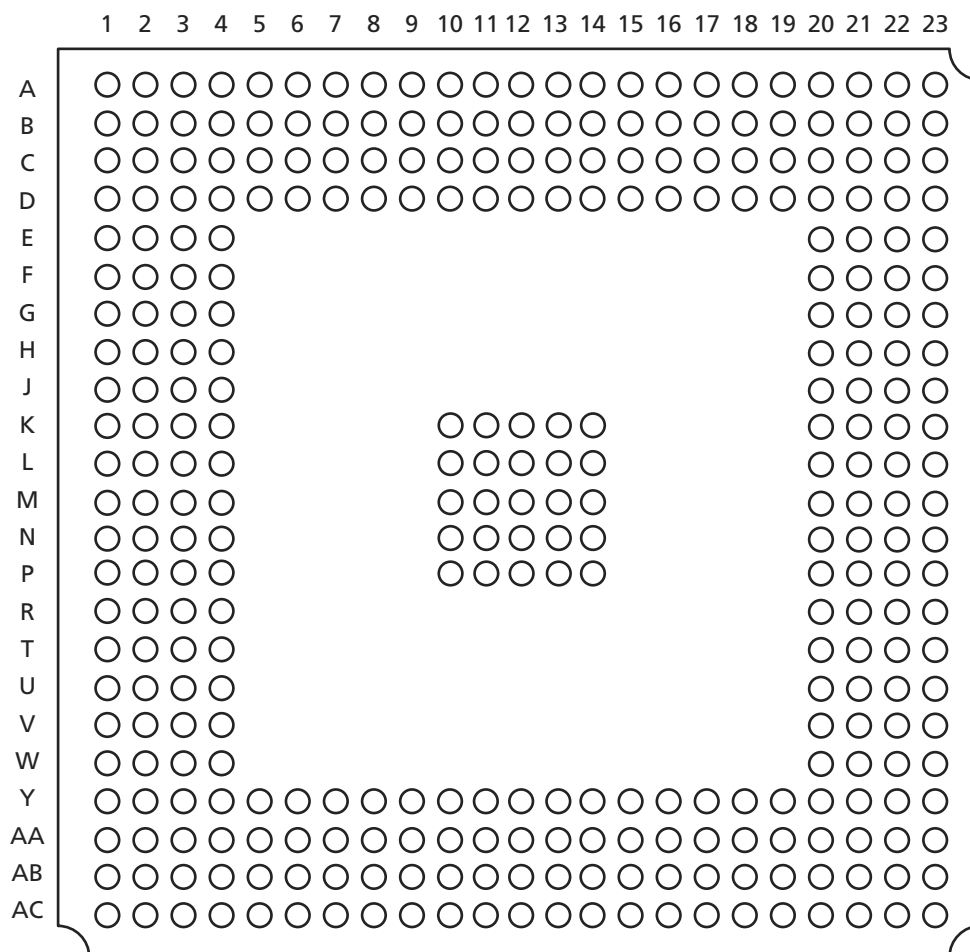| 313-Pin PBGA	
Pin Number	A54SX32 Function
E15	I/O
E17	I/O
E19	I/O
E21	I/O
E23	I/O
E25	I/O
F2	I/O
F4	I/O
F6	NC
F8	I/O
F10	NC
F12	I/O
F14	I/O
F16	NC
F18	I/O
F20	I/O
F22	I/O
F24	I/O
G1	I/O
G3	TMS
G5	I/O
G7	I/O
G9	V_{CCI}
G11	I/O
G13	CLKB
G15	I/O
G17	I/O
G19	I/O
G21	I/O
G23	I/O
G25	I/O
H2	I/O
H4	I/O
H6	I/O
H8	I/O
H10	I/O
H12	PRA, I/O
H14	I/O
H16	I/O
H18	NC

329-Pin PBGA

Figure 2-7 • **329-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at
http://www.actel.com/products/rescenter/package/index.html.

144-Pin FBGA	
Pin Number	A54SX08 Function
A1	I/O
A2	I/O
A3	I/O
A4	I/O
A5	V_{CCA}
A6	GND
A7	CLKA
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
B1	I/O
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	CLKB
B8	I/O
B9	I/O
B10	I/O
B11	GND
B12	I/O
C1	I/O
C2	I/O
C3	TCK, I/O
C4	I/O
C5	I/O
C6	PRA, I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O

144-Pin FBGA	
Pin Number	A54SX08 Function
D1	I/O
D2	V_{CCI}
D3	TDI, I/O
D4	I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	I/O
E1	I/O
E2	I/O
E3	I/O
E4	I/O
E5	TMS
E6	V_{CCI}
E7	V_{CCI}
E8	V_{CCI}
E9	V_{CCA}
E10	I/O
E11	GND
E12	I/O
F1	I/O
F2	I/O
F3	V_{CCR}
F4	I/O
F5	GND
F6	GND
F7	GND
F8	V_{CCI}
F9	I/O
F10	GND
F11	I/O
F12	I/O

144-Pin FBGA	
Pin Number	A54SX08 Function
G1	I/O
G2	GND
G3	I/O
G4	I/O
G5	GND
G6	GND
G7	GND
G8	V_{CCI}
G9	I/O
G10	I/O
G11	I/O
G12	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H5	V_{CCA}
H6	V_{CCA}
H7	V_{CCI}
H8	V_{CCI}
H9	V_{CCA}
H10	I/O
H11	I/O
H12	V_{CCR}
J1	I/O
J2	I/O
J3	I/O
J4	I/O
J5	I/O
J6	PRB, I/O
J7	I/O
J8	I/O
J9	I/O
J10	I/O
J11	I/O
J12	V_{CCA}

144-Pin FBGA	
Pin Number	A54SX08 Function
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K5	I/O
K6	I/O
K7	GND
K8	I/O
K9	I/O
K10	GND
K11	I/O
K12	I/O
L1	GND
L2	I/O
L3	I/O
L4	I/O
L5	I/O
L6	I/O
L7	HCLK
L8	I/O
L9	I/O
L10	I/O
L11	I/O
L12	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M5	I/O
M6	I/O
M7	V_{CCA}
M8	I/O
M9	I/O
M10	I/O
M11	TDO, I/O
M12	I/O