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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1452 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 113 |
| Number of Gates | 24000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a54sx16p-1tqg144 |

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## Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect,* which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

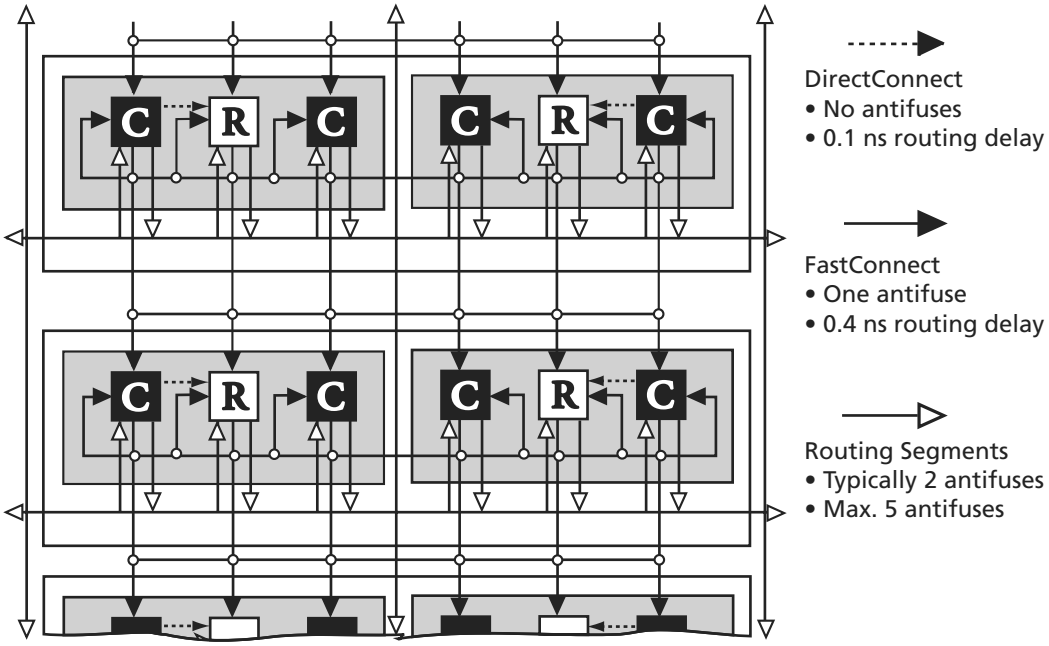


*Figure 1-5* • **DirectConnect and FastConnect for Type 1 SuperClusters**

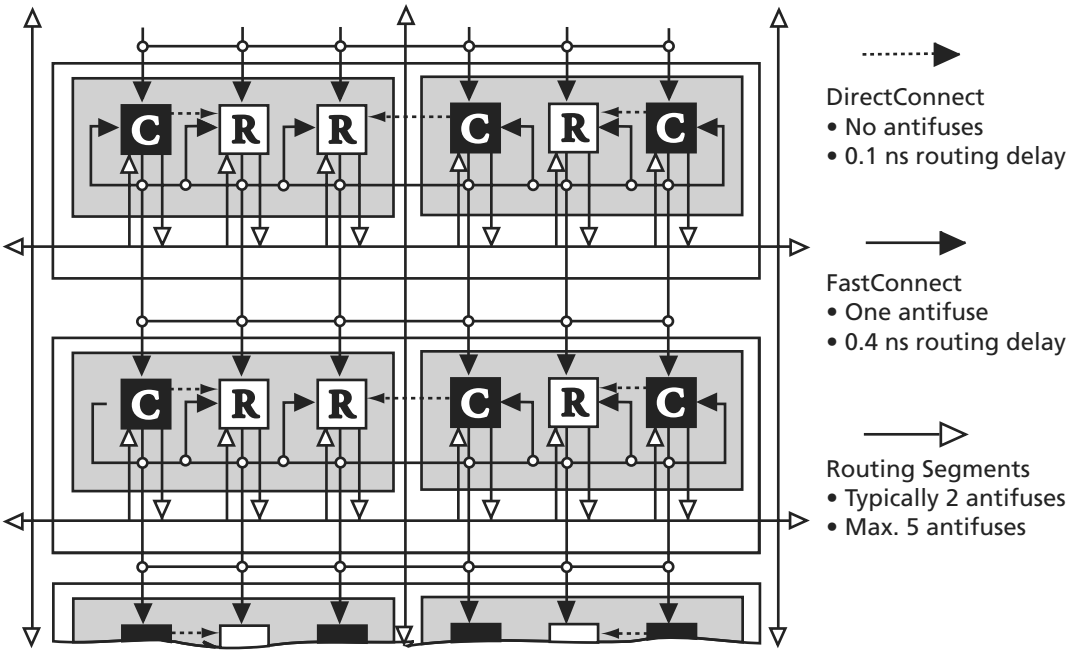


*Figure 1-6* • **DirectConnect and FastConnect for Type 2 SuperClusters**

## Boundary Scan Testing (BST)

All SX devices are IEEE 1149.1 compliant. SX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 1-2. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10 kΩ. TMS can be pulled LOW to initiate the test sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

*Table 1-2* • **Boundary Scan Pin Functionality**

| **Program Fuse Blown (Dedicated Test Mode)** | **Program Fuse Not Blown (Flexible Mode)** |
|---|---|
| TCK, TDI, TDO are dedicated BST pins. | TCK, TDI, TDO are flexible and may be used as I/Os. |
| No need for pull-up resistor for TMS | Use a pull-up resistor of 10 kΩ on TMS. |

## Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software by checking the "Reserve JTAG" box in "Device Selection Wizard" (Figure 1-7). JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the Table 1-5 on page 1-8 for detailed specifications.

*Figure 1-7* • **Device Selection Wizard**

## Development Tool Support

The SX family of FPGAs is fully supported by both the Actel Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the Libero IDE flow diagram (located on the Actel website) for more information.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators, and the simulation results can be cross-probed with Silicon Explorer II, Actel integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Actel Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys®, and Cadence® Design Systems. The Designer software is available for both the Windows® and UNIX® operating systems.

## Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-8 on page 1-7 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

## Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuitry.

*Table 1-4 •* **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature Range* | 0 to + 70 | –40 to + 85 | –55 to +125 | °C |
| 3.3 V Power Supply Tolerance | ±10 | ±10 | ±10 | %$V_{CC}$ |
| 5.0 V Power Supply Tolerance | ±5 | ±10 | ±10 | %$V_{CC}$ |

***Note:*** **Ambient temperature ($T_A$) is used for commercial and industrial; case temperature ($T_C$) is used for military.*

*Table 1-5 •* **Electrical Specifications**

| | | Commercial | | Industrial | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $V_{OH}$ | ($I_{OH}$ = –20 µA) (CMOS)<br>($I_{OH}$ = –8 mA) (TTL)<br>($I_{OH}$ = –6 mA) (TTL) | ($V_{CCI}$ – 0.1)<br>2.4 | $V_{CCI}$<br>$V_{CCI}$ | ($V_{CCI}$ – 0.1)<br><br>2.4 | $V_{CCI}$<br><br>$V_{CCI}$ | V |
| $V_{OL}$ | ($I_{OL}$= 20 µA) (CMOS)<br>($I_{OL}$ = 12 mA) (TTL)<br>($I_{OL}$ = 8 mA) (TTL) | | 0.10<br>0.50 | | <br><br>0.50 | V |
| $V_{IL}$ | | | 0.8 | | 0.8 | V |
| $V_{IH}$ | | 2.0 | | 2.0 | | V |
| $t_R$, $t_F$ | Input Transition Time $t_R$, $t_F$ | | 50 | | 50 | ns |
| $C_{IO}$ | $C_{IO}$ I/O Capacitance | | 10 | | 10 | pF |
| $I_{CC}$ | Standby Current, $I_{CC}$ | | 4.0 | | 4.0 | mA |
| $I_{CC(D)}$ | $I_{CC(D)}$ $I_{Dynamic}$ $V_{CC}$ Supply Current | See "Evaluating Power in SX Devices" on page 1-16. | | | | |

Figure 1-10 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

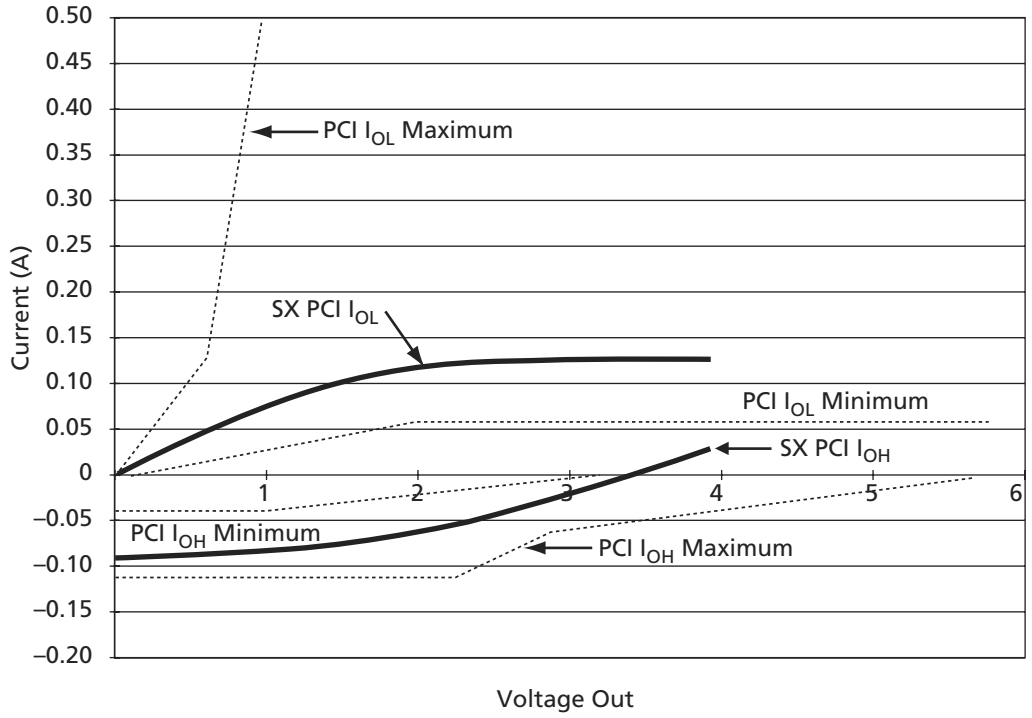


*Figure 1-10* • **3.3 V PCI Curve for A54SX16P Device**

$$I_{OH} = (98.0/V_{CC}) \times (V_{OUT} - V_{CC}) \times (V_{OUT} + 0.4V_{CC})$$
$$\text{for } V_{CC} > V_{OUT} > 0.7\ V_{CC} \qquad \textit{EQ 1-3}$$

$$I_{OL} = (256/V_{CC}) \times V_{OUT} \times (V_{CC} - V_{OUT})$$
$$\text{for } 0\ V < V_{OUT} < 0.18\ V_{CC} \qquad \textit{EQ 1-4}$$

# Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

## Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{Total} = P_{DC} + P_{AC}$$

*EQ 1-5*

## DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

*Table 1-12* • **Standby Power**

| $I_{CC}$ | $V_{CC}$ | Power |
|---|---|---|
| 4 mA | 3.6 V | 14.4 mW |

The DC power dissipation is defined in EQ 1-6.

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + xV_{OL} \times I_{OL} + y(V_{CCI} - V_{OH}) \times V_{OH}$$

*EQ 1-6*

## AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

*EQ 1-7*

$$P_{AC} = V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + (n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + (0.5 \times (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + (0.5 \times (q2 \times CEQCR \times f_{q2}) + (r2 \times f_{q2}))RCLKB + (0.5 \times (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]$$

*EQ 1-8*

### Definition of Terms Used in Formula

$m$ = Number of logic modules switching at $f_m$
$n$ = Number of input buffers switching at $f_n$
$p$ = Number of output buffers switching at $f_p$
$q_1$ = Number of clock loads on the first routed array clock
$q_2$ = Number of clock loads on the second routed array clock
$x$ = Number of I/Os at logic low
$y$ = Number of I/Os at logic high
$r_1$ = Fixed capacitance due to first routed array clock
$r_2$ = Fixed capacitance due to second routed array clock
$s_1$ = Number of clock loads on the dedicated array clock
$C_{EQM}$ = Equivalent capacitance of logic modules in pF
$C_{EQI}$ = Equivalent capacitance of input buffers in pF
$C_{EQO}$ = Equivalent capacitance of output buffers in pF
$C_{EQCR}$ = Equivalent capacitance of routed array clock in pF
$C_{EQHV}$ = Variable capacitance of dedicated array clock
$C_{EQHF}$ = Fixed capacitance of dedicated array clock
$C_L$ = Output lead capacitance in pF
$f_m$ = Average logic module switching rate in MHz
$f_n$ = Average input buffer switching rate in MHz
$f_p$ = Average output buffer switching rate in MHz
$f_{q1}$ = Average first routed array clock rate in MHz
$f_{q2}$ = Average second routed array clock rate in MHz
$f_{s1}$ = Average dedicated array clock rate in MHz

Table 1-13 shows capacitance values for various devices.

*Table 1-13* • **Capacitance Values for Devices**

| | A54SX08 | A54SX16 | A54SX16P | A54SX32 |
|---|---|---|---|---|
| $C_{EQM}$ (pF) | 4.0 | 4.0 | 4.0 | 4.0 |
| $C_{EQI}$ (pF) | 3.4 | 3.4 | 3.4 | 3.4 |
| $C_{EQO}$ (pF) | 4.7 | 4.7 | 4.7 | 4.7 |
| $C_{EQCR}$ (pF) | 1.6 | 1.6 | 1.6 | 1.6 |
| $C_{EQHV}$ | 0.615 | 0.615 | 0.615 | 0.615 |
| $C_{EQHF}$ | 60 | 96 | 96 | 140 |
| $r_1$ (pF) | 87 | 138 | 138 | 171 |
| $r_2$ (pF) | 87 | 138 | 138 | 171 |

## Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

## Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A54SX16P device. A pattern of 0101… was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101… caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

*Table 1-14* • **Power Consumption Guidelines**

| Description | Power Consumption Guideline |
|---|---|
| Logic Modules (m) | 20% of modules |
| Inputs Switching (n) | # inputs/4 |
| Outputs Switching (p) | # outputs/4 |
| First Routed Array Clock Loads ($q_1$) | 20% of register cells |
| Second Routed Array Clock Loads ($q_2$) | 20% of register cells |
| Load Capacitance ($C_L$) | 35 pF |
| Average Logic Module Switching Rate ($f_m$) | f/10 |
| Average Input Switching Rate ($f_n$) | f/5 |
| Average Output Switching Rate ($f_p$) | f/10 |
| Average First Routed Array Clock Rate ($f_{q1}$) | f/2 |
| Average Second Routed Array Clock Rate ($f_{q2}$) | f/2 |
| Average Dedicated Array Clock Rate ($f_{s1}$) | f |
| Dedicated Clock Array Clock Loads ($s_1$) | 20% of regular modules |

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{Total} = P_{AC} \text{ (dynamic power)} + P_{DC} \text{ (static power)}$$

*EQ 1-9*

## AC Power Dissipation

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

*EQ 1-10*

$$P_{AC} = V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + (n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + (0.5\ (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + (0.5\ (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2}))_{RCLKB} + (0.5\ (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]$$

*EQ 1-11*

Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.

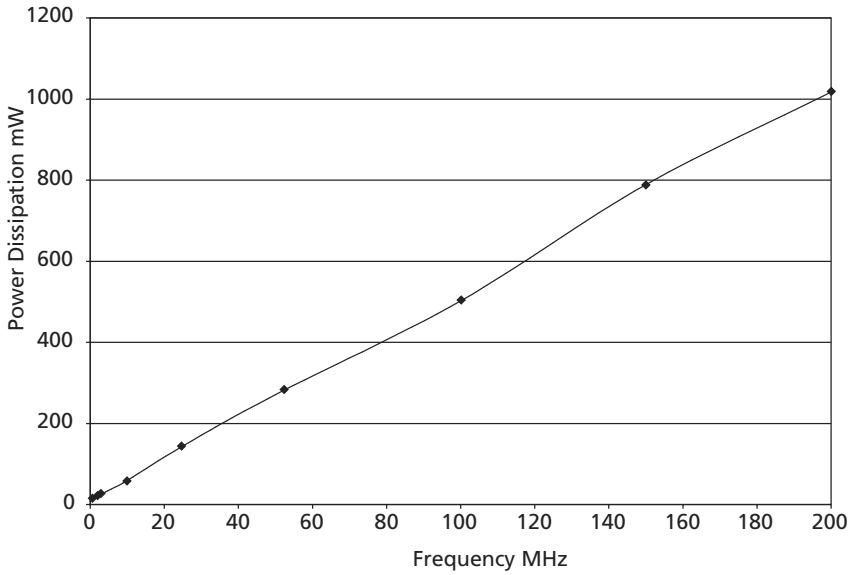


*Figure 1-11* • **Power Dissipation**

## Junction Temperature ($T_J$)

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a$$

*EQ 1-13*

Where:

$T_a$ = Ambient Temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} \times P$

P = Power calculated from Estimating Power Consumption section

$\theta_{ja}$ = Junction to ambient of package. $\theta_{ja}$ numbers are located in the "Package Thermal Characteristics" section.

### Package Thermal Characteristics

The device junction to case thermal characteristic is $\theta_{jc}$, and the junction to ambient air characteristic is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown with two different air flow rates.

The maximum junction temperature is 150 °C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{ (°C/W)}} = \frac{150°C - 70°C}{28°C/W} = 2.86\text{ W}$$

*EQ 1-14*

## A54SX08 Timing Characteristics

*Table 1-17* • **A54SX08 Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCR}$ = 4.75 V, $V_{CCA}$,$V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | '–3' Speed | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[1]** | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| **Predicted Routing Delays[2]** | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |
| **R-Cell Timing** | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.8 | | 1.1 | | 1.2 | | 1.4 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.0 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.5 | | 0.5 | | 0.7 | | 0.8 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y HIGH | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y LOW | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |

***Note:***

1. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$, $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$, or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

*Table 1-17* • **A54SX08 Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCR}$ = 4.75 V, $V_{CCA}$,$V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | '–3' Speed | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Network** | | | | | | | | | | |
| $t_{HCKH}$ | Input LOW to HIGH (pad to R-Cell input) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | ns |
| $t_{HCKL}$ | Input HIGH to LOW (pad to R-Cell input) | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| $t_{HPWH}$ | Minimum Pulse Width HIGH | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width LOW | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.1 | | 0.2 | | 0.2 | | 0.2 | ns |
| $t_{HP}$ | Minimum Period | 2.7 | | 3.1 | | 3.6 | | 4.2 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 350 | | 320 | | 280 | | 240 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input LOW to HIGH (light load) (pad to R-Cell input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (light load) (pad to R-Cell Input) | | 1.4 | | 1.6 | | 1.8 | | 2.1 | ns |
| $t_{RCKH}$ | Input LOW to HIGH (50% load) (pad to R-Cell input) | | 1.4 | | 1.7 | | 1.9 | | 2.2 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (50% load) (pad to R-Cell input) | | 1.5 | | 1.7 | | 2.0 | | 2.3 | ns |
| $t_{RCKH}$ | Input LOW to HIGH (100% load) (pad to R-Cell input) | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (100% load) (pad to R-Cell input) | | 1.5 | | 1.8 | | 2.0 | | 2.3 | ns |
| $t_{RPWH}$ | Min. Pulse Width HIGH | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| $t_{RPWL}$ | Min. Pulse Width LOW | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (light load) | | 0.1 | | 0.2 | | 0.2 | | 0.2 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% load) | | 0.3 | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% load) | | 0.3 | | 0.3 | | 0.4 | | 0.4 | ns |
| **TTL Output Module Timing1** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.8 | | 3.2 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.3 | | 2.7 | | 3.1 | | 3.6 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 1.4 | | 1.7 | | 1.9 | | 2.2 | ns |

***Note:***

1. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$, $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$, or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

*Table 1-19* • **A54SX16P Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCR}$ = 4.75 V, $V_{CCA}$,$V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | '–3' Speed | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Network** | | | | | | | | | | |
| $t_{HCKH}$ | Input LOW to HIGH (pad to R-Cell input) | | 1.2 | | 1.4 | | 1.5 | | 1.8 | ns |
| $t_{HCKL}$ | Input HIGH to LOW (pad to R-Cell input) | | 1.2 | | 1.4 | | 1.6 | | 1.9 | ns |
| $t_{HPWH}$ | Minimum Pulse Width HIGH | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width LOW | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.2 | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{HP}$ | Minimum Period | 2.7 | | 3.1 | | 3.6 | | 4.2 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 350 | | 320 | | 280 | | 240 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input LOW to HIGH (light load) (pad to R-Cell input) | | 1.6 | | 1.8 | | 2.1 | | 2.5 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (Light Load) (pad to R-Cell input) | | 1.8 | | 2.0 | | 2.3 | | 2.7 | ns |
| $t_{RCKH}$ | Input LOW to HIGH (50% load) (pad to R-Cell input) | | 1.8 | | 2.1 | | 2.5 | | 2.8 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (50% load) (pad to R-Cell input) | | 2.0 | | 2.2 | | 2.5 | | 3.0 | ns |
| $t_{RCKH}$ | Input LOW to HIGH (100% load) (pad to R-Cell input) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (100% load) (pad to R-Cell input) | | 2.0 | | 2.2 | | 2.5 | | 3.0 | ns |
| $t_{RPWH}$ | Min. Pulse Width HIGH | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| $t_{RPWL}$ | Min. Pulse Width LOW | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (light load) | | 0.5 | | 0.5 | | 0.5 | | 0.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% load) | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% load) | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| **TTL Output Module Timing** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 2.4 | | 2.8 | | 3.1 | | 3.7 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 2.3 | | 2.9 | | 3.2 | | 3.8 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 3.0 | | 3.4 | | 3.9 | | 4.6 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.3 | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.3 | | 2.7 | | 3.0 | | 3.5 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |

***Note:***

1. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$, $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$, or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 10 pF loading.*

*Table 1-19* • **A54SX16P Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCR}$ = 4.75 V, $V_{CCA}$,$V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | '–3' Speed | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **TTL/PCI Output Module Timing** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 1.5 | | 1.7 | | 2.0 | | 2.3 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 1.9 | | 2.2 | | 2.4 | | 2.9 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.3 | | 2.6 | | 3.0 | | 3.5 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 1.5 | | 1.7 | | 1.9 | | 2.3 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.7 | | 3.1 | | 3.5 | | 4.1 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | ns |
| **PCI Output Module Timing[3]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 1.8 | | 2.0 | | 2.3 | | 2.7 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 1.7 | | 2.0 | | 2.2 | | 2.6 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 0.8 | | 1.0 | | 1.1 | | 1.3 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 1.2 | | 1.2 | | 1.5 | | 1.8 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 1.0 | | 1.1 | | 1.3 | | 1.5 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 1.1 | | 1.3 | | 1.5 | | 1.7 | ns |
| **TTL Output Module Timing** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 2.1 | | 2.5 | | 2.8 | | 3.3 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 2.0 | | 2.3 | | 2.6 | | 3.1 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.5 | | 2.9 | | 3.2 | | 3.8 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.0 | | 3.5 | | 3.9 | | 4.6 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.3 | | 2.7 | | 3.1 | | 3.6 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | ns |

***Note:***

1. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$, $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$, or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 10 pF loading.*

## Pin Description

**CLKA/B Clock A and B**

These pins are 3.3 V / 5.0 V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as bidirectional.)

**GND Ground**

LOW supply voltage.

**HCLK Dedicated (hardwired) Array Clock**

This pin is the 3.3 V / 5.0 V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

**I/O Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3 V PCI or 5.0 V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

**NC No Connection**

This pin is not connected to circuitry within the device.

**PRA, I/O Probe A**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

**PRB, I/O Probe B**

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

**TCK Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDI Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDO Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TMS Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-2 on page 1-6). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

**$V_{CCI}$ Supply Voltage**

Supply voltage for I/Os. See Table 1-1 on page 1-5.

**$V_{CCA}$ Supply Voltage**

Supply voltage for Array. See Table 1-1 on page 1-5.

**$V_{CCR}$ Supply Voltage**

Supply voltage for input tolerance (required for internal biasing). See Table 1-1 on page 1-5.

| 208-Pin PQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08 Function** | **A54SX16, A54SX16P Function** | **A54SX32 Function** |
| 73 | NC | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | NC | I/O | I/O |
| 76 | PRB, I/O | PRB, I/O | PRB, I/O |
| 77 | GND | GND | GND |
| 78 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 79 | GND | GND | GND |
| 80 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 81 | I/O | I/O | I/O |
| 82 | HCLK | HCLK | HCLK |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | NC | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | NC | I/O | I/O |
| 89 | I/O | I/O | I/O |
| 90 | I/O | I/O | I/O |
| 91 | NC | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | NC | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | NC | I/O | I/O |
| 98 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 99 | I/O | I/O | I/O |
| 100 | I/O | I/O | I/O |
| 101 | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O |
| 103 | TDO, I/O | TDO, I/O | TDO, I/O |
| 104 | I/O | I/O | I/O |
| 105 | GND | GND | GND |
| 106 | NC | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | NC | I/O | I/O |

| 208-Pin PQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08 Function** | **A54SX16, A54SX16P Function** | **A54SX32 Function** |
| 109 | I/O | I/O | I/O |
| 110 | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | NC | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | NC | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | NC | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | NC | I/O | I/O |
| 126 | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | GND | GND | GND |
| 130 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 131 | GND | GND | GND |
| 132 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | NC | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | NC | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | I/O | I/O | I/O |
| 141 | NC | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | NC | I/O | I/O |
| 144 | I/O | I/O | I/O |

***Note:*** ** Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

| 208-Pin PQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08 Function** | **A54SX16, A54SX16P Function** | **A54SX32 Function** |
| 145 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 146 | GND | GND | GND |
| 147 | I/O | I/O | I/O |
| 148 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 149 | I/O | I/O | I/O |
| 150 | I/O | I/O | I/O |
| 151 | I/O | I/O | I/O |
| 152 | I/O | I/O | I/O |
| 153 | I/O | I/O | I/O |
| 154 | I/O | I/O | I/O |
| 155 | NC | I/O | I/O |
| 156 | NC | I/O | I/O |
| 157 | GND | GND | GND |
| 158 | I/O | I/O | I/O |
| 159 | I/O | I/O | I/O |
| 160 | I/O | I/O | I/O |
| 161 | I/O | I/O | I/O |
| 162 | I/O | I/O | I/O |
| 163 | I/O | I/O | I/O |
| 164 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 165 | I/O | I/O | I/O |
| 166 | I/O | I/O | I/O |
| 167 | NC | I/O | I/O |
| 168 | I/O | I/O | I/O |
| 169 | I/O | I/O | I/O |
| 170 | NC | I/O | I/O |
| 171 | I/O | I/O | I/O |
| 172 | I/O | I/O | I/O |
| 173 | NC | I/O | I/O |
| 174 | I/O | I/O | I/O |
| 175 | I/O | I/O | I/O |
| 176 | NC | I/O | I/O |
| 177 | I/O | I/O | I/O |
| 178 | I/O | I/O | I/O |
| 179 | I/O | I/O | I/O |
| 180 | CLKA | CLKA | CLKA |

| 208-Pin PQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08 Function** | **A54SX16, A54SX16P Function** | **A54SX32 Function** |
| 181 | CLKB | CLKB | CLKB |
| 182 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 183 | GND | GND | GND |
| 184 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 185 | GND | GND | GND |
| 186 | PRA, I/O | PRA, I/O | PRA, I/O |
| 187 | I/O | I/O | I/O |
| 188 | I/O | I/O | I/O |
| 189 | NC | I/O | I/O |
| 190 | I/O | I/O | I/O |
| 191 | I/O | I/O | I/O |
| 192 | NC | I/O | I/O |
| 193 | I/O | I/O | I/O |
| 194 | I/O | I/O | I/O |
| 195 | NC | I/O | I/O |
| 196 | I/O | I/O | I/O |
| 197 | I/O | I/O | I/O |
| 198 | NC | I/O | I/O |
| 199 | I/O | I/O | I/O |
| 200 | I/O | I/O | I/O |
| 201 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 202 | NC | I/O | I/O |
| 203 | NC | I/O | I/O |
| 204 | I/O | I/O | I/O |
| 205 | NC | I/O | I/O |
| 206 | I/O | I/O | I/O |
| 207 | I/O | I/O | I/O |
| 208 | TCK, I/O | TCK, I/O | TCK, I/O |

***Note:*** ** Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

| 144-Pin TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08 Function** | **A54SX16P Function** | **A54SX32 Function** |
| 73 | GND | GND | GND |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 80 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 81 | GND | GND | GND |
| 82 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | I/O |
| 89 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 90 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 99 | GND | GND | GND |
| 100 | I/O | I/O | I/O |
| 101 | GND | GND | GND |
| 102 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 103 | I/O | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08 Function** | **A54SX16P Function** | **A54SX32 Function** |
| 109 | GND | GND | GND |
| 110 | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | I/O | I/O | I/O |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | CLKA | CLKA | CLKA |
| 126 | CLKB | CLKB | CLKB |
| 127 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 128 | GND | GND | GND |
| 129 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 130 | I/O | I/O | I/O |
| 131 | PRA, I/O | PRA, I/O | PRA, I/O |
| 132 | I/O | I/O | I/O |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | TCK, I/O | TCK, I/O | TCK, I/O |

| 176-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 69 | HCLK | HCLK | HCLK |
| 70 | I/O | I/O | I/O |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | NC | I/O | I/O |
| 80 | I/O | I/O | I/O |
| 81 | NC | I/O | I/O |
| 82 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | TDO, I/O | TDO, I/O | TDO, I/O |
| 88 | I/O | I/O | I/O |
| 89 | GND | GND | GND |
| 90 | NC | I/O | I/O |
| 91 | NC | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 99 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 100 | I/O | I/O | I/O |
| 101 | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O |

| 176-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 103 | I/O | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | GND | GND | GND |
| 109 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 110 | GND | GND | GND |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | I/O | I/O | I/O |
| 115 | I/O | I/O | I/O |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | NC | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | NC | I/O | I/O |
| 121 | NC | I/O | I/O |
| 122 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 123 | GND | GND | GND |
| 124 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 125 | I/O | I/O | I/O |
| 126 | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | I/O | I/O | I/O |
| 130 | I/O | I/O | I/O |
| 131 | NC | I/O | I/O |
| 132 | NC | I/O | I/O |
| 133 | GND | GND | GND |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O |

# 313-Pin PBGA

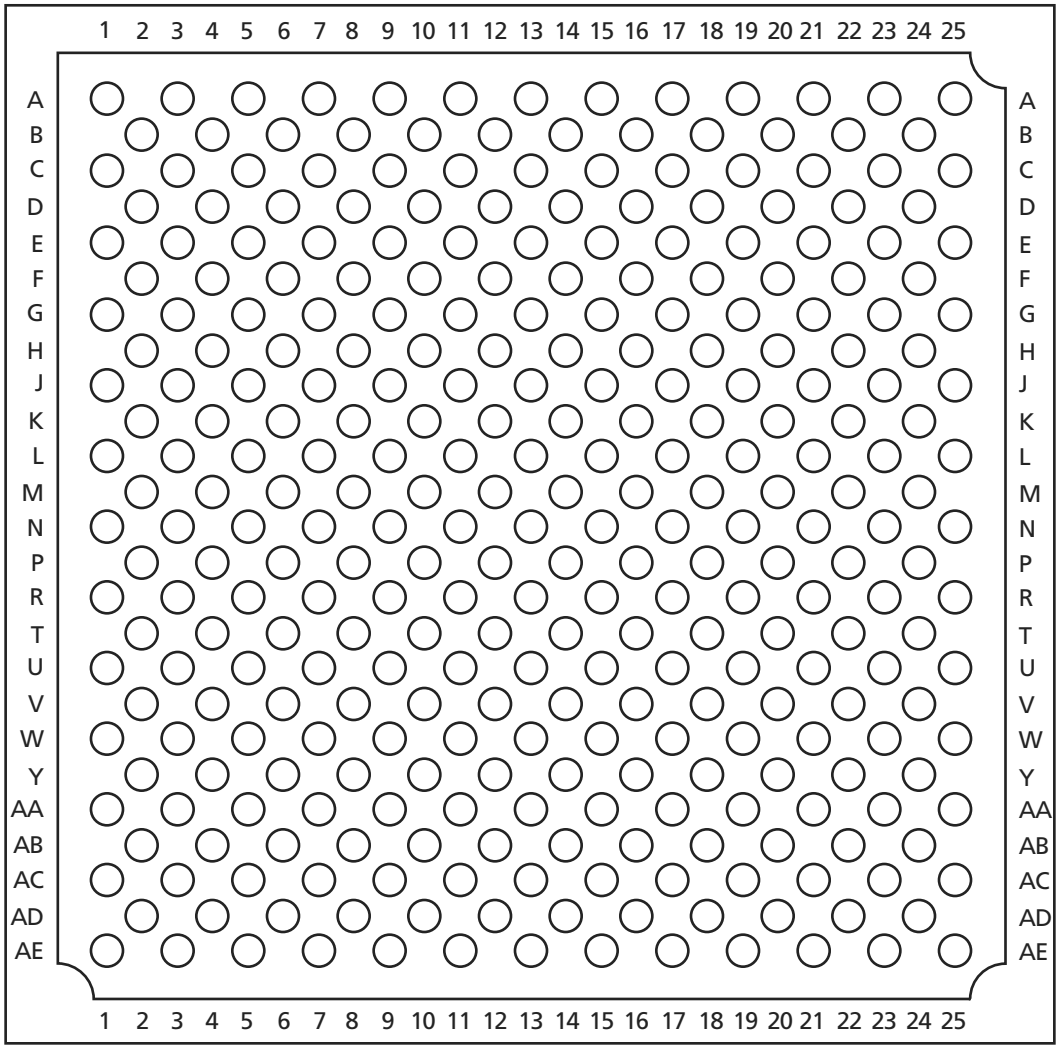


*Figure 2-6* • **313-Pin PBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

# 329-Pin PBGA

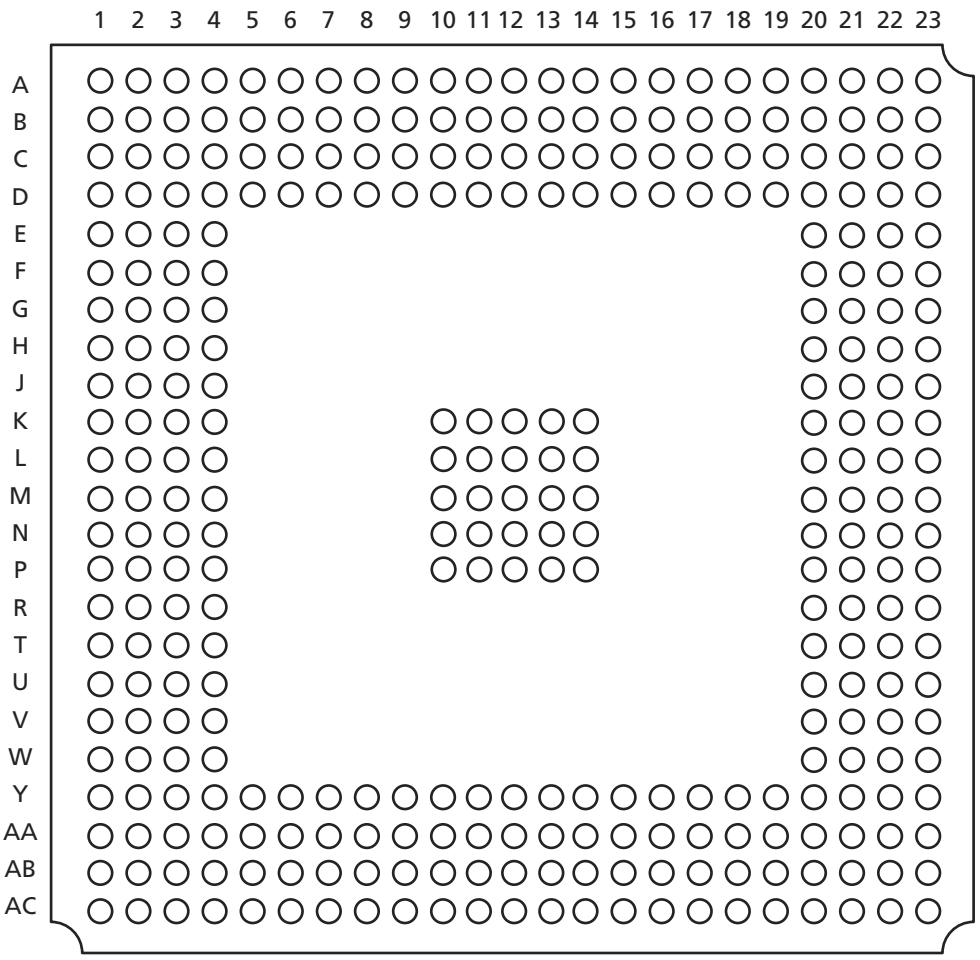


*Figure 2-7* • **329-Pin PBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 144-Pin FBGA | |
|---|---|
| **Pin Number** | **A54SX08 Function** |
| A1 | I/O |
| A2 | I/O |
| A3 | I/O |
| A4 | I/O |
| A5 | $V_{CCA}$ |
| A6 | GND |
| A7 | CLKA |
| A8 | I/O |
| A9 | I/O |
| A10 | I/O |
| A11 | I/O |
| A12 | I/O |
| B1 | I/O |
| B2 | GND |
| B3 | I/O |
| B4 | I/O |
| B5 | I/O |
| B6 | I/O |
| B7 | CLKB |
| B8 | I/O |
| B9 | I/O |
| B10 | I/O |
| B11 | GND |
| B12 | I/O |
| C1 | I/O |
| C2 | I/O |
| C3 | TCK, I/O |
| C4 | I/O |
| C5 | I/O |
| C6 | PRA, I/O |
| C7 | I/O |
| C8 | I/O |
| C9 | I/O |
| C10 | I/O |
| C11 | I/O |
| C12 | I/O |

| 144-Pin FBGA | |
|---|---|
| **Pin Number** | **A54SX08 Function** |
| D1 | I/O |
| D2 | $V_{CCI}$ |
| D3 | TDI, I/O |
| D4 | I/O |
| D5 | I/O |
| D6 | I/O |
| D7 | I/O |
| D8 | I/O |
| D9 | I/O |
| D10 | I/O |
| D11 | I/O |
| D12 | I/O |
| E1 | I/O |
| E2 | I/O |
| E3 | I/O |
| E4 | I/O |
| E5 | TMS |
| E6 | $V_{CCI}$ |
| E7 | $V_{CCI}$ |
| E8 | $V_{CCI}$ |
| E9 | $V_{CCA}$ |
| E10 | I/O |
| E11 | GND |
| E12 | I/O |
| F1 | I/O |
| F2 | I/O |
| F3 | $V_{CCR}$ |
| F4 | I/O |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | $V_{CCI}$ |
| F9 | I/O |
| F10 | GND |
| F11 | I/O |
| F12 | I/O |

| 144-Pin FBGA | |
|---|---|
| **Pin Number** | **A54SX08 Function** |
| G1 | I/O |
| G2 | GND |
| G3 | I/O |
| G4 | I/O |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | $V_{CCI}$ |
| G9 | I/O |
| G10 | I/O |
| G11 | I/O |
| G12 | I/O |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| H5 | $V_{CCA}$ |
| H6 | $V_{CCA}$ |
| H7 | $V_{CCI}$ |
| H8 | $V_{CCI}$ |
| H9 | $V_{CCA}$ |
| H10 | I/O |
| H11 | I/O |
| H12 | $V_{CCR}$ |
| J1 | I/O |
| J2 | I/O |
| J3 | I/O |
| J4 | I/O |
| J5 | I/O |
| J6 | PRB, I/O |
| J7 | I/O |
| J8 | I/O |
| J9 | I/O |
| J10 | I/O |
| J11 | I/O |
| J12 | $V_{CCA}$ |

| 144-Pin FBGA | |
|---|---|
| **Pin Number** | **A54SX08 Function** |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | I/O |
| K5 | I/O |
| K6 | I/O |
| K7 | GND |
| K8 | I/O |
| K9 | I/O |
| K10 | GND |
| K11 | I/O |
| K12 | I/O |
| L1 | GND |
| L2 | I/O |
| L3 | I/O |
| L4 | I/O |
| L5 | I/O |
| L6 | I/O |
| L7 | HCLK |
| L8 | I/O |
| L9 | I/O |
| L10 | I/O |
| L11 | I/O |
| L12 | I/O |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | I/O |
| M5 | I/O |
| M6 | I/O |
| M7 | $V_{CCA}$ |
| M8 | I/O |
| M9 | I/O |
| M10 | I/O |
| M11 | TDO, I/O |
| M12 | I/O |