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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	175
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx16p-2pqg208i

SX Family FPGAs

General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX's flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

Logic Module Design

The SX family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

Boundary Scan Testing (BST)

All SX devices are IEEE 1149.1 compliant. SX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 1-2. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10 kΩ. TMS can be pulled LOW to initiate the test sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

Table 1-2 • **Boundary Scan Pin Functionality**

Program Fuse Blown (Dedicated Test Mode)	**Program Fuse Not Blown (Flexible Mode)**
TCK, TDI, TDO are dedicated BST pins.	TCK, TDI, TDO are flexible and may be used as I/Os.
No need for pull-up resistor for TMS	Use a pull-up resistor of 10 kΩ on TMS.

Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software by checking the "Reserve JTAG" box in "Device Selection Wizard" (Figure 1-7). JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the Table 1-5 on page 1-8 for detailed specifications.

Figure 1-7 • **Device Selection Wizard**

Development Tool Support

The SX family of FPGAs is fully supported by both the Actel Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the Libero IDE flow diagram (located on the Actel website) for more information.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators, and the simulation results can be cross-probed with Silicon Explorer II, Actel integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Actel Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys®, and Cadence® Design Systems. The Designer software is available for both the Windows® and UNIX® operating systems.

Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-8 on page 1-7 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuitry.

Table 1-4 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to + 70	–40 to + 85	–55 to +125	°C
3.3 V Power Supply Tolerance	±10	±10	±10	%V_{CC}
5.0 V Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note: **Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Table 1-5 • **Electrical Specifications**

		Commercial		Industrial		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{OH}	(I_{OH} = –20 µA) (CMOS) (I_{OH} = –8 mA) (TTL) (I_{OH} = –6 mA) (TTL)	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	V
V_{OL}	(I_{OL}= 20 µA) (CMOS) (I_{OL} = 12 mA) (TTL) (I_{OL} = 8 mA) (TTL)		0.10 0.50		 0.50	V
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		4.0	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See "Evaluating Power in SX Devices" on page 1-16.				

Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{Total} = P_{DC} + P_{AC}$$

EQ 1-5

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • **Standby Power**

I_{CC}	V_{CC}	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + xV_{OL} \times I_{OL} + y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-6

AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

EQ 1-7

$$P_{AC} = V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + (n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + (0.5 \times (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + (0.5 \times (q2 \times CEQCR \times f_{q2}) + (r2 \times f_{q2}))RCLKB + (0.5 \times (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]$$

EQ 1-8

Definition of Terms Used in Formula

m = Number of logic modules switching at f_m
n = Number of input buffers switching at f_n
p = Number of output buffers switching at f_p
q_1 = Number of clock loads on the first routed array clock
q_2 = Number of clock loads on the second routed array clock
x = Number of I/Os at logic low
y = Number of I/Os at logic high
r_1 = Fixed capacitance due to first routed array clock
r_2 = Fixed capacitance due to second routed array clock
s_1 = Number of clock loads on the dedicated array clock
C_{EQM} = Equivalent capacitance of logic modules in pF
C_{EQI} = Equivalent capacitance of input buffers in pF
C_{EQO} = Equivalent capacitance of output buffers in pF
C_{EQCR} = Equivalent capacitance of routed array clock in pF
C_{EQHV} = Variable capacitance of dedicated array clock
C_{EQHF} = Fixed capacitance of dedicated array clock
C_L = Output lead capacitance in pF
f_m = Average logic module switching rate in MHz
f_n = Average input buffer switching rate in MHz
f_p = Average output buffer switching rate in MHz
f_{q1} = Average first routed array clock rate in MHz
f_{q2} = Average second routed array clock rate in MHz
f_{s1} = Average dedicated array clock rate in MHz

Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.

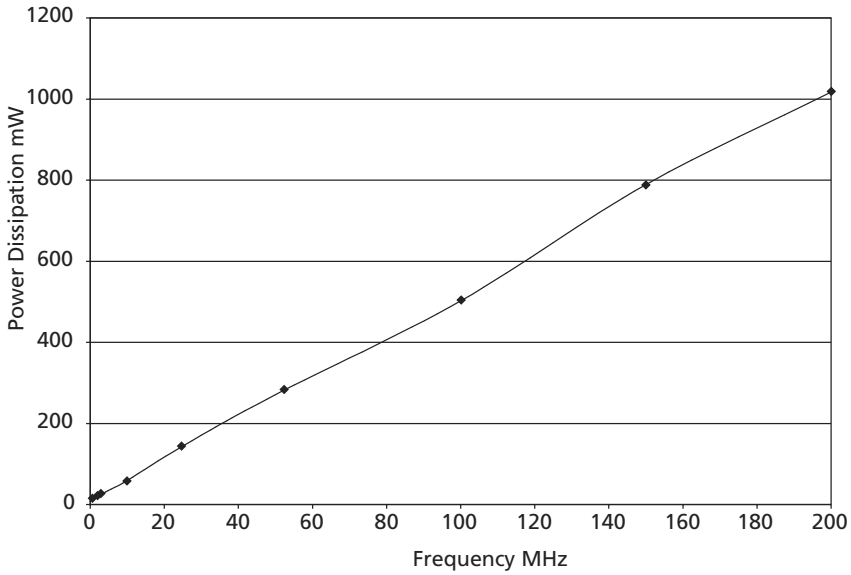

Figure 1-11 • **Power Dissipation**

Junction Temperature (T_J)

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a$$

EQ 1-13

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} \times P$

P = Power calculated from Estimating Power Consumption section

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150 °C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{ (°C/W)}} = \frac{150°C - 70°C}{28°C/W} = 2.86\text{ W}$$

EQ 1-14

Table 1-15 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min.	Units
Plastic Leaded Chip Carrier (PLCC)	84	12	32	22	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Very Thin Quad Flatpack (VQFP)	100	10	38	32	°C/W
Plastic Quad Flat Pack (PQFP) without Heat Spreader	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	14.5	°C/W
Plastic Ball Grid Array (PBGA)	313	3	23	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W

Note: *SX08 does not have a heat spreader.*

Table 1-16 • **Temperature and Voltage Derating Factors***

	Junction Temperature						
V_{CCA}	–55	–40	0	25	70	85	125
3.0	0.75	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.70	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.66	0.69	0.77	0.78	0.87	0.92	1.02

Note: **Normalized to worst-case commercial, T_J = 70°C, V_{CCA} = 3.0 V*

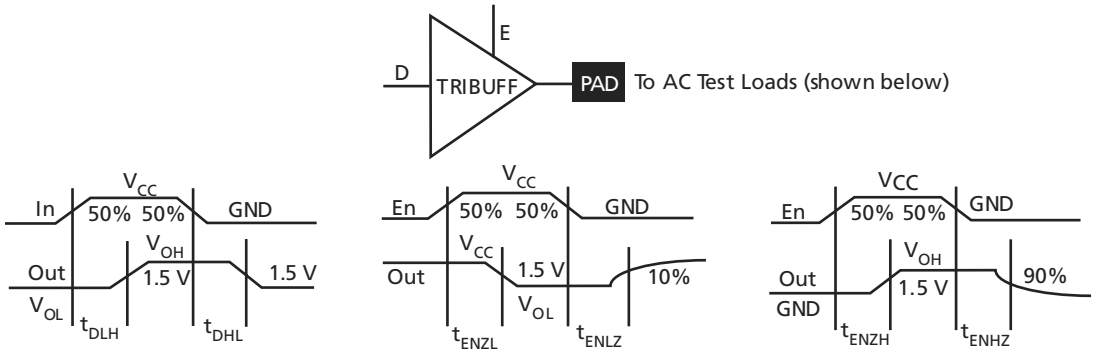

Figure 1-13 • **Output Buffer Delays**

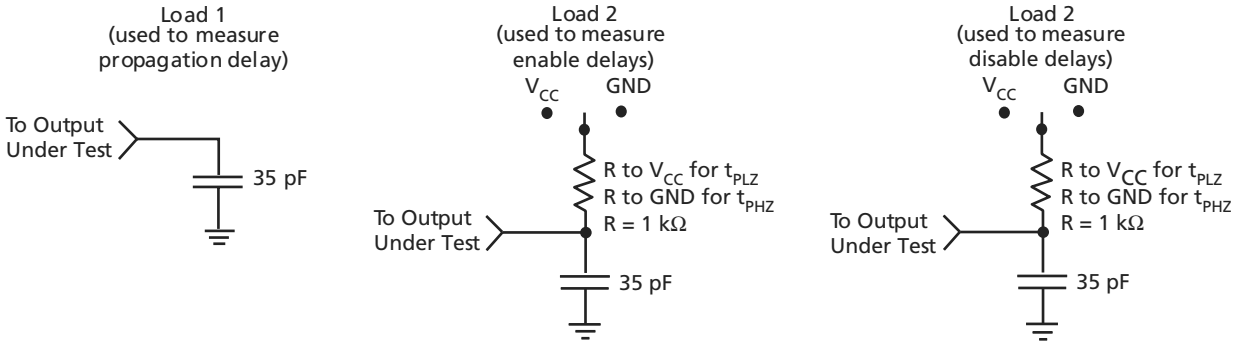

Figure 1-14 • **AC Test Loads**

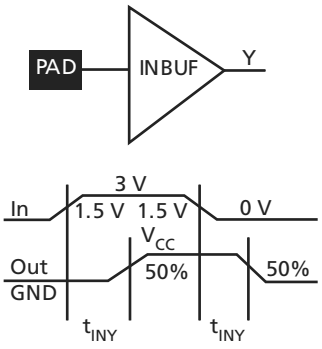

Figure 1-15 • **Input Buffer Delays**

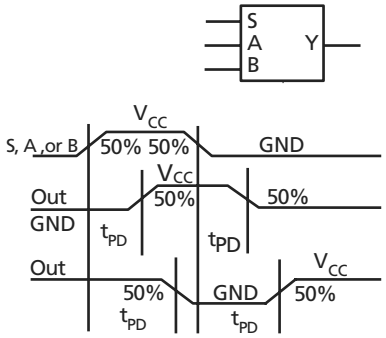

Figure 1-16 • **C-Cell Delays**

A54SX08 Timing Characteristics

Table 1-17 • **A54SX08 Timing Characteristics (Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Input Module Predicted Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics (Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH}, the loading is 5 pF.*

A54SX16P Timing Characteristics

Table 1-19 • **A54SX16P Timing Characteristics (Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.9		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 10 pF loading.*

Table 1-19 • **A54SX16P Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (pad to R-Cell input)		1.2		1.4		1.5		1.8	ns
t_{HCKL}	Input HIGH to LOW (pad to R-Cell input)		1.2		1.4		1.6		1.9	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.3		0.3	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)		1.6		1.8		2.1		2.5	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (pad to R-Cell input)		1.8		2.0		2.3		2.7	ns
t_{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)		1.8		2.1		2.5		2.8	ns
t_{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)		2.0		2.2		2.5		3.0	ns
t_{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)		1.8		2.1		2.4		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)		2.0		2.2		2.5		3.0	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (light load)		0.5		0.5		0.5		0.7	ns
t_{RCKSW}	Maximum Skew (50% load)		0.5		0.6		0.7		0.8	ns
t_{RCKSW}	Maximum Skew (100% load)		0.5		0.6		0.7		0.8	ns
TTL Output Module Timing										
t_{DLH}	Data-to-Pad LOW to HIGH		2.4		2.8		3.1		3.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.3		2.9		3.2		3.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.0		3.4		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.3		3.8		4.3		5.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.3		2.7		3.0		3.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 10 pF loading.*

Table 1-20 • **A54SX32 Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (pad to R-Cell input)		1.9		2.1		2.4		2.8	ns
t_{HCKL}	Input HIGH to LOW (pad to R-Cell input)		1.9		2.1		2.4		2.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)		2.4		2.7		3.0		3.5	ns
t_{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell input)		2.4		2.7		3.1		3.6	ns
t_{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)		2.7		3.0		3.5		4.1	ns
t_{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)		2.7		3.1		3.6		4.2	ns
t_{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)		2.7		3.1		3.5		4.1	ns
t_{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)		2.8		3.2		3.6		4.3	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (light load)		0.85		0.98		1.1		1.3	ns
t_{RCKSW}	Maximum Skew (50% load)		1.23		1.4		1.6		1.9	ns
t_{RCKSW}	Maximum Skew (100% load)		1.30		1.5		1.7		2.0	ns
TTL Output Module Timing[3]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.*

Package Pin Assignments

84-Pin PLCC

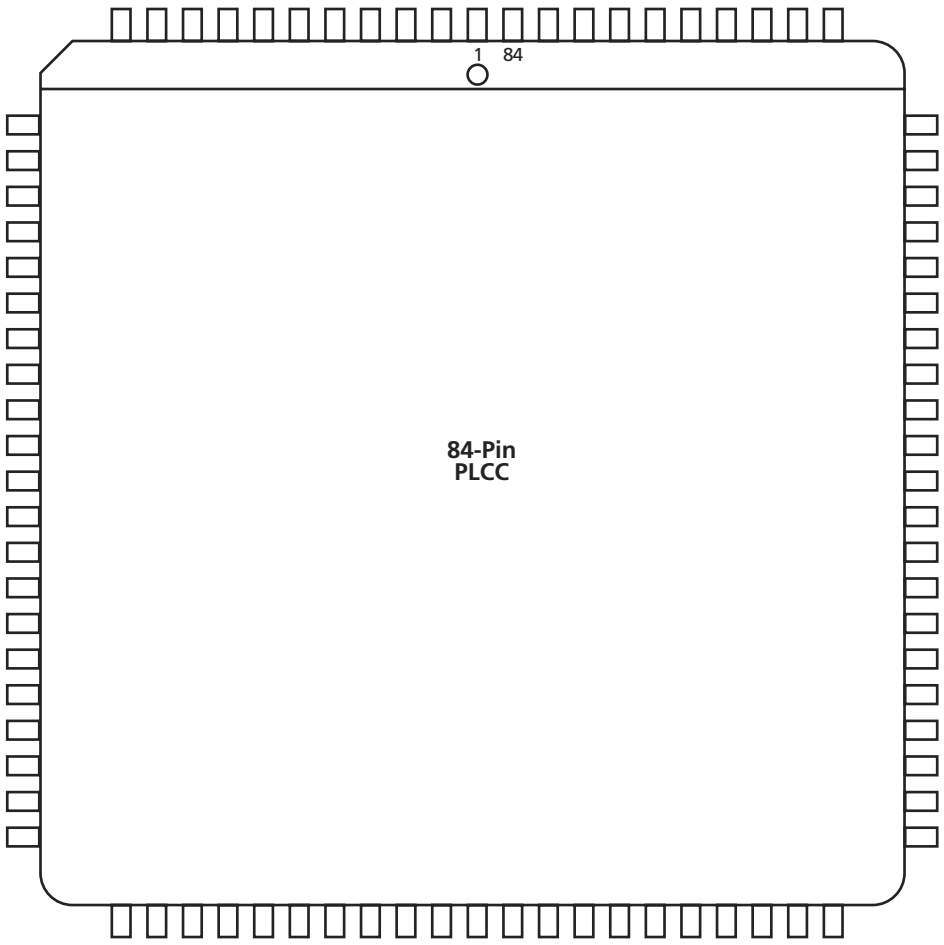

Figure 2-1 • **84-Pin PLCC (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	NC	I/O	I/O
5	I/O	I/O	I/O
6	NC	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	I/O	I/O	I/O
11	TMS	TMS	TMS
12	V_{CCI}	V_{CCI}	V_{CCI}
13	I/O	I/O	I/O
14	NC	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	NC	I/O	I/O
24	I/O	I/O	I/O
25	V_{CCR}	V_{CCR}	V_{CCR}
26	GND	GND	GND
27	V_{CCA}	V_{CCA}	V_{CCA}
28	GND	GND	GND
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	NC	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	I/O	I/O
36	I/O	I/O	I/O

208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	NC	I/O	I/O
40	V_{CCI}	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}	V_{CCA}
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	NC	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	I/O	I/O	I/O
52	GND	GND	GND
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65*	I/O	I/O	NC*
66	I/O	I/O	I/O
67	NC	I/O	I/O
68	I/O	I/O	I/O
69	I/O	I/O	I/O
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O

Note: ** Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
73	NC	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND
78	V_{CCA}	V_{CCA}	V_{CCA}
79	GND	GND	GND
80	V_{CCR}	V_{CCR}	V_{CCR}
81	I/O	I/O	I/O
82	HCLK	HCLK	HCLK
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	NC	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	NC	I/O	I/O
89	I/O	I/O	I/O
90	I/O	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	NC	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	NC	I/O	I/O
98	V_{CCI}	V_{CCI}	V_{CCI}
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	I/O	I/O
107	I/O	I/O	I/O
108	NC	I/O	I/O

208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	V_{CCA}	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}	V_{CCI}
116	NC	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	NC	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	NC	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	NC	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	GND	GND	GND
130	V_{CCA}	V_{CCA}	V_{CCA}
131	GND	GND	GND
132	V_{CCR}	V_{CCR}	V_{CCR}
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	I/O	I/O	I/O

Note: ** Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

144-Pin TQFP

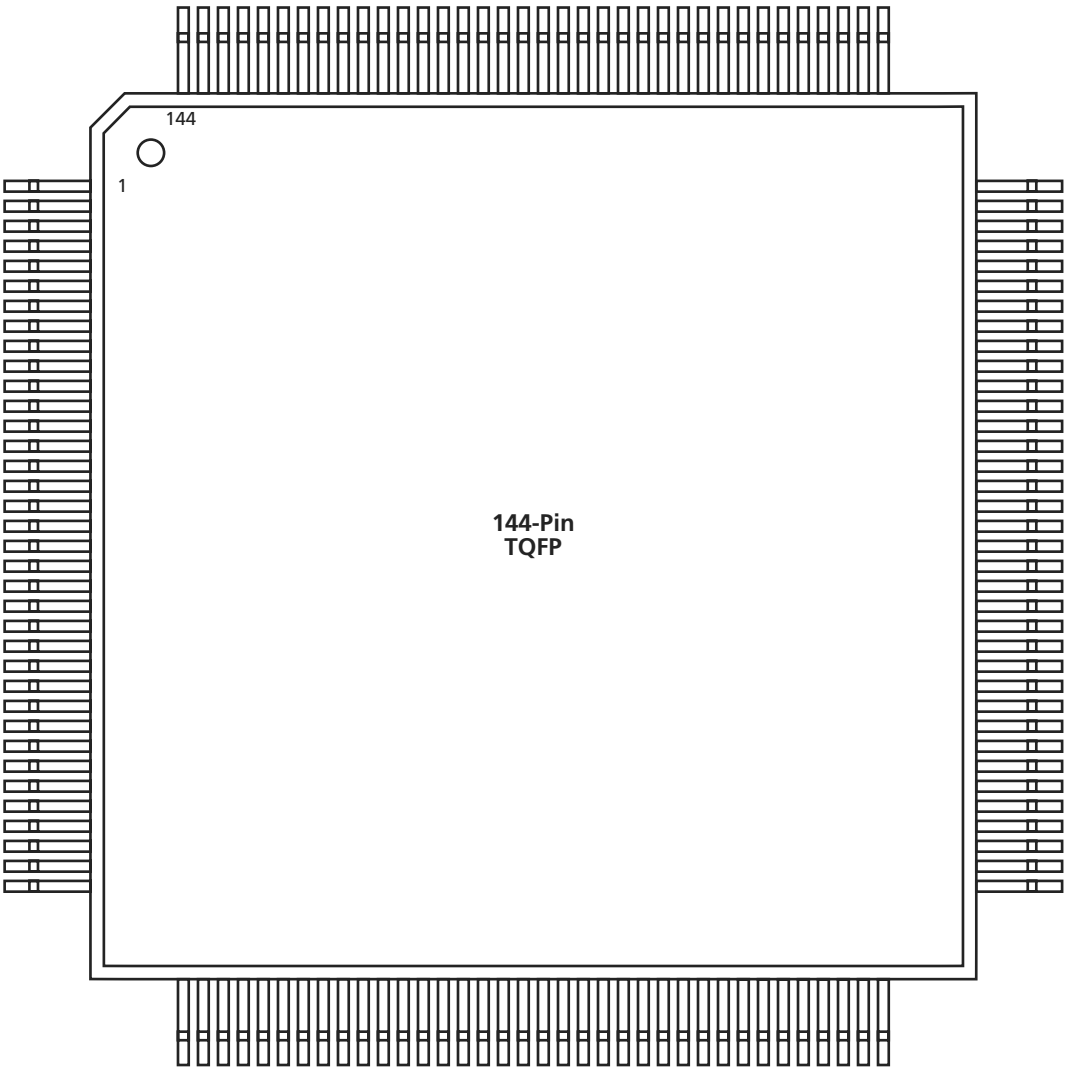

Figure 2-3 • **144-Pin TQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V_{CCI}	V_{CCI}	V_{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	V_{CCR}	V_{CCR}	V_{CCR}
20	V_{CCA}	V_{CCA}	V_{CCA}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V_{CCI}	V_{CCI}	V_{CCI}
30	V_{CCA}	V_{CCA}	V_{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V_{CCA}	V_{CCA}	V_{CCA}
57	GND	GND	GND
58	V_{CCR}	V_{CCR}	V_{CCR}
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V_{CCI}	V_{CCI}	V_{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O

329-Pin PBGA	
Pin Number	**A54SX32 Function**
A1	GND
A2	GND
A3	V_{CCI}
A4	NC
A5	I/O
A6	I/O
A7	V_{CCI}
A8	NC
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	CLKB
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
A20	I/O
A21	NC
A22	V_{CCI}
A23	GND
AA1	V_{CCI}
AA2	I/O
AA3	GND
AA4	I/O
AA5	I/O
AA6	I/O
AA7	I/O
AA8	I/O
AA9	I/O
AA10	I/O
AA11	I/O
AA12	I/O

329-Pin PBGA	
Pin Number	**A54SX32 Function**
AA13	I/O
AA14	I/O
AA15	I/O
AA16	I/O
AA17	I/O
AA18	I/O
AA19	I/O
AA20	TDO, I/O
AA21	V_{CCI}
AA22	I/O
AA23	V_{CCI}
AB1	I/O
AB2	GND
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AB10	I/O
AB11	PRB, I/O
AB12	I/O
AB13	HCLK
AB14	I/O
AB15	I/O
AB16	I/O
AB17	I/O
AB18	I/O
AB19	I/O
AB20	I/O
AB21	I/O
AB22	GND
AB23	I/O
AC1	GND

329-Pin PBGA	
Pin Number	**A54SX32 Function**
AC2	V_{CCI}
AC3	NC
AC4	I/O
AC5	I/O
AC6	I/O
AC7	I/O
AC8	I/O
AC9	V_{CCI}
AC10	I/O
AC11	I/O
AC12	I/O
AC13	I/O
AC14	I/O
AC15	NC
AC16	I/O
AC17	I/O
AC18	I/O
AC19	I/O
AC20	I/O
AC21	NC
AC22	V_{CCI}
AC23	GND
B1	V_{CCI}
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	PRA, I/O
B13	CLKA

329-Pin PBGA	
Pin Number	**A54SX32 Function**
B14	I/O
B15	I/O
B16	I/O
B17	I/O
B18	I/O
B19	I/O
B20	I/O
B21	I/O
B22	GND
B23	V_{CCI}
C1	NC
C2	TDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O
C21	V_{CCI}
C22	GND
C23	NC
D1	I/O
D2	I/O

329-Pin PBGA	
Pin Number	**A54SX32 Function**
D3	I/O
D4	TCK, I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O
D11	V_{CCA}
D12	V_{CCR}
D13	I/O
D14	I/O
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D20	I/O
D21	I/O
D22	I/O
D23	I/O
E1	V_{CCI}
E2	I/O
E3	I/O
E4	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
F1	I/O
F2	TMS
F3	I/O
F4	I/O
F20	I/O
F21	I/O

329-Pin PBGA	
Pin Number	**A54SX32 Function**
F22	I/O
F23	I/O
G1	I/O
G2	I/O
G3	I/O
G4	I/O
G20	I/O
G21	I/O
G22	I/O
G23	GND
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H20	V_{CCA}
H21	I/O
H22	I/O
H23	I/O
J1	NC
J2	I/O
J3	I/O
J4	I/O
J20	I/O
J21	I/O
J22	I/O
J23	I/O
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND

329-Pin PBGA	
Pin Number	**A54SX32 Function**
K20	I/O
K21	I/O
K22	I/O
K23	I/O
L1	I/O
L2	I/O
L3	I/O
L4	V_{CCR}
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L20	V_{CCR}
L21	I/O
L22	I/O
L23	NC
M1	I/O
M2	I/O
M3	I/O
M4	V_{CCA}
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M20	V_{CCA}
M21	I/O
M22	I/O
M23	V_{CCI}
N1	I/O
N2	I/O
N3	I/O
N4	I/O
N10	GND

329-Pin PBGA	
Pin Number	**A54SX32 Function**
N11	GND
N12	GND
N13	GND
N14	GND
N20	NC
N21	I/O
N22	I/O
N23	I/O
P1	I/O
P2	I/O
P3	I/O
P4	I/O
P10	GND
P11	GND
P12	GND
P13	GND
P14	GND
P20	I/O
P21	I/O
P22	I/O
P23	I/O
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R20	I/O
R21	I/O
R22	I/O
R23	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T20	I/O
T21	I/O

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v3.2)	Page
v3.1 (June 2003)	The "Ordering Information" was updated to include RoHS information.	1-ii
	The Product Plan was removed since all products have been released.	N/A
	Information concerning the TRST pin in the "Probe Circuit Control Pins" section was removed.	1-6
	The "Dedicated Test Mode" section is new.	1-6
	The "Programming" section is new.	1-7
	A note was added to the "Power-Up Sequencing" table.	1-15
	A note was added to the "Power-Down Sequencing" table. The 3.3 V comments were updated for the following devices: A54SX08, A54SX16, A54SX32.	1-15
	U11 and U13 were added to the "313-Pin PBGA" table.	2-17
v3.0.1	Storage temperature in Table 1-3 was updated.	1-7
	Table 1-1 was updated.	1-5

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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