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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	147
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx16p-2tq176

PCI Compliance for the SX Family

The SX family supports 3.3 V and 5.0 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 1-6 • A54SX16P DC Specifications (5.0 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		4.75	5.25	V
V_{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V_{IH}	Input High Voltage ¹		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage ¹		-0.5	0.8	V
I_{IH}	Input High Leakage Current	$V_{IN} = 2.7$		70	μA
I_{IL}	Input Low Leakage Current	$V_{IN} = 0.5$		-70	μA
V_{OH}	Output High Voltage	$I_{OUT} = -2 \text{ mA}$	2.4		V
V_{OL}	Output Low Voltage ²	$I_{OUT} = 3 \text{ mA}, 6 \text{ mA}$		0.55	V
C_{IN}	Input Pin Capacitance ³			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance ⁴			8	pF

Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used, AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

A54SX16P DC Specifications (3.3 V PCI Operation)

Table 1-8 • A54SX16P DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		3.0	3.6	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CC}$	V
I_{PU}	Input Pull-up Voltage ¹		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current ²	$0 < V_{IN} < V_{CC}$		± 10	μA
V_{OH}	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OUT} = 1500 \mu A$		$0.1V_{CC}$	V
C_{IN}	Input Pin Capacitance ³			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance ⁴			8	pF

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

Step 1: Define Terms Used in Formula

Module	V_{CCA}	3.3
Number of logic modules switching at f_m (Used 50%)	m	264
Average logic modules switching rate f_m (MHz) (Guidelines: $f/10$)	f_m	20
Module capacitance C_{EQM} (pF)	C_{EQM}	4.0
Input Buffer		
Number of input buffers switching at f_n	n	1
Average input switching rate f_n (MHz) (Guidelines: $f/5$)	f_n	40
Input buffer capacitance C_{EQI} (pF)	C_{EQI}	3.4
Output Buffer		
Number of output buffers switching at f_p	p	1
Average output buffers switching rate f_p (MHz) (Guidelines: $f/10$)	f_p	20
Output buffers buffer capacitance C_{EQO} (pF)	C_{EQO}	4.7
Output Load capacitance C_L (pF)	C_L	35
RCLKA		
Number of Clock loads q_1	q_1	528
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q1}	200
Fixed capacitance (pF)	r_1	138
RCLKB		
Number of Clock loads q_2	q_2	0
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q2}	0
Fixed capacitance (pF)	r_2	138
HCLK		
Number of Clock loads	s_1	0
Variable capacitance of dedicated array clock (pF)	C_{EQHV}	0.61 5
Fixed capacitance of dedicated array clock (pF)	C_{EQHF}	96
Average clock rate (MHz)	f_{s1}	0

Step 2: Calculate Dynamic Power Consumption

$V_{CCA} \times V_{CCA}$	10.89
$m \times f_m \times C_{EQM}$	0.02112
$n \times f_n \times C_{EQI}$	0.000136
$p \times f_p \times (C_{EQO} + C_L)$	0.000794
$0.5 (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1})$	0.11208
$0.5 (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2})$	0
$0.5 (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1})$	0
$P_{AC} = 1.461 \text{ W}$	

Step 3: Calculate DC Power Dissipation**DC Power Dissipation**

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + X \times V_{OL} \times I_{OL} + Y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-12

For a rough estimate of DC Power Dissipation, only use $P_{DC} = (I_{standby}) \times V_{CCA}$. The rest of the formula provides a very small number that can be considered negligible.

$$P_{DC} = (I_{standby}) \times V_{CCA}$$

$$P_{DC} = .55 \text{ mA} \times 3.3 \text{ V}$$

$$P_{DC} = 0.001815 \text{ W}$$

Step 4: Calculate Total Power Consumption

$$P_{Total} = P_{AC} + P_{DC}$$

$$P_{Total} = 1.461 + 0.001815$$

$$P_{Total} = 1.4628 \text{ W}$$

Step 5: Compare Estimated Power Consumption against Characterized Power Consumption

The estimated total power consumption for this design is 1.46 W. The characterized power consumption for this design at 200 MHz is 1.0164 W.

The diagram illustrates the timing of a 2-stage pipeline. It is divided into three main sections: Input Delays, Internal Delays, and Output Delays.

- Input Delays:** The input signal passes through an I/O Module with a delay $t_{INY} = 1.5 \text{ ns}$. The signal then splits into two paths: one to the Combinatorial Cell and another to the first Register Cell. The delay from the input to the first Register Cell is $t_{IRD2} = 0.6 \text{ ns}$.
- Internal Delays:**
 - The **Combinatorial Cell** has a delay $t_{PD} = 0.6 \text{ ns}$.
 - The **Register Cell** has a setup time $t_{SUD} = 0.5 \text{ ns}$, a hold time $t_{HD} = 0.0 \text{ ns}$, and a recovery time $t_{RCO} = 0.8 \text{ ns}$.
 - The **Register Cell** has a delay $t_{RD1} = 0.3 \text{ ns}$.
- Output Delays:**
 - The output of the first Register Cell passes through an I/O Module with a delay $t_{DHL} = 1.6 \text{ ns}$.
 - The output of the second Register Cell passes through an I/O Module with a delay $t_{DLH} = 1.6 \text{ ns}$ and an enable-to-high delay $t_{ENZH} = 2.3 \text{ ns}$.

The diagram also shows the clocking of the pipeline. The **Routed Clock** has a delay $t_{RCKH} = 1.5 \text{ ns}$ (100% Load) and a maximum frequency $F_{MAX} = 250 \text{ MHz}$. The **Hardwired Clock** has a delay $t_{HCKH} = 1.0 \text{ ns}$ and a maximum frequency $F_{HMAX} = 320 \text{ MHz}$.

Figure 1-12 • SX Timing Model

Routed Clock

EQ 1-15

EQ 1-17

Clock-to-Out (Pin-to-Pin)

EQ 1-16

EQ 1-18

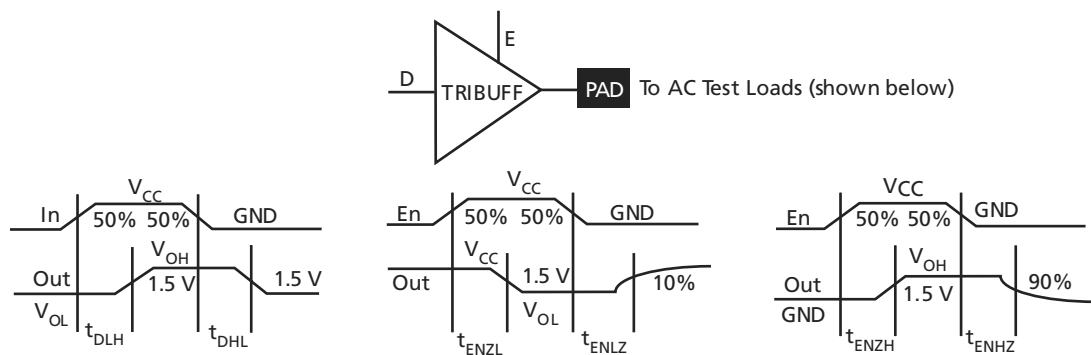


Figure 1-13 • Output Buffer Delays

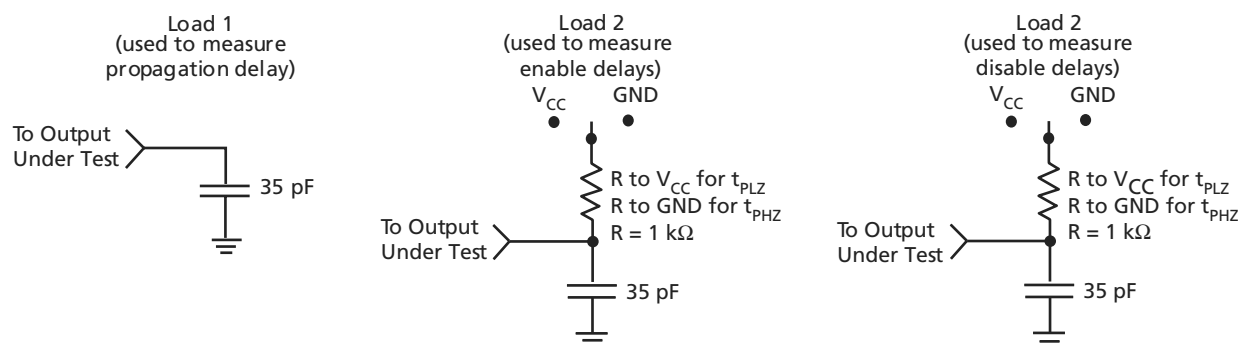


Figure 1-14 • AC Test Loads

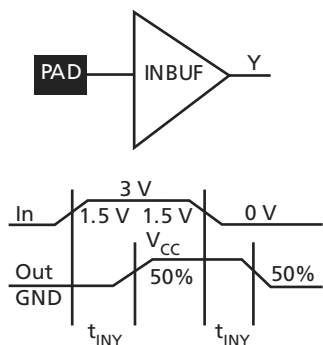


Figure 1-15 • Input Buffer Delays

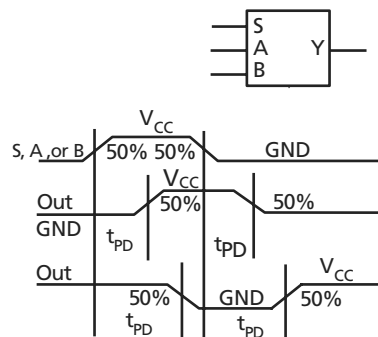


Figure 1-16 • C-Cell Delays

Package Pin Assignments

84-Pin PLCC

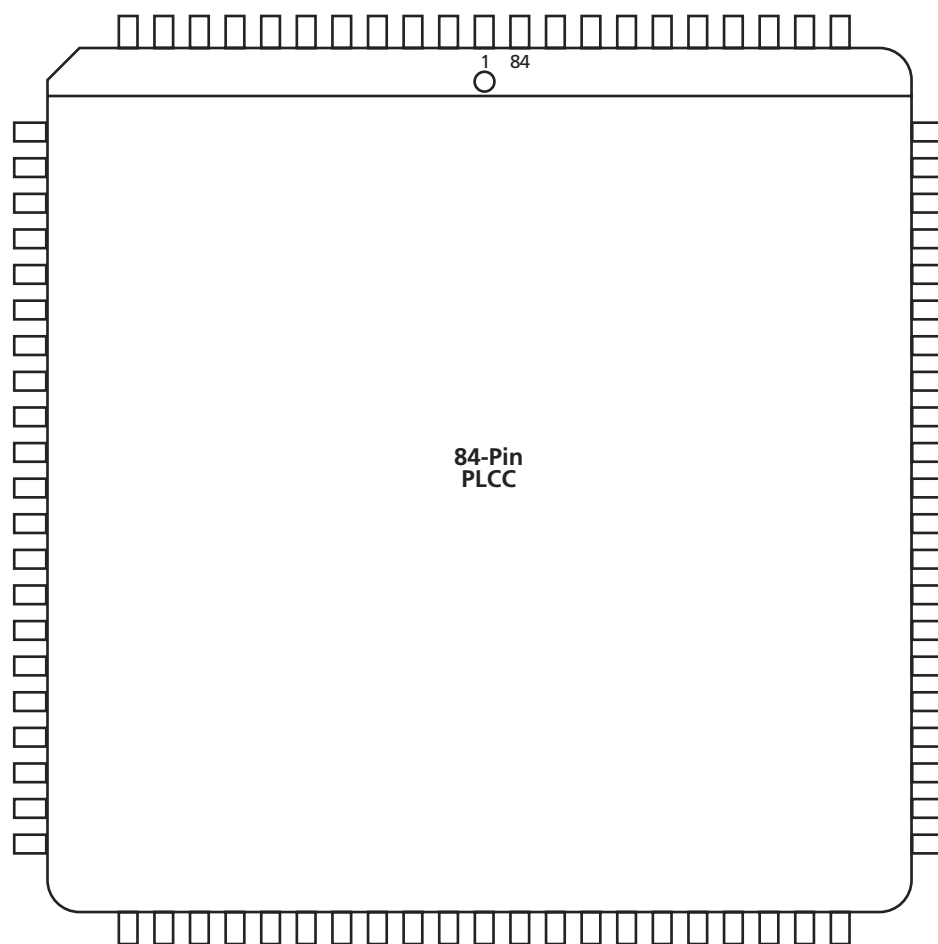


Figure 2-1 • 84-Pin PLCC (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

84-Pin PLCC	
Pin Number	A54SX08 Function
1	V _{CCR}
2	GND
3	V _{CCA}
4	PRA, I/O
5	I/O
6	I/O
7	V _{CCI}
8	I/O
9	I/O
10	I/O
11	TCK, I/O
12	TDI, I/O
13	I/O
14	I/O
15	I/O
16	TMS
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V _{CCI}
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O

84-Pin PLCC	
Pin Number	A54SX08 Function
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V _{CCA}
42	GND
43	V _{CCR}
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V _{CCA}
60	V _{CCI}
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V _{CCA}
69	GND
70	I/O

84-Pin PLCC	
Pin Number	A54SX08 Function
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	CLKA
84	CLKB

208-Pin PQFP

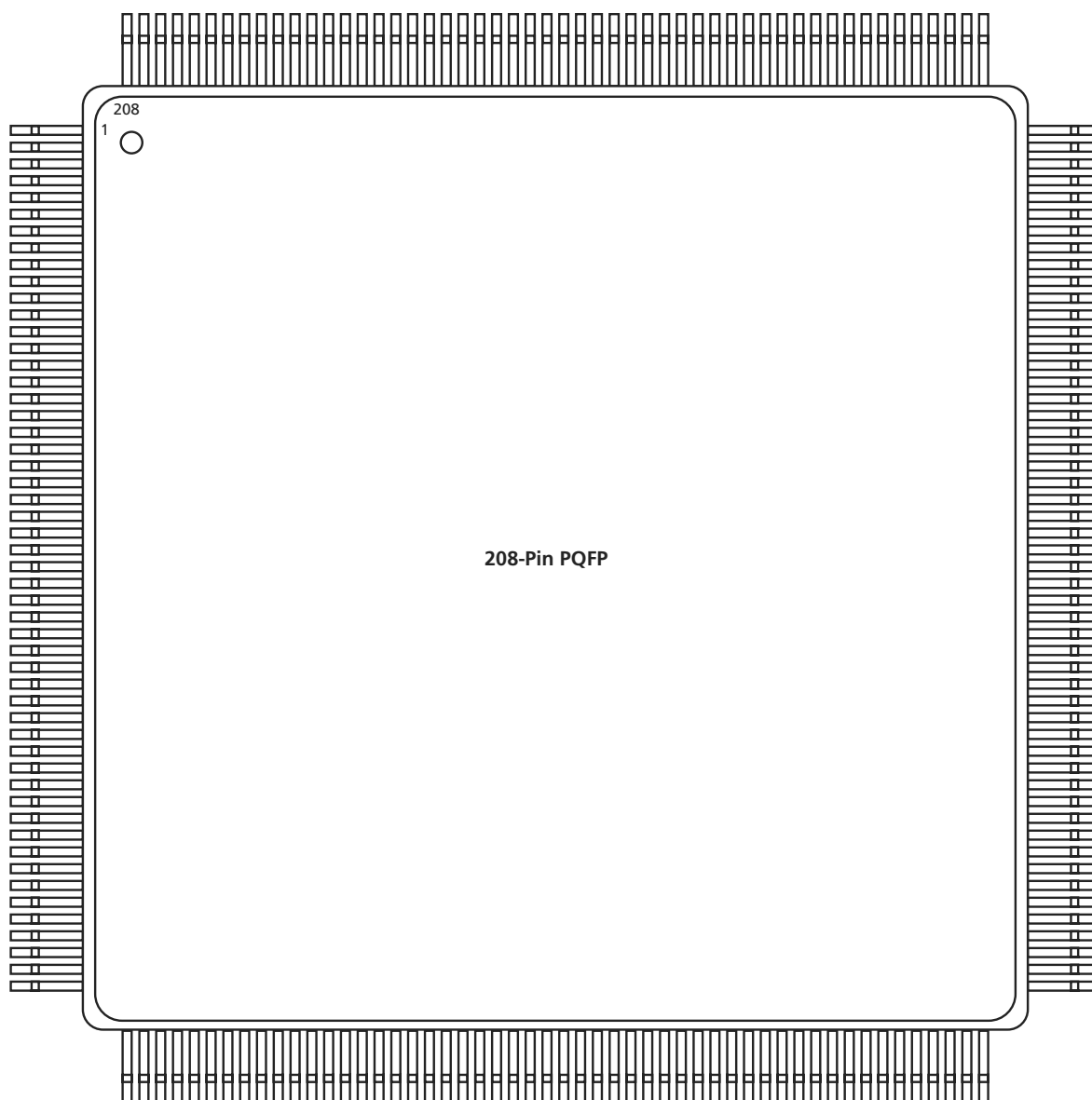


Figure 2-2 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
145	V _{CCA}	V _{CCA}	V _{CCA}
146	GND	GND	GND
147	I/O	I/O	I/O
148	V _{CCI}	V _{CCI}	V _{CCI}
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	NC	I/O	I/O
156	NC	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	V _{CCI}	V _{CCI}	V _{CCI}
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	NC	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	NC	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	NC	I/O	I/O
177	I/O	I/O	I/O
178	I/O	I/O	I/O
179	I/O	I/O	I/O
180	CLKA	CLKA	CLKA

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
181	CLKB	CLKB	CLKB
182	V _{CCR}	V _{CCR}	V _{CCR}
183	GND	GND	GND
184	V _{CCA}	V _{CCA}	V _{CCA}
185	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	NC	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	NC	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	NC	I/O	I/O
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	NC	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	V _{CCI}	V _{CCI}	V _{CCI}
202	NC	I/O	I/O
203	NC	I/O	I/O
204	I/O	I/O	I/O
205	NC	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

144-Pin TQFP

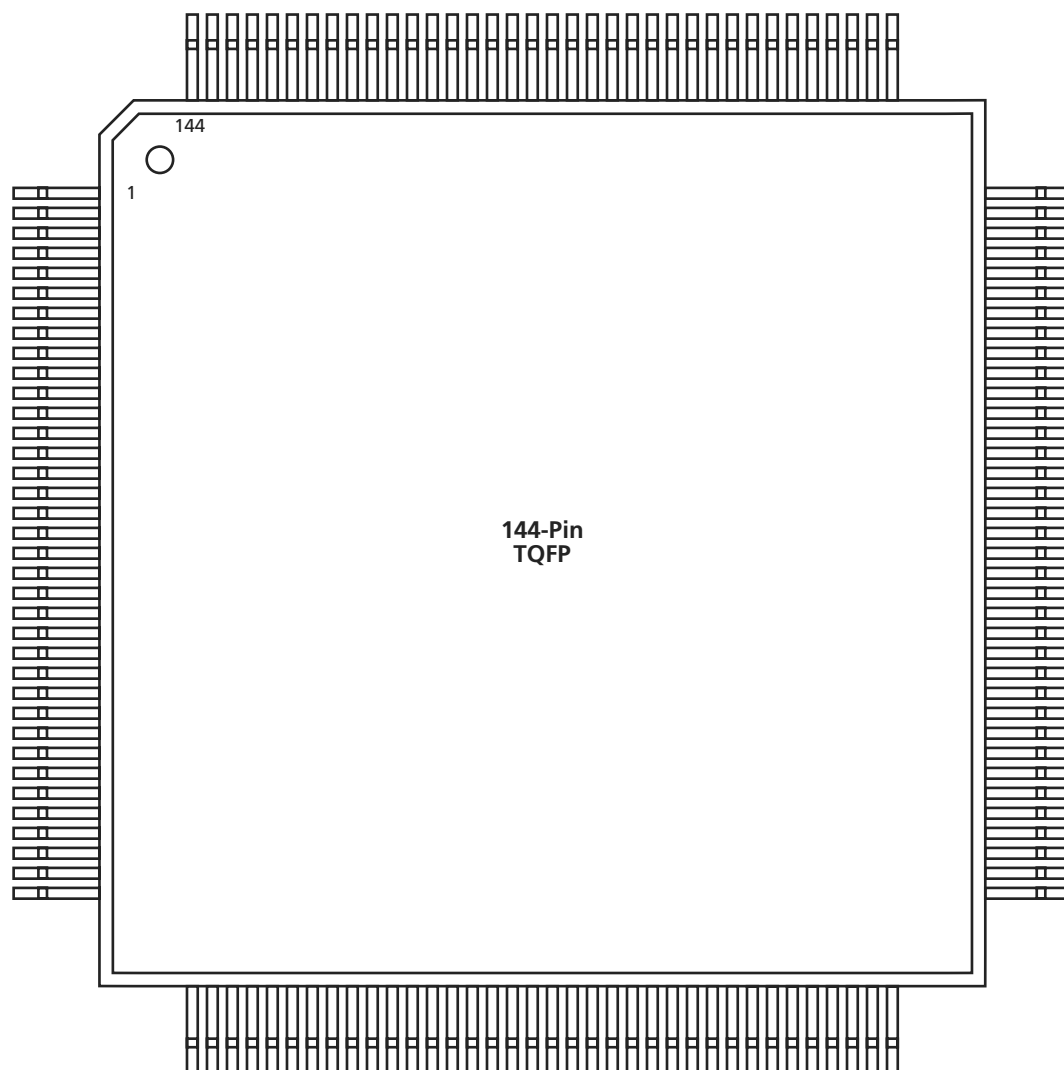


Figure 2-3 • 144-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V _{CCI}	V _{CCI}	V _{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	V _{CCR}	V _{CCR}	V _{CCR}
20	V _{CCA}	V _{CCA}	V _{CCA}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V _{CCI}	V _{CCI}	V _{CCI}
30	V _{CCA}	V _{CCA}	V _{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V _{CCI}	V _{CCI}	V _{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V _{CCA}	V _{CCA}	V _{CCA}
57	GND	GND	GND
58	V _{CCR}	V _{CCR}	V _{CCR}
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V _{CCI}	V _{CCI}	V _{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V _{CCI}	V _{CCI}	V _{CCI}
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V _{CCA}	V _{CCA}	V _{CCA}
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V _{CCI}	V _{CCI}	V _{CCI}
33	V _{CCA}	V _{CCA}	V _{CCA}
34	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V _{CCI}	V _{CCI}	V _{CCI}
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V _{CCA}	V _{CCA}	V _{CCA}
67	V _{CCR}	V _{CCR}	V _{CCR}
68	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	I/O	I/O	I/O
146	I/O	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	CLKA	CLKA	CLKA
153	CLKB	CLKB	CLKB
154	V _{CCR}	V _{CCR}	V _{CCR}
155	GND	GND	GND
156	V _{CCA}	V _{CCA}	V _{CCA}

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
157	PRA, I/O	PRA, I/O	PRA, I/O
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	V _{CCI}	V _{CCI}	V _{CCI}
170	I/O	I/O	I/O
171	NC	I/O	I/O
172	NC	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	TCK, I/O	TCK, I/O	TCK, I/O

100-Pin VQFP		
Pin Number	A545X08 Function	A545X16, A545X16P Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	TMS	TMS
8	V _{CCI}	V _{CCI}
9	GND	GND
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	V _{CCI}	V _{CCI}
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	PRB, I/O	PRB, I/O

100-Pin VQFP		
Pin Number	A545X08 Function	A545X16, A545X16P Function
35	V _{CCA}	V _{CCA}
36	GND	GND
37	V _{CCR}	V _{CCR}
38	I/O	I/O
39	HCLK	HCLK
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	V _{CCI}	V _{CCI}
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	TDO, I/O	TDO, I/O
50	I/O	I/O
51	GND	GND
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	V _{CCA}	V _{CCA}
58	V _{CCI}	V _{CCI}
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	V _{CCA}	V _{CCA}
68	GND	GND

100-Pin VQFP		
Pin Number	A545X08 Function	A545X16, A545X16P Function
69	GND	GND
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	V _{CCI}	V _{CCI}
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	CLKA	CLKA
88	CLKB	CLKB
89	V _{CCR}	V _{CCR}
90	V _{CCA}	V _{CCA}
91	GND	GND
92	PRA, I/O	PRA, I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	TCK, I/O	TCK, I/O

313-Pin PBGA

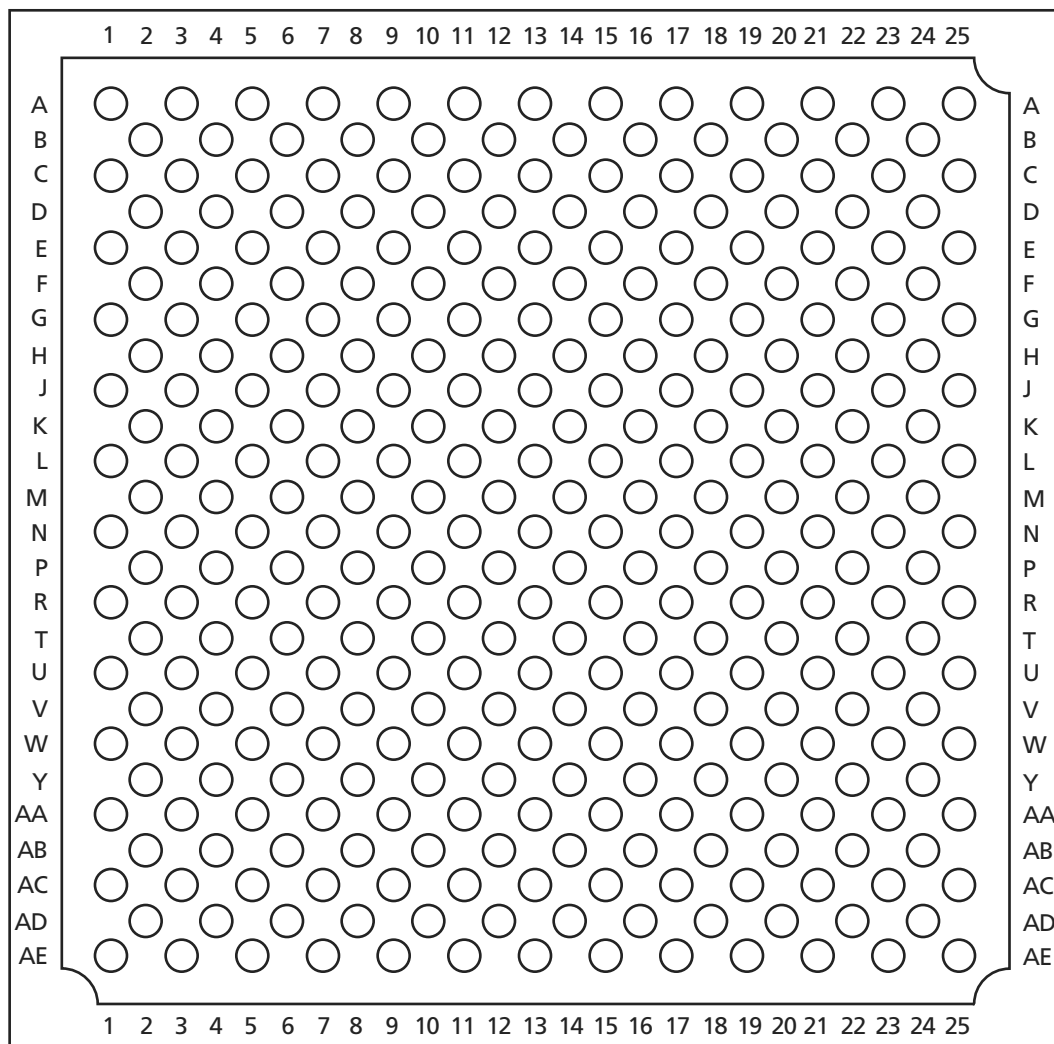


Figure 2-6 • 313-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
A1	GND	AA13	I/O	AC2	V _{CCI}	B14	I/O
A2	GND	AA14	I/O	AC3	NC	B15	I/O
A3	V _{CCI}	AA15	I/O	AC4	I/O	B16	I/O
A4	NC	AA16	I/O	AC5	I/O	B17	I/O
A5	I/O	AA17	I/O	AC6	I/O	B18	I/O
A6	I/O	AA18	I/O	AC7	I/O	B19	I/O
A7	V _{CCI}	AA19	I/O	AC8	I/O	B20	I/O
A8	NC	AA20	TDO, I/O	AC9	V _{CCI}	B21	I/O
A9	I/O	AA21	V _{CCI}	AC10	I/O	B22	GND
A10	I/O	AA22	I/O	AC11	I/O	B23	V _{CCI}
A11	I/O	AA23	V _{CCI}	AC12	I/O	C1	NC
A12	I/O	AB1	I/O	AC13	I/O	C2	TDI, I/O
A13	CLKB	AB2	GND	AC14	I/O	C3	GND
A14	I/O	AB3	I/O	AC15	NC	C4	I/O
A15	I/O	AB4	I/O	AC16	I/O	C5	I/O
A16	I/O	AB5	I/O	AC17	I/O	C6	I/O
A17	I/O	AB6	I/O	AC18	I/O	C7	I/O
A18	I/O	AB7	I/O	AC19	I/O	C8	I/O
A19	I/O	AB8	I/O	AC20	I/O	C9	I/O
A20	I/O	AB9	I/O	AC21	NC	C10	I/O
A21	NC	AB10	I/O	AC22	V _{CCI}	C11	I/O
A22	V _{CCI}	AB11	PRB, I/O	AC23	GND	C12	I/O
A23	GND	AB12	I/O	B1	V _{CCI}	C13	I/O
AA1	V _{CCI}	AB13	HCLK	B2	GND	C14	I/O
AA2	I/O	AB14	I/O	B3	I/O	C15	I/O
AA3	GND	AB15	I/O	B4	I/O	C16	I/O
AA4	I/O	AB16	I/O	B5	I/O	C17	I/O
AA5	I/O	AB17	I/O	B6	I/O	C18	I/O
AA6	I/O	AB18	I/O	B7	I/O	C19	I/O
AA7	I/O	AB19	I/O	B8	I/O	C20	I/O
AA8	I/O	AB20	I/O	B9	I/O	C21	V _{CCI}
AA9	I/O	AB21	I/O	B10	I/O	C22	GND
AA10	I/O	AB22	GND	B11	I/O	C23	NC
AA11	I/O	AB23	I/O	B12	PRA, I/O	D1	I/O
AA12	I/O	AC1	GND	B13	CLKA	D2	I/O

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function
D3	I/O	F22	I/O	K20	I/O	N11	GND
D4	TCK, I/O	F23	I/O	K21	I/O	N12	GND
D5	I/O	G1	I/O	K22	I/O	N13	GND
D6	I/O	G2	I/O	K23	I/O	N14	GND
D7	I/O	G3	I/O	L1	I/O	N20	NC
D8	I/O	G4	I/O	L2	I/O	N21	I/O
D9	I/O	G20	I/O	L3	I/O	N22	I/O
D10	I/O	G21	I/O	L4	V _{CCR}	N23	I/O
D11	V _{CCA}	G22	I/O	L10	GND	P1	I/O
D12	V _{CCR}	G23	GND	L11	GND	P2	I/O
D13	I/O	H1	I/O	L12	GND	P3	I/O
D14	I/O	H2	I/O	L13	GND	P4	I/O
D15	I/O	H3	I/O	L14	GND	P10	GND
D16	I/O	H4	I/O	L20	V _{CCR}	P11	GND
D17	I/O	H20	V _{CCA}	L21	I/O	P12	GND
D18	I/O	H21	I/O	L22	I/O	P13	GND
D19	I/O	H22	I/O	L23	NC	P14	GND
D20	I/O	H23	I/O	M1	I/O	P20	I/O
D21	I/O	J1	NC	M2	I/O	P21	I/O
D22	I/O	J2	I/O	M3	I/O	P22	I/O
D23	I/O	J3	I/O	M4	V _{CCA}	P23	I/O
E1	V _{CCI}	J4	I/O	M10	GND	R1	I/O
E2	I/O	J20	I/O	M11	GND	R2	I/O
E3	I/O	J21	I/O	M12	GND	R3	I/O
E4	I/O	J22	I/O	M13	GND	R4	I/O
E20	I/O	J23	I/O	M14	GND	R20	I/O
E21	I/O	K1	I/O	M20	V _{CCA}	R21	I/O
E22	I/O	K2	I/O	M21	I/O	R22	I/O
E23	I/O	K3	I/O	M22	I/O	R23	I/O
F1	I/O	K4	I/O	M23	V _{CCI}	T1	I/O
F2	TMS	K10	GND	N1	I/O	T2	I/O
F3	I/O	K11	GND	N2	I/O	T3	I/O
F4	I/O	K12	GND	N3	I/O	T4	I/O
F20	I/O	K13	GND	N4	I/O	T20	I/O
F21	I/O	K14	GND	N10	GND	T21	I/O

144-Pin FBGA

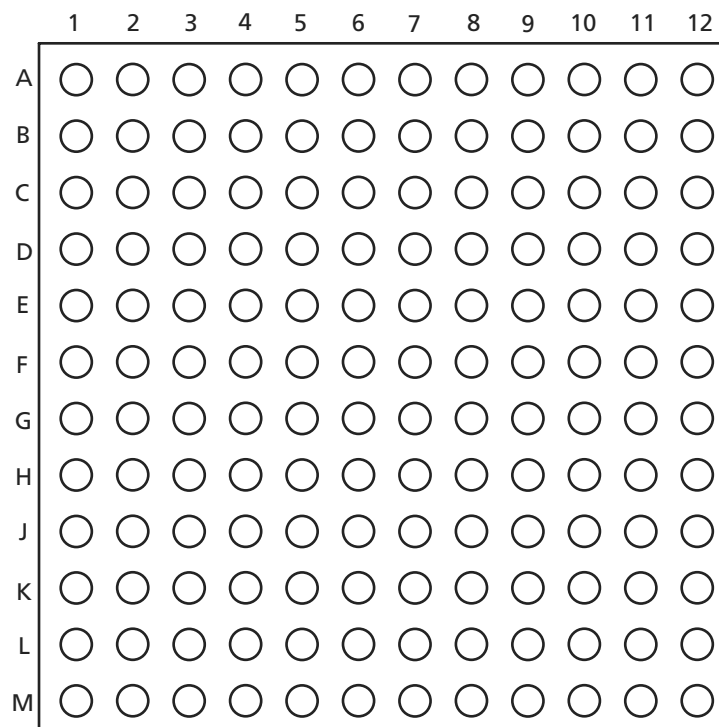


Figure 2-8 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v3.2)	Page
v3.1 (June 2003)	The "Ordering Information" was updated to include RoHS information.	1-ii
	The Product Plan was removed since all products have been released.	N/A
	Information concerning the TRST pin in the "Probe Circuit Control Pins" section was removed.	1-6
	The "Dedicated Test Mode" section is new.	1-6
	The "Programming" section is new.	1-7
	A note was added to the "Power-Up Sequencing" table.	1-15
	A note was added to the "Power-Down Sequencing" table. The 3.3 V comments were updated for the following devices: A545X08, A545X16, A545X32.	1-15
	U11 and U13 were added to the "313-Pin PBGA" table.	2-17
v3.0.1	Storage temperature in Table 1-3 was updated.	1-7
	Table 1-1 was updated.	1-5

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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