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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

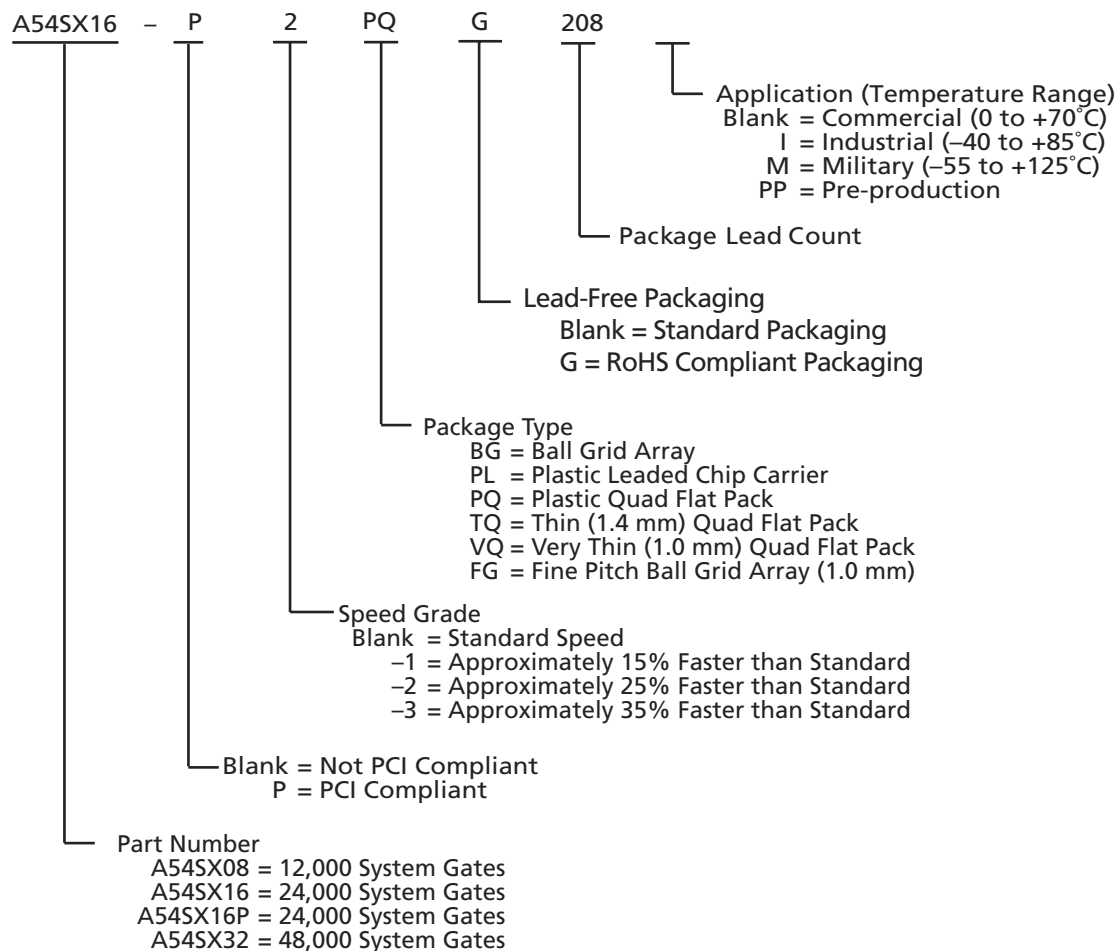
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	175
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx16p-pqg208

Ordering Information



Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PLCC 84-Pin	VQFP 100-Pin	PQFP 208-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 313-Pin	PBGA 329-Pin	FBGA 144-Pin
A54SX08	69	81	130	113	128	–	–	111
A54SX16	–	81	175	–	147	–	–	–
A54SX16P	–	81	175	113	147	–	–	–
A54SX32	–	–	174	113	147	249	249	–

Note: Package Definitions (Consult your local Actel sales representative for product availability):

PLCC = Plastic Leaded Chip Carrier

PQFP = Plastic Quad Flat Pack

TQFP = Thin Quad Flat Pack

VQFP = Very Thin Quad Flat Pack

PBGA = Plastic Ball Grid Array

FBGA = Fine Pitch (1.0 mm) Ball Grid Array

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

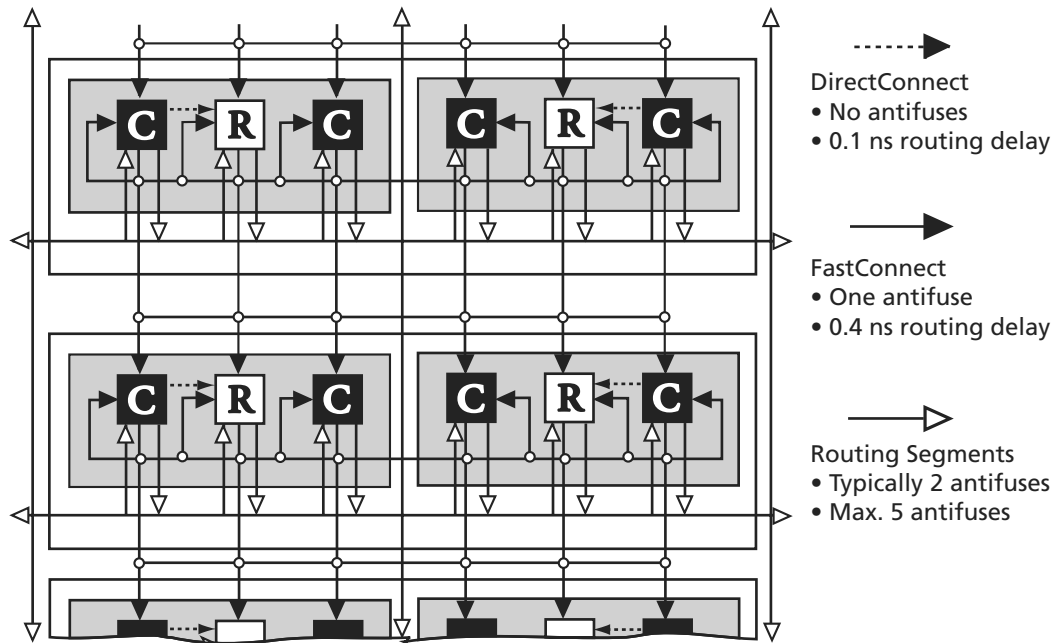


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

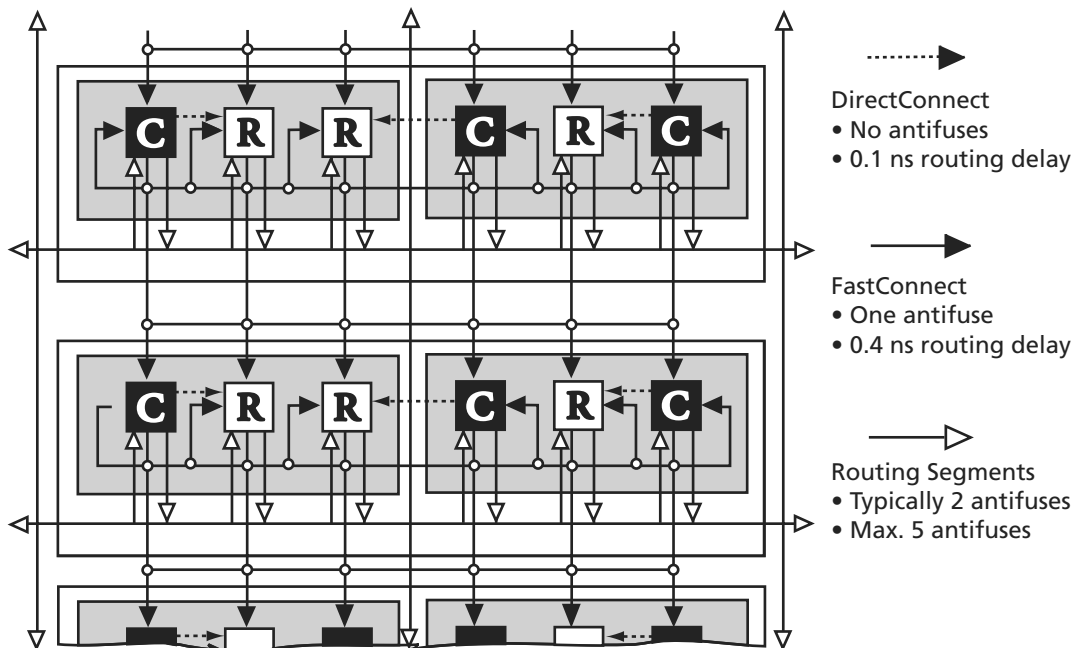


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

Table 1-4 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to + 70	–40 to + 85	–55 to +125	°C
3.3 V Power Supply Tolerance	±10	±10	±10	%V _{CC}
5.0 V Power Supply Tolerance	±5	±10	±10	%V _{CC}

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Table 1-5 • Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V _{OH}	(I _{OH} = –20 μ A) (CMOS) (I _{OH} = –8 mA) (TTL) (I _{OH} = –6 mA) (TTL)	(V _{CCI} – 0.1) 2.4	V _{CCI} V _{CCI}	(V _{CCI} – 0.1) 2.4	V _{CCI} V _{CCI}	V
V _{OL}	(I _{OL} = 20 μ A) (CMOS) (I _{OL} = 12 mA) (TTL) (I _{OL} = 8 mA) (TTL)		0.10 0.50		0.50	V
V _{IL}			0.8		0.8	V
V _{IH}		2.0		2.0		V
t _R , t _F	Input Transition Time t _R , t _F		50		50	ns
C _{IO}	C _{IO} I/O Capacitance		10		10	pF
I _{CC}	Standby Current, I _{CC}		4.0		4.0	mA
I _{CC(D)}	I _{CC(D)} I _{Dynamic} V _{CC} Supply Current	See "Evaluating Power in SX Devices" on page 1-16.				

PCI Compliance for the SX Family

The SX family supports 3.3 V and 5.0 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 1-6 • A54SX16P DC Specifications (5.0 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V _{CCA}	Supply Voltage for Array		3.0	3.6	V
V _{CCR}	Supply Voltage required for Internal Biasing		4.75	5.25	V
V _{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V _{IH}	Input High Voltage ¹		2.0	V _{CC} + 0.5	V
V _{IL}	Input Low Voltage ¹		-0.5	0.8	V
I _{IH}	Input High Leakage Current	V _{IN} = 2.7		70	μA
I _{IL}	Input Low Leakage Current	V _{IN} = 0.5		-70	μA
V _{OH}	Output High Voltage	I _{OUT} = -2 mA	2.4		V
V _{OL}	Output Low Voltage ²	I _{OUT} = 3 mA, 6 mA		0.55	V
C _{IN}	Input Pin Capacitance ³			10	pF
C _{CLK}	CLK Pin Capacitance		5	12	pF
C _{IDSEL}	IDSEL Pin Capacitance ⁴			8	pF

Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used, AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

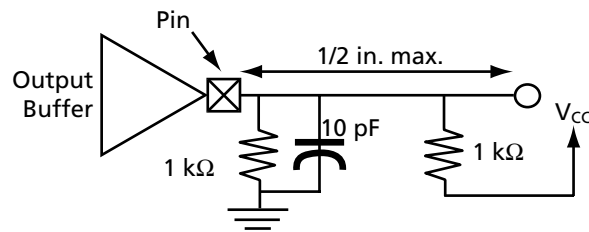
A54SX16P AC Specifications for (PCI Operation)

Table 1-7 • A54SX16P AC Specifications for (PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4^1$	-44		mA
		$1.4 \leq V_{OUT} < 2.4^1, ^2$	$-44 + (V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}^{1, ^3}$		EQ 1-1 on page 1-11	
	(Test Point)	$V_{OUT} = 3.1^3$		-142	mA
$I_{OL(AC)}$	Switching Current High	$V_{OUT} \geq 2.2^1$	95		mA
		$2.2 > V_{OUT} > 0.55^1$	$V_{OUT}/0.023$		
		$0.71 > V_{OUT} > 0^{1, ^3}$		EQ 1-2 on page 1-11	mA
	(Test Point)	$V_{OUT} = 0.71^3$		206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load ⁴	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load ⁴	1	5	V/ns

Notes:

1. Refer to the *V_I* curves in Figure 1-9 on page 1-11. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half-size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maxima (A and B) are provided with the respective diagrams in Figure 1-9 on page 1-11. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.



A54SX16P DC Specifications (3.3 V PCI Operation)

Table 1-8 • A54SX16P DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		3.0	3.6	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CC}$	V
I_{IPU}	Input Pull-up Voltage ¹		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current ²	$0 < V_{IN} < V_{CC}$		± 10	μA
V_{OH}	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OUT} = 1500 \mu A$		$0.1V_{CC}$	V
C_{IN}	Input Pin Capacitance ³			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance ⁴			8	pF

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

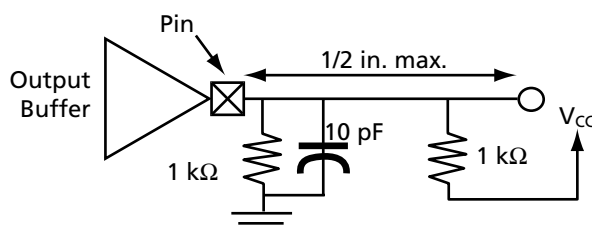
A54SX16P AC Specifications (3.3 V PCI Operation)

Table 1-9 • A54SX16P AC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CC}^1$			mA
		$0.3V_{CC} \leq V_{OUT} < 0.9V_{CC}^1$	$-12V_{CC}$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}^{1,2}$	$-17.1 + (V_{CC} - V_{OUT})$	EQ 1-3 on page 1-14	
	(Test Point)	$V_{OUT} = 0.7V_{CC}^2$		$-32V_{CC}$	mA
$I_{OL(AC)}$	Switching Current High	$V_{CC} > V_{OUT} \geq 0.6V_{CC}^1$			mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}^1$	$16V_{CC}$		mA
		$0.18V_{CC} > V_{OUT} > 0^{1,2}$	$26.7V_{OUT}$	EQ 1-4 on page 1-14	mA
	(Test Point)	$V_{OUT} = 0.18V_{CC}^2$		$38V_{CC}$	
I_{CL}	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$-3 < V_{IN} \leq -1$	$25 + (V_{IN} - V_{OUT} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate ³	0.2V _{CC} to 0.6V _{CC} load	1	4	V/ns
$slew_F$	Output Fall Slew Rate ³	0.6V _{CC} to 0.2V _{CC} load	1	4	V/ns

Notes:

1. Refer to the V/I curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.



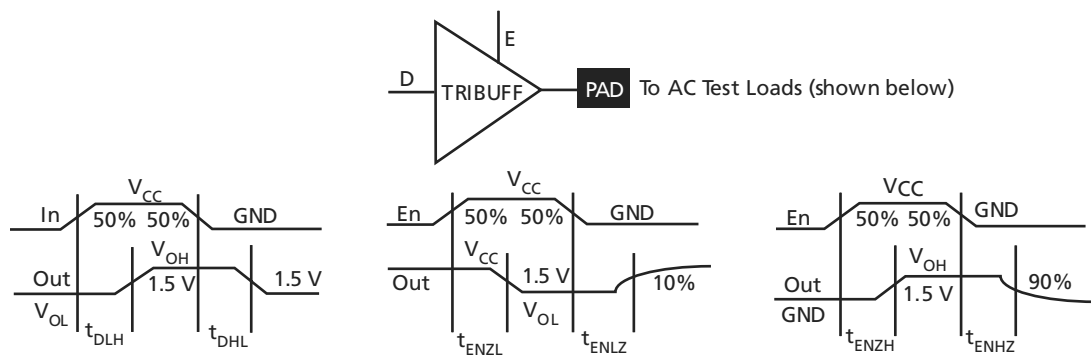


Figure 1-13 • Output Buffer Delays

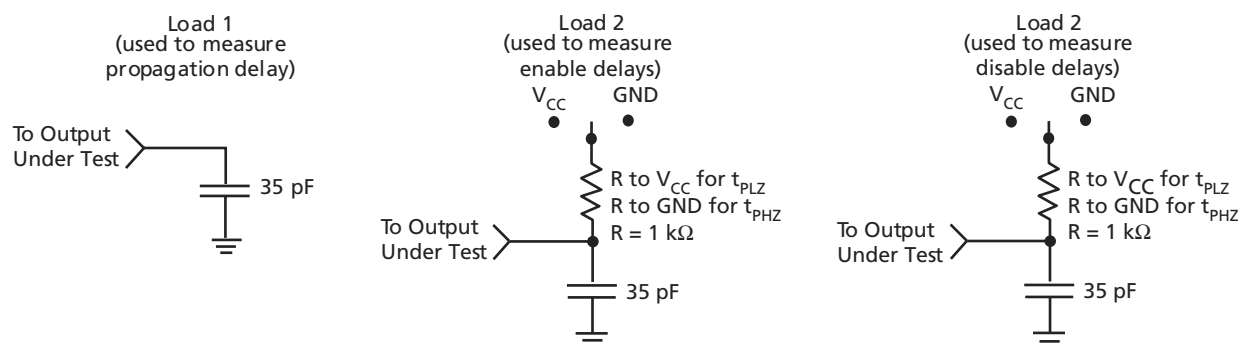


Figure 1-14 • AC Test Loads

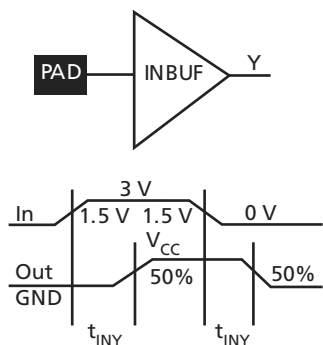


Figure 1-15 • Input Buffer Delays

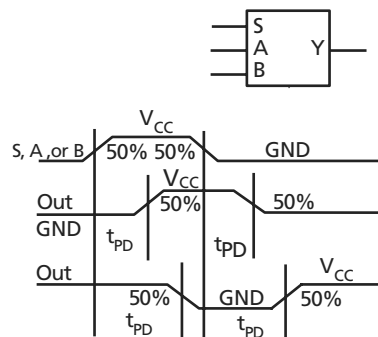


Figure 1-16 • C-Cell Delays

A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics**
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ¹										
t _{PD}	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays ²										
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{RD2}	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t _{RD3}	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t _{RD4}	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{RD8}	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t _{RD12}	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t _{RCO}	Sequential Clock-to-Q	0.8		1.1		1.2		1.4		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t _{INYH}	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t _{INYL}	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays ²										
t _{IRD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{IRD2}	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t _{IRD3}	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t _{IRD4}	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{IRD8}	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t _{IRD12}	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} , the loading is 5 pF.

Table 1-19 • A54SX16P Timing Characteristics (Continued)

(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL/PCI Output Module Timing										
t _{DLH}	Data-to-Pad LOW to HIGH	1.5		1.7		2.0		2.3		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.9		2.2		2.4		2.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.3		2.6		3.0		3.5		ns
t _{ENZH}	Enable-to-Pad, Z to H	1.5		1.7		1.9		2.3		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.7		3.1		3.5		4.1		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.9		3.3		3.7		4.4		ns
PCI Output Module Timing ³										
t _{DLH}	Data-to-Pad LOW to HIGH	1.8		2.0		2.3		2.7		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.7		2.0		2.2		2.6		ns
t _{ENZL}	Enable-to-Pad, Z to L	0.8		1.0		1.1		1.3		ns
t _{ENZH}	Enable-to-Pad, Z to H	1.2		1.2		1.5		1.8		ns
t _{ENLZ}	Enable-to-Pad, L to Z	1.0		1.1		1.3		1.5		ns
t _{ENHZ}	Enable-to-Pad, H to Z	1.1		1.3		1.5		1.7		ns
TTL Output Module Timing										
t _{DLH}	Data-to-Pad LOW to HIGH	2.1		2.5		2.8		3.3		ns
t _{DHL}	Data-to-Pad HIGH to LOW	2.0		2.3		2.6		3.1		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.5		2.9		3.2		3.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.0		3.5		3.9		4.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.3		2.7		3.1		3.6		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.9		3.3		3.7		4.4		ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 10 pF loading.

Package Pin Assignments

84-Pin PLCC

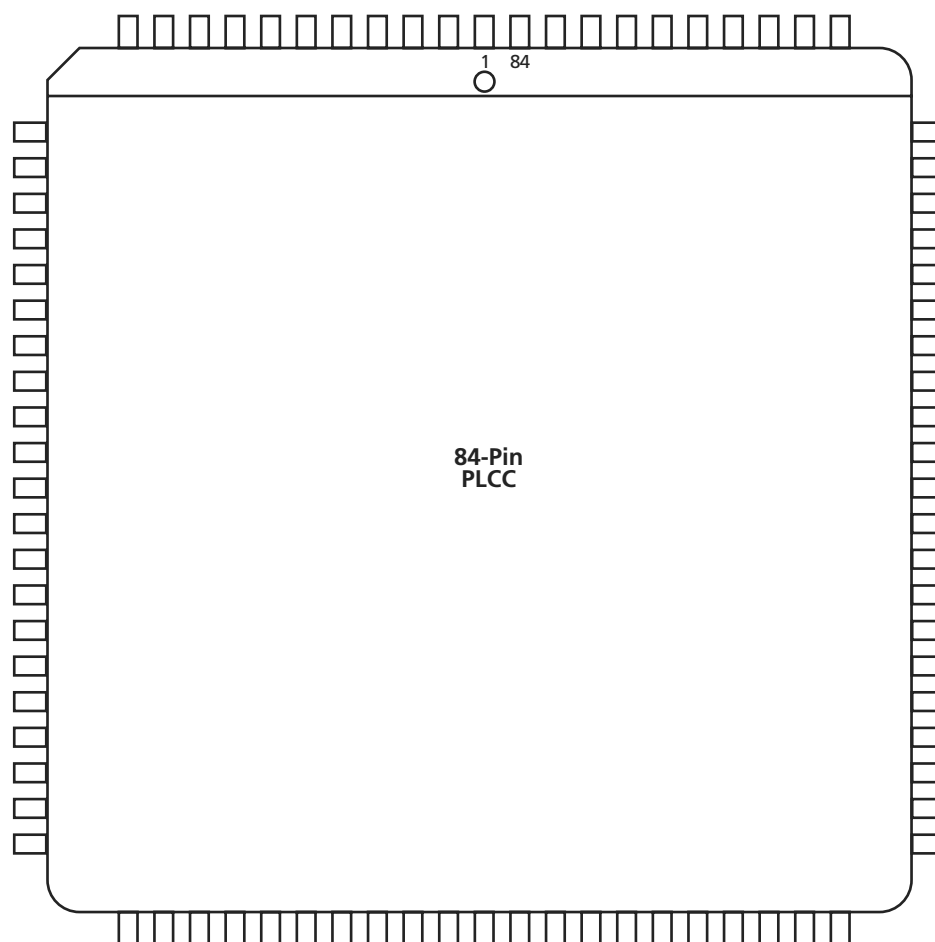


Figure 2-1 • 84-Pin PLCC (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

208-Pin PQFP

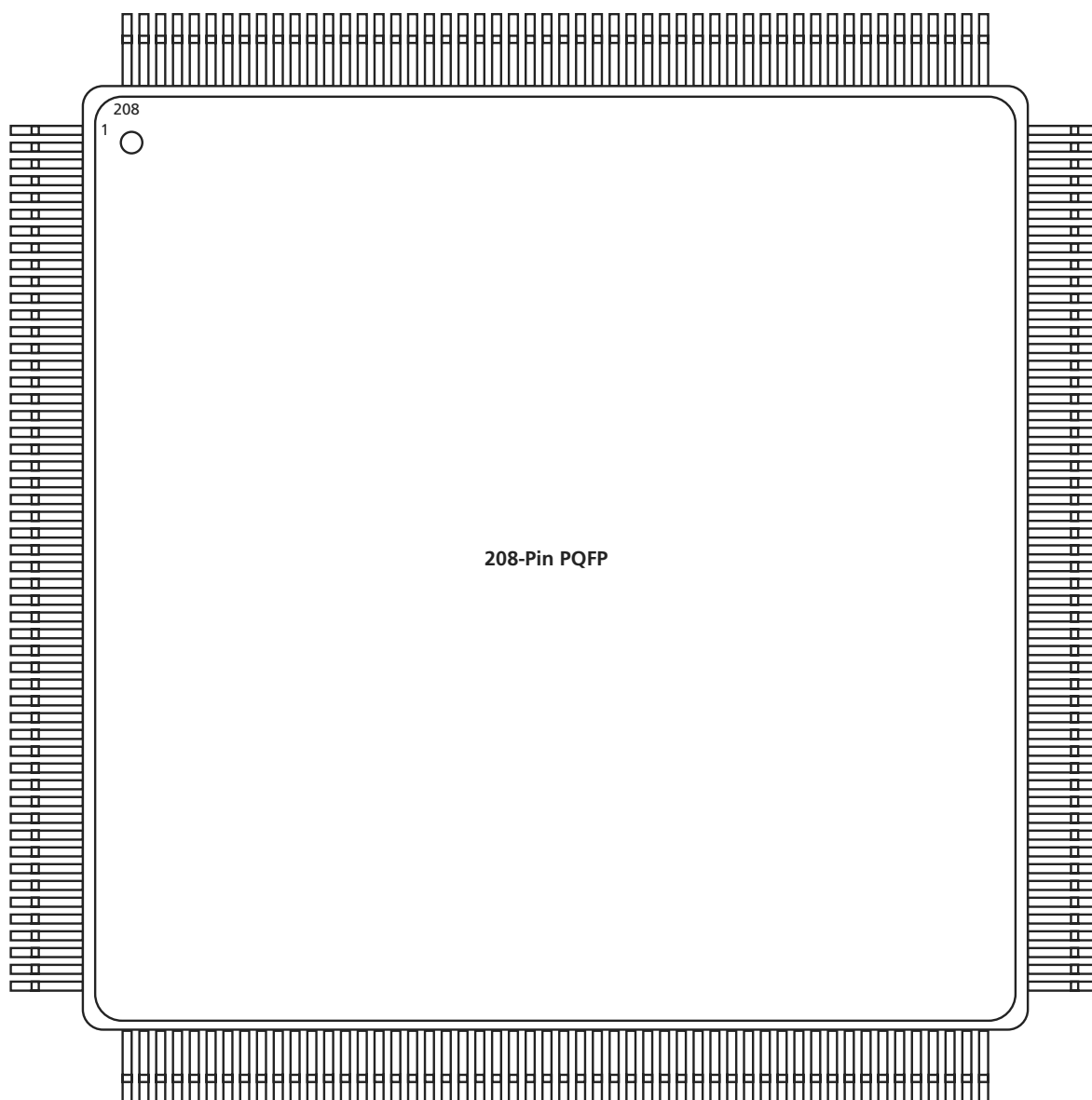


Figure 2-2 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	NC	I/O	I/O
5	I/O	I/O	I/O
6	NC	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	I/O	I/O	I/O
11	TMS	TMS	TMS
12	V _{CCI}	V _{CCI}	V _{CCI}
13	I/O	I/O	I/O
14	NC	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	NC	I/O	I/O
24	I/O	I/O	I/O
25	V _{CCR}	V _{CCR}	V _{CCR}
26	GND	GND	GND
27	V _{CCA}	V _{CCA}	V _{CCA}
28	GND	GND	GND
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	NC	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	I/O	I/O
36	I/O	I/O	I/O

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	NC	I/O	I/O
40	V _{CCI}	V _{CCI}	V _{CCI}
41	V _{CCA}	V _{CCA}	V _{CCA}
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	NC	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	I/O	I/O	I/O
52	GND	GND	GND
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	V _{CCI}	V _{CCI}	V _{CCI}
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65*	I/O	I/O	NC*
66	I/O	I/O	I/O
67	NC	I/O	I/O
68	I/O	I/O	I/O
69	I/O	I/O	I/O
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

176-Pin TQFP

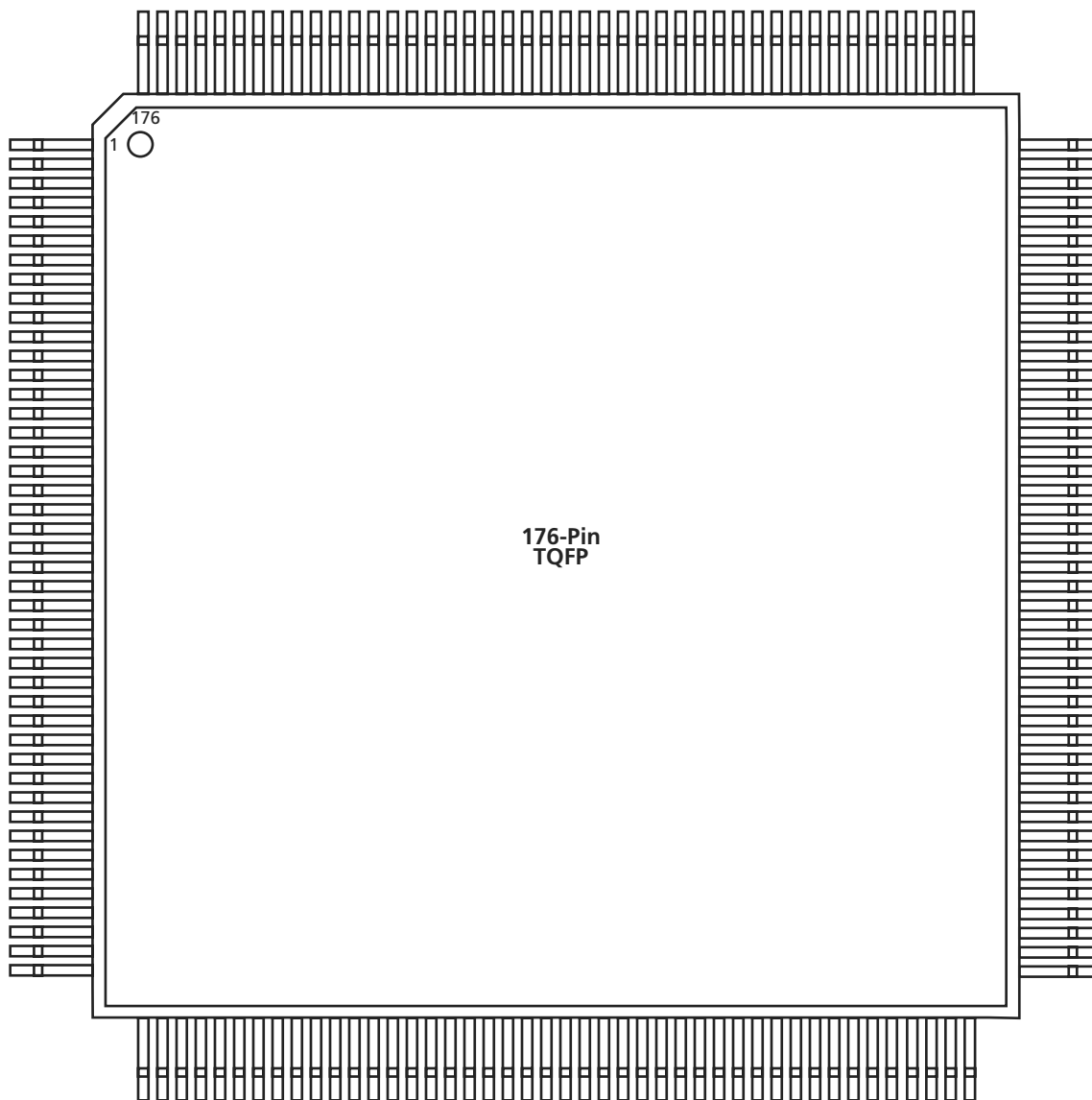


Figure 2-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
69	HCLK	HCLK	HCLK
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	I/O	I/O	I/O
81	NC	I/O	I/O
82	V _{CCI}	V _{CCI}	V _{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	TDO, I/O	TDO, I/O	TDO, I/O
88	I/O	I/O	I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	V _{CCI}	V _{CCI}	V _{CCI}
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	GND	GND	GND
109	V _{CCA}	V _{CCA}	V _{CCA}
110	GND	GND	GND
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	I/O	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	NC	I/O	I/O
119	I/O	I/O	I/O
120	NC	I/O	I/O
121	NC	I/O	I/O
122	V _{CCA}	V _{CCA}	V _{CCA}
123	GND	GND	GND
124	V _{CCI}	V _{CCI}	V _{CCI}
125	I/O	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	NC	I/O	I/O
132	NC	I/O	I/O
133	GND	GND	GND
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	I/O	I/O	I/O
146	I/O	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	CLKA	CLKA	CLKA
153	CLKB	CLKB	CLKB
154	V _{CCR}	V _{CCR}	V _{CCR}
155	GND	GND	GND
156	V _{CCA}	V _{CCA}	V _{CCA}

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
157	PRA, I/O	PRA, I/O	PRA, I/O
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	V _{CCI}	V _{CCI}	V _{CCI}
170	I/O	I/O	I/O
171	NC	I/O	I/O
172	NC	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	TCK, I/O	TCK, I/O	TCK, I/O

313-Pin PBGA

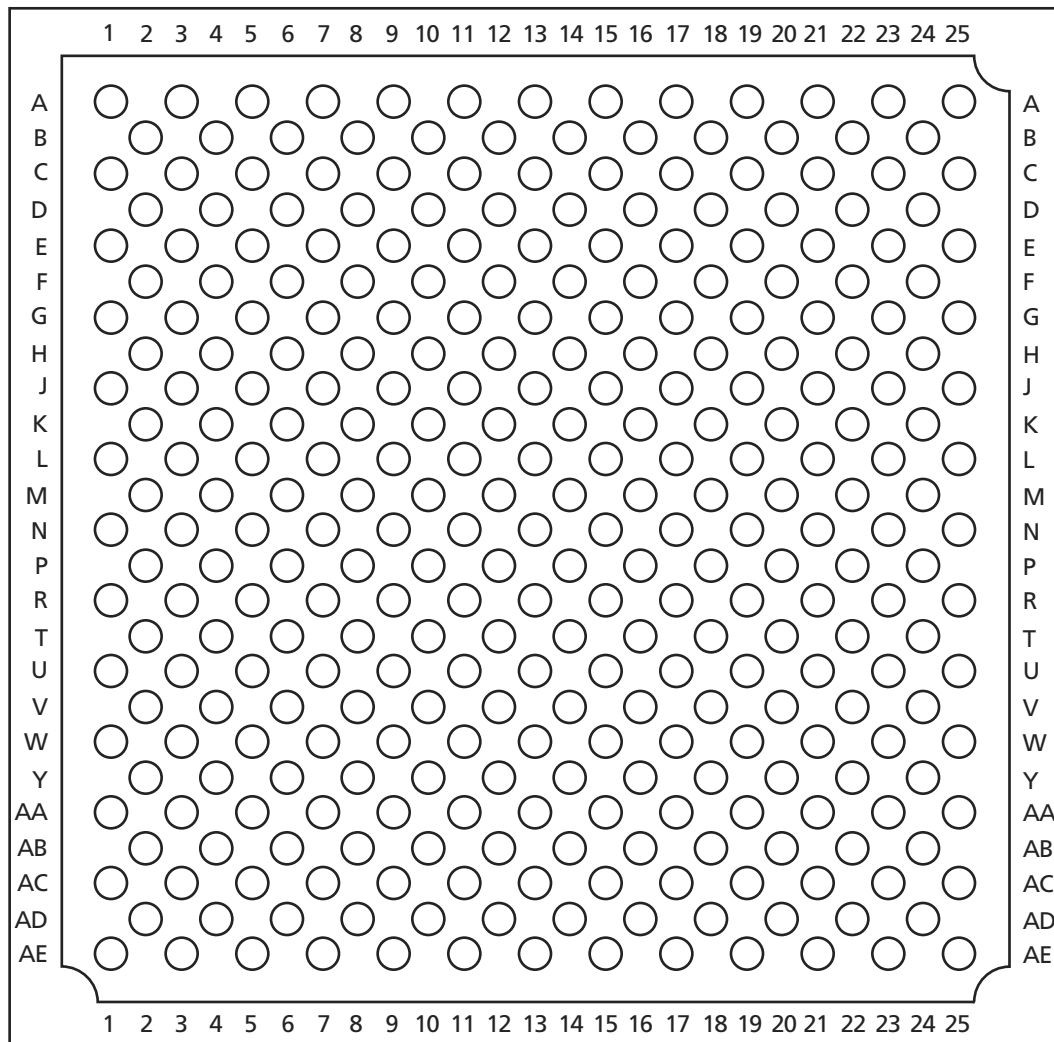


Figure 2-6 • 313-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
A1	GND	AA13	I/O	AC2	V _{CCI}	B14	I/O
A2	GND	AA14	I/O	AC3	NC	B15	I/O
A3	V _{CCI}	AA15	I/O	AC4	I/O	B16	I/O
A4	NC	AA16	I/O	AC5	I/O	B17	I/O
A5	I/O	AA17	I/O	AC6	I/O	B18	I/O
A6	I/O	AA18	I/O	AC7	I/O	B19	I/O
A7	V _{CCI}	AA19	I/O	AC8	I/O	B20	I/O
A8	NC	AA20	TDO, I/O	AC9	V _{CCI}	B21	I/O
A9	I/O	AA21	V _{CCI}	AC10	I/O	B22	GND
A10	I/O	AA22	I/O	AC11	I/O	B23	V _{CCI}
A11	I/O	AA23	V _{CCI}	AC12	I/O	C1	NC
A12	I/O	AB1	I/O	AC13	I/O	C2	TDI, I/O
A13	CLKB	AB2	GND	AC14	I/O	C3	GND
A14	I/O	AB3	I/O	AC15	NC	C4	I/O
A15	I/O	AB4	I/O	AC16	I/O	C5	I/O
A16	I/O	AB5	I/O	AC17	I/O	C6	I/O
A17	I/O	AB6	I/O	AC18	I/O	C7	I/O
A18	I/O	AB7	I/O	AC19	I/O	C8	I/O
A19	I/O	AB8	I/O	AC20	I/O	C9	I/O
A20	I/O	AB9	I/O	AC21	NC	C10	I/O
A21	NC	AB10	I/O	AC22	V _{CCI}	C11	I/O
A22	V _{CCI}	AB11	PRB, I/O	AC23	GND	C12	I/O
A23	GND	AB12	I/O	B1	V _{CCI}	C13	I/O
AA1	V _{CCI}	AB13	HCLK	B2	GND	C14	I/O
AA2	I/O	AB14	I/O	B3	I/O	C15	I/O
AA3	GND	AB15	I/O	B4	I/O	C16	I/O
AA4	I/O	AB16	I/O	B5	I/O	C17	I/O
AA5	I/O	AB17	I/O	B6	I/O	C18	I/O
AA6	I/O	AB18	I/O	B7	I/O	C19	I/O
AA7	I/O	AB19	I/O	B8	I/O	C20	I/O
AA8	I/O	AB20	I/O	B9	I/O	C21	V _{CCI}
AA9	I/O	AB21	I/O	B10	I/O	C22	GND
AA10	I/O	AB22	GND	B11	I/O	C23	NC
AA11	I/O	AB23	I/O	B12	PRA, I/O	D1	I/O
AA12	I/O	AC1	GND	B13	CLKA	D2	I/O

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