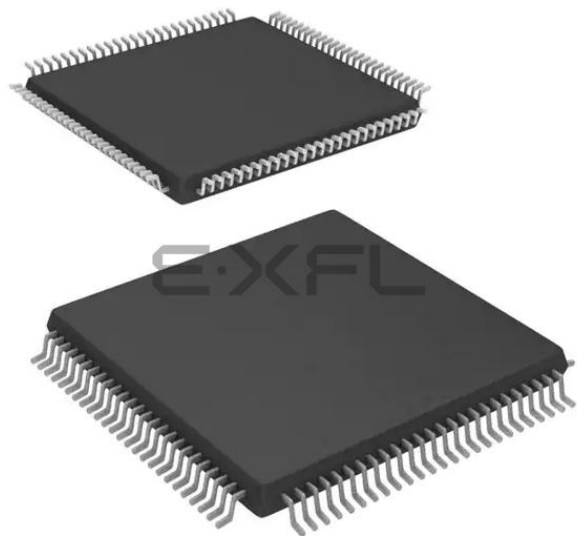




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx16p-vq100m

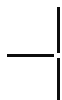


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The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional

flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.

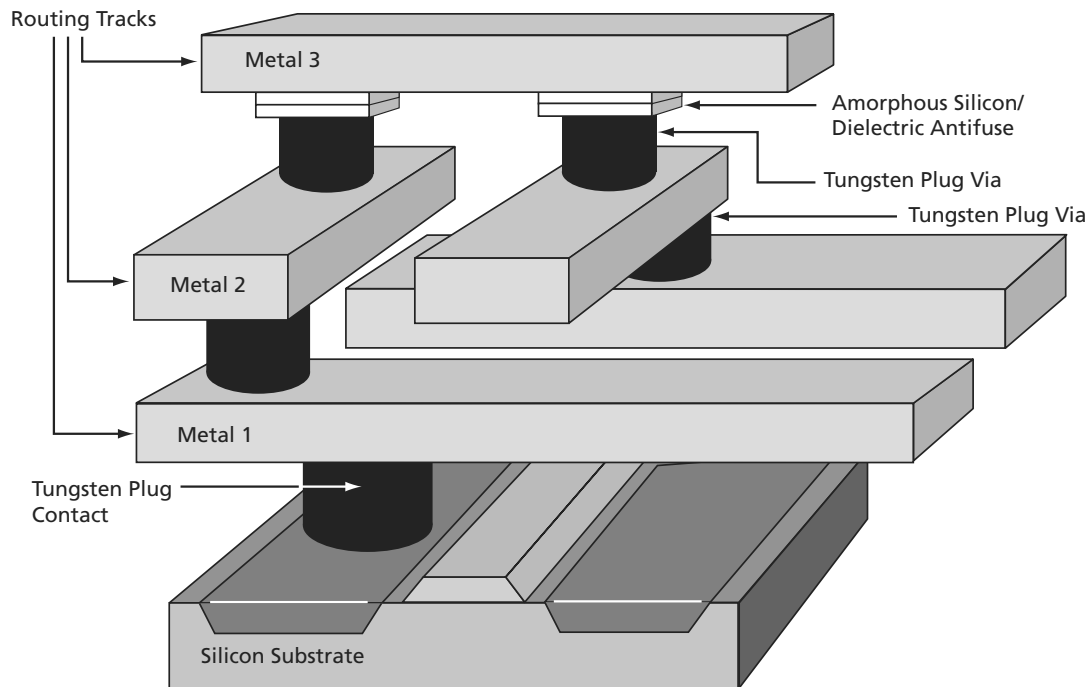


Figure 1-1 • SX Family Interconnect Elements

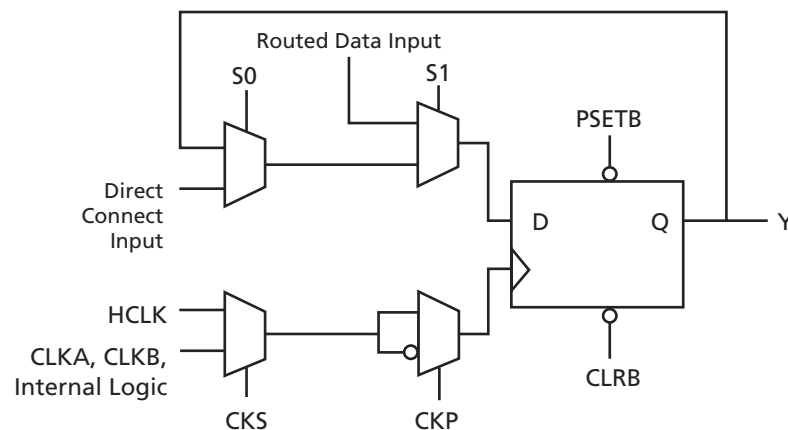


Figure 1-2 • R-Cell

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility

enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

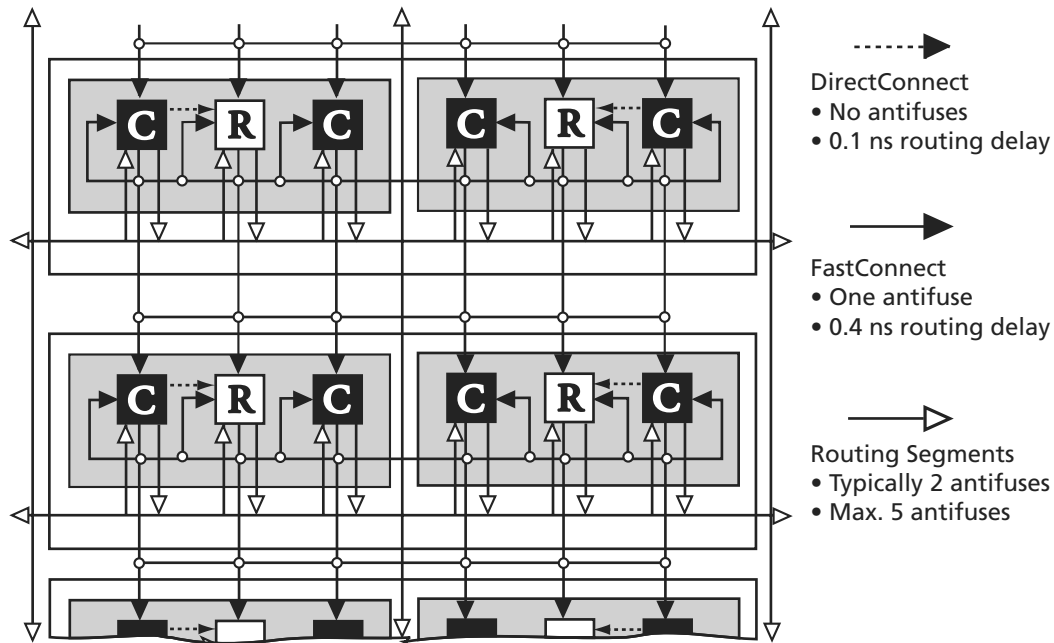


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

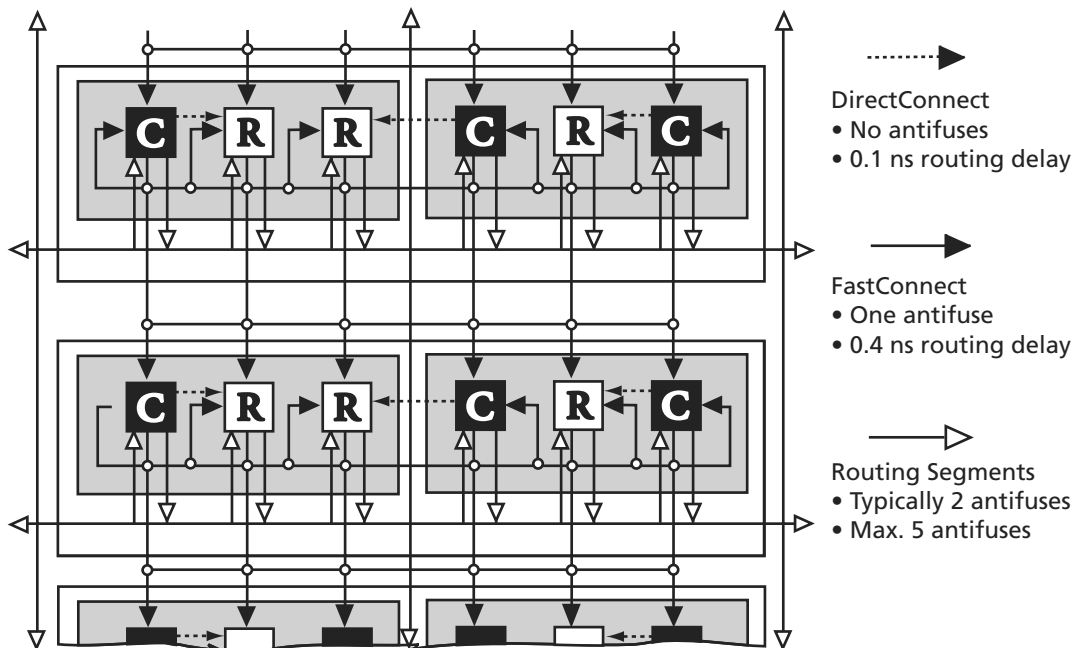


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

Power-Up Sequencing

Table 1-10 • Power-Up Sequencing

V _{CCA}	V _{CCR}	V _{CCI}	Power-Up Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Note: No inputs should be driven (high or low) before completion of power-up.

Power-Down Sequencing

Table 1-11 • Power-Down Sequencing

V _{CCA}	V _{CCR}	V _{CCI}	Power-Down Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Note: No inputs should be driven (high or low) after the beginning of the power-down sequence.

Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}}$$

EQ 1-5

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • Standby Power

I _{CC}	V _{CC}	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

$$P_{\text{DC}} = (I_{\text{standby}}) \times V_{\text{CCA}} + (I_{\text{standby}}) \times V_{\text{CCR}} + (I_{\text{standby}}) \times V_{\text{CCI}} + xV_{\text{OL}} \times I_{\text{OL}} + y(V_{\text{CCI}} - V_{\text{OH}}) \times V_{\text{OH}}$$

EQ 1-6

AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-7

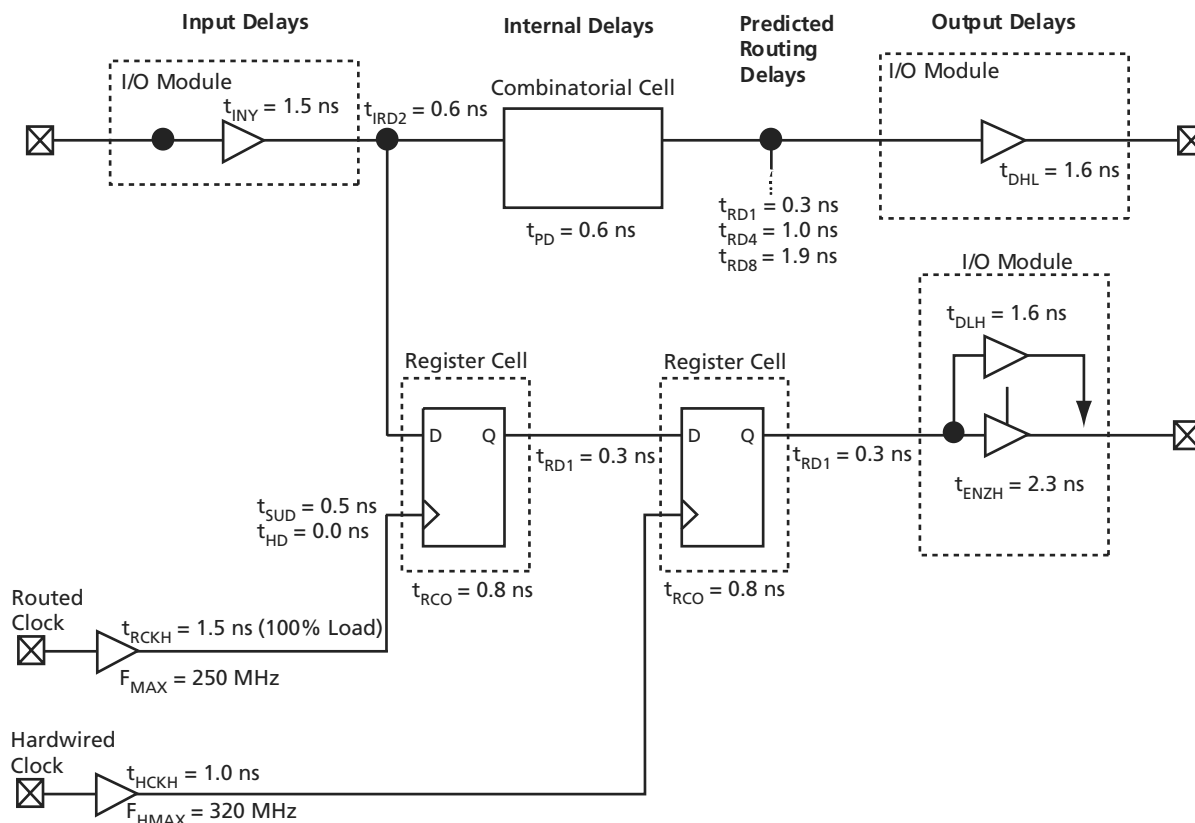
$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 \times (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 \times (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 \times (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-8

Definition of Terms Used in Formula

- m = Number of logic modules switching at f_m
- n = Number of input buffers switching at f_n
- p = Number of output buffers switching at f_p
- q₁ = Number of clock loads on the first routed array clock
- q₂ = Number of clock loads on the second routed array clock
- x = Number of I/Os at logic low
- y = Number of I/Os at logic high
- r₁ = Fixed capacitance due to first routed array clock
- r₂ = Fixed capacitance due to second routed array clock
- s₁ = Number of clock loads on the dedicated array clock
- C_{EQM} = Equivalent capacitance of logic modules in pF
- C_{EQI} = Equivalent capacitance of input buffers in pF
- C_{EQO} = Equivalent capacitance of output buffers in pF
- C_{EQCR} = Equivalent capacitance of routed array clock in pF
- C_{EQHV} = Variable capacitance of dedicated array clock
- C_{EQHF} = Fixed capacitance of dedicated array clock
- C_L = Output lead capacitance in pF
- f_m = Average logic module switching rate in MHz
- f_n = Average input buffer switching rate in MHz
- f_p = Average output buffer switching rate in MHz
- f_{q1} = Average first routed array clock rate in MHz
- f_{q2} = Average second routed array clock rate in MHz
- f_{s1} = Average dedicated array clock rate in MHz

SX Timing Model



Note: Values shown for A54SX08-3, worst-case commercial conditions.

Figure 1-12 • SX Timing Model

Hardwired Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.0 = 1.3 \text{ ns} \end{aligned}$$

EQ 1-15

Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.0 + 0.8 + 0.3 + 1.6 = 3.7 \text{ ns} \end{aligned}$$

EQ 1-16

Routed Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.5 = 0.8 \text{ ns} \end{aligned}$$

EQ 1-17

Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.52 + 0.8 + 0.3 + 1.6 = 4.2 \text{ ns} \end{aligned}$$

EQ 1-18

Table 1-19 • A54SX16P Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL/PCI Output Module Timing										
t _{DLH}	Data-to-Pad LOW to HIGH	1.5		1.7		2.0		2.3		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.9		2.2		2.4		2.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.3		2.6		3.0		3.5		ns
t _{ENZH}	Enable-to-Pad, Z to H	1.5		1.7		1.9		2.3		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.7		3.1		3.5		4.1		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.9		3.3		3.7		4.4		ns
PCI Output Module Timing ³										
t _{DLH}	Data-to-Pad LOW to HIGH	1.8		2.0		2.3		2.7		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.7		2.0		2.2		2.6		ns
t _{ENZL}	Enable-to-Pad, Z to L	0.8		1.0		1.1		1.3		ns
t _{ENZH}	Enable-to-Pad, Z to H	1.2		1.2		1.5		1.8		ns
t _{ENLZ}	Enable-to-Pad, L to Z	1.0		1.1		1.3		1.5		ns
t _{ENHZ}	Enable-to-Pad, H to Z	1.1		1.3		1.5		1.7		ns
TTL Output Module Timing										
t _{DLH}	Data-to-Pad LOW to HIGH	2.1		2.5		2.8		3.3		ns
t _{DHL}	Data-to-Pad HIGH to LOW	2.0		2.3		2.6		3.1		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.5		2.9		3.2		3.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.0		3.5		3.9		4.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.3		2.7		3.1		3.6		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.9		3.3		3.7		4.4		ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 10 pF loading.

A54SX32 Timing Characteristics

Table 1-20 • **A54SX32 Timing Characteristics**
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ¹										
t _{PD}	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays ²										
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{RD2}	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t _{RD3}	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{RD4}	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t _{RD8}	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t _{RD12}	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns
R-Cell Timing										
t _{RCO}	Sequential Clock-to-Q	0.8		1.1		1.3		1.4		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t _{INYH}	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t _{INYL}	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays ²										
t _{IRD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{IRD2}	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t _{IRD3}	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{IRD4}	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t _{IRD8}	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t _{IRD12}	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} the loading is 5 pF.

Table 1-20 • **A54SX32 Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t _{HCKH}	Input LOW to HIGH (pad to R-Cell input)	1.9		2.1		2.4		2.8		ns
t _{HCKL}	Input HIGH to LOW (pad to R-Cell input)	1.9		2.1		2.4		2.8		ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew	0.3		0.4		0.4		0.5		ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t _{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)	2.4		2.7		3.0		3.5		ns
t _{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell input)	2.4		2.7		3.1		3.6		ns
t _{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)	2.7		3.0		3.5		4.1		ns
t _{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)	2.7		3.1		3.6		4.2		ns
t _{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)	2.7		3.1		3.5		4.1		ns
t _{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)	2.8		3.2		3.6		4.3		ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (light load)	0.85		0.98		1.1		1.3		ns
t _{RCKSW}	Maximum Skew (50% load)	1.23		1.4		1.6		1.9		ns
t _{RCKSW}	Maximum Skew (100% load)	1.30		1.5		1.7		2.0		ns
TTL Output Module Timing ³										
t _{DLH}	Data-to-Pad LOW to HIGH	1.6		1.9		2.1		2.5		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.6		1.9		2.1		2.5		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.8		3.2		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3		2.7		3.1		3.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	1.4		1.7		1.9		2.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	1.3		1.5		1.7		2.0		ns

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} the loading is 5 pF.

Package Pin Assignments

84-Pin PLCC

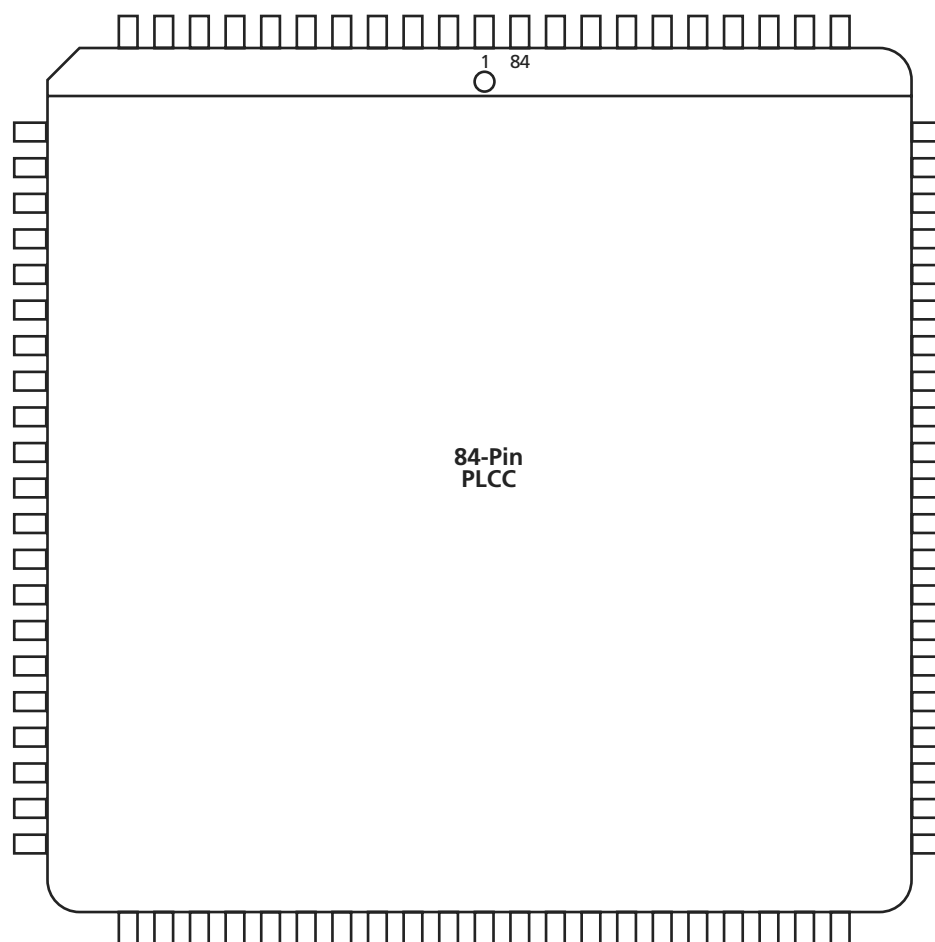


Figure 2-1 • 84-Pin PLCC (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
73	NC	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND
78	V _{CCA}	V _{CCA}	V _{CCA}
79	GND	GND	GND
80	V _{CCR}	V _{CCR}	V _{CCR}
81	I/O	I/O	I/O
82	HCLK	HCLK	HCLK
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	NC	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	NC	I/O	I/O
89	I/O	I/O	I/O
90	I/O	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	NC	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	NC	I/O	I/O
98	V _{CCI}	V _{CCI}	V _{CCI}
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	I/O	I/O
107	I/O	I/O	I/O
108	NC	I/O	I/O

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	V _{CCA}	V _{CCA}	V _{CCA}
115	V _{CCI}	V _{CCI}	V _{CCI}
116	NC	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	NC	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	NC	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	NC	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	GND	GND	GND
130	V _{CCA}	V _{CCA}	V _{CCA}
131	GND	GND	GND
132	V _{CCR}	V _{CCR}	V _{CCR}
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	I/O	I/O	I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

144-Pin TQFP

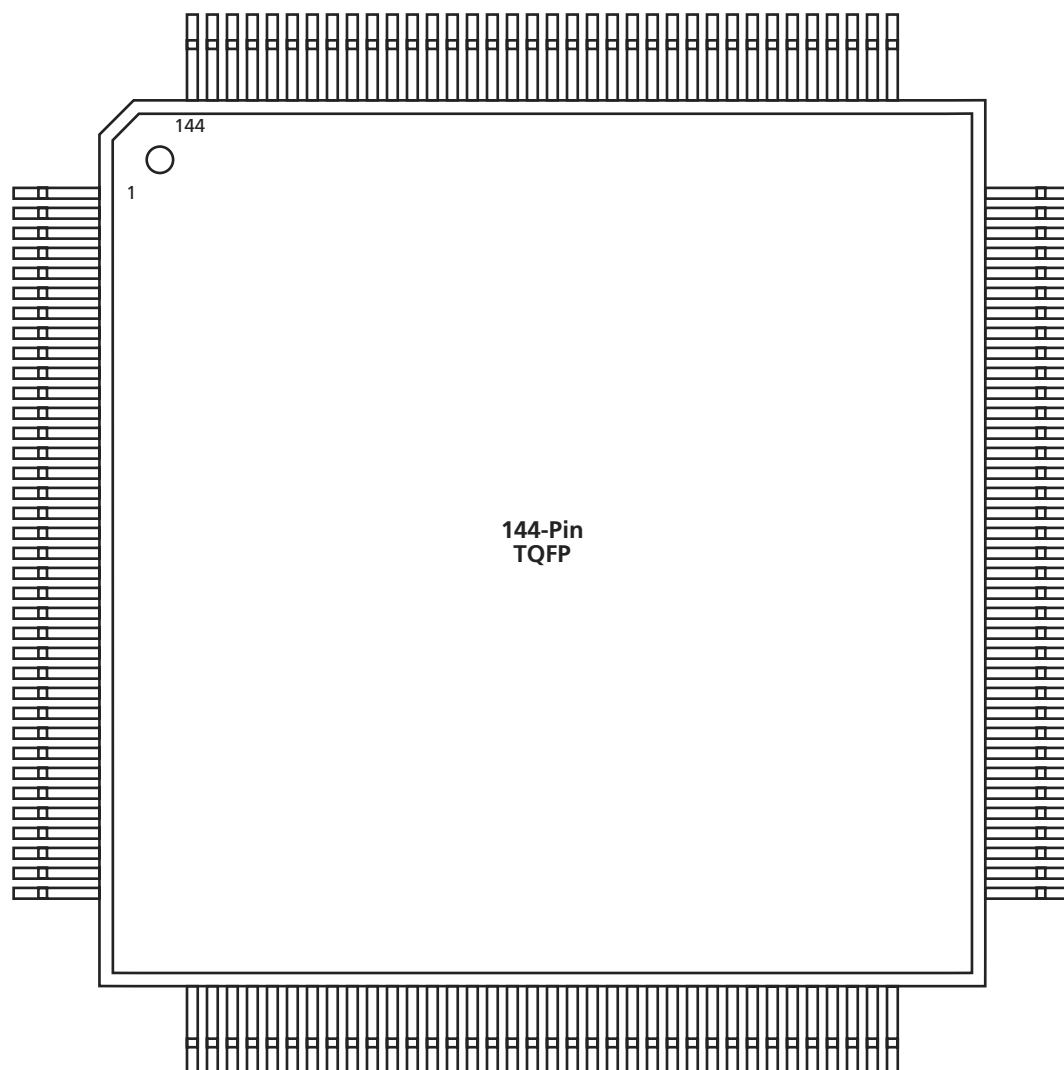


Figure 2-3 • 144-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V _{CCA}	V _{CCA}	V _{CCA}
80	V _{CCI}	V _{CCI}	V _{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V _{CCA}	V _{CCA}	V _{CCA}
90	V _{CCR}	V _{CCR}	V _{CCR}
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V _{CCI}	V _{CCI}	V _{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
109	GND	GND	GND
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V _{CCI}	V _{CCI}	V _{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	V _{CCR}	V _{CCR}	V _{CCR}
128	GND	GND	GND
129	V _{CCA}	V _{CCA}	V _{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

176-Pin TQFP

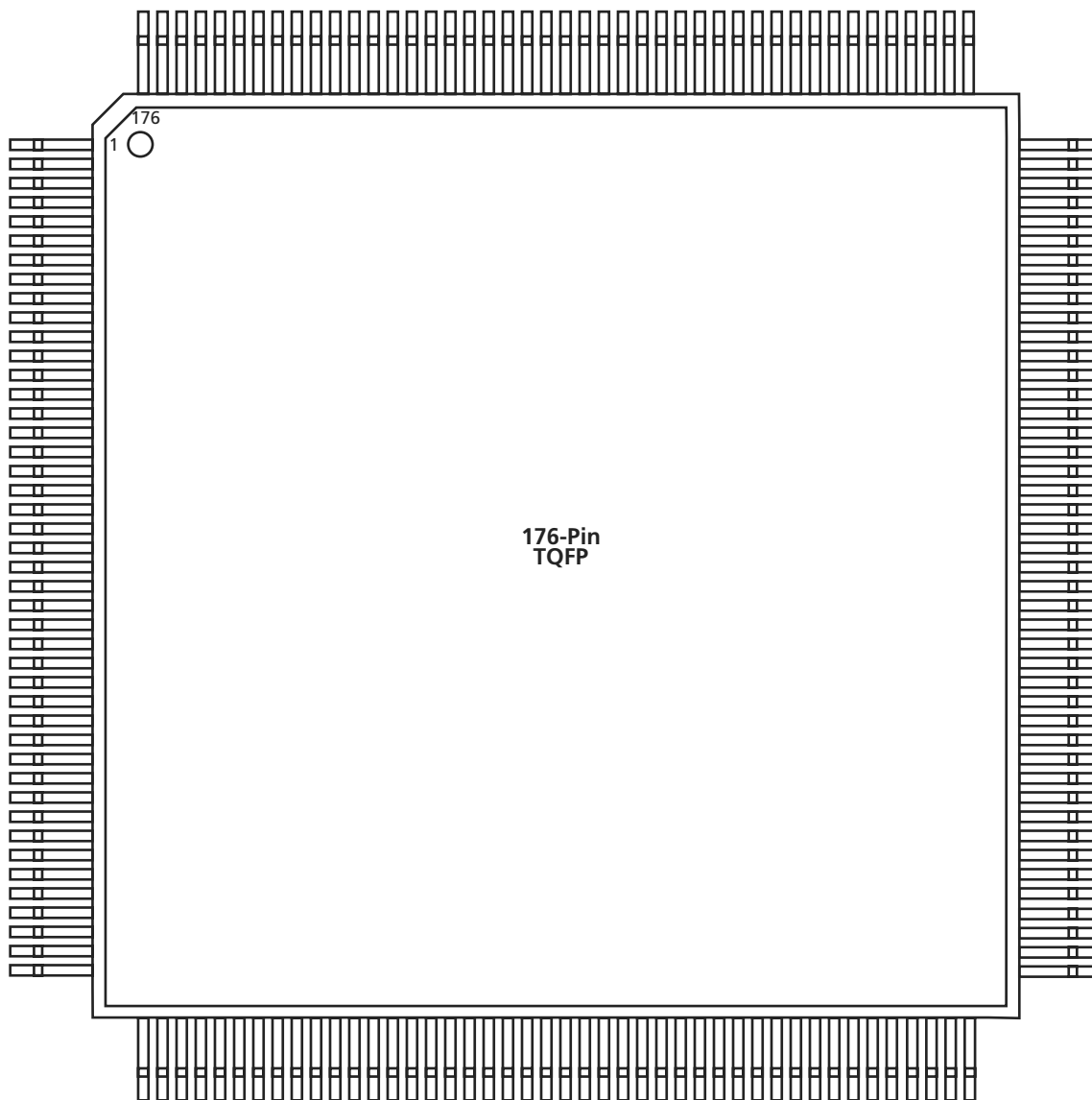


Figure 2-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V _{CCI}	V _{CCI}	V _{CCI}
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V _{CCA}	V _{CCA}	V _{CCA}
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V _{CCI}	V _{CCI}	V _{CCI}
33	V _{CCA}	V _{CCA}	V _{CCA}
34	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V _{CCI}	V _{CCI}	V _{CCI}
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V _{CCA}	V _{CCA}	V _{CCA}
67	V _{CCR}	V _{CCR}	V _{CCR}
68	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
69	HCLK	HCLK	HCLK
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	I/O	I/O	I/O
81	NC	I/O	I/O
82	V _{CCI}	V _{CCI}	V _{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	TDO, I/O	TDO, I/O	TDO, I/O
88	I/O	I/O	I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	V _{CCI}	V _{CCI}	V _{CCI}
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	GND	GND	GND
109	V _{CCA}	V _{CCA}	V _{CCA}
110	GND	GND	GND
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	I/O	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	NC	I/O	I/O
119	I/O	I/O	I/O
120	NC	I/O	I/O
121	NC	I/O	I/O
122	V _{CCA}	V _{CCA}	V _{CCA}
123	GND	GND	GND
124	V _{CCI}	V _{CCI}	V _{CCI}
125	I/O	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	NC	I/O	I/O
132	NC	I/O	I/O
133	GND	GND	GND
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O

100-Pin VQFP

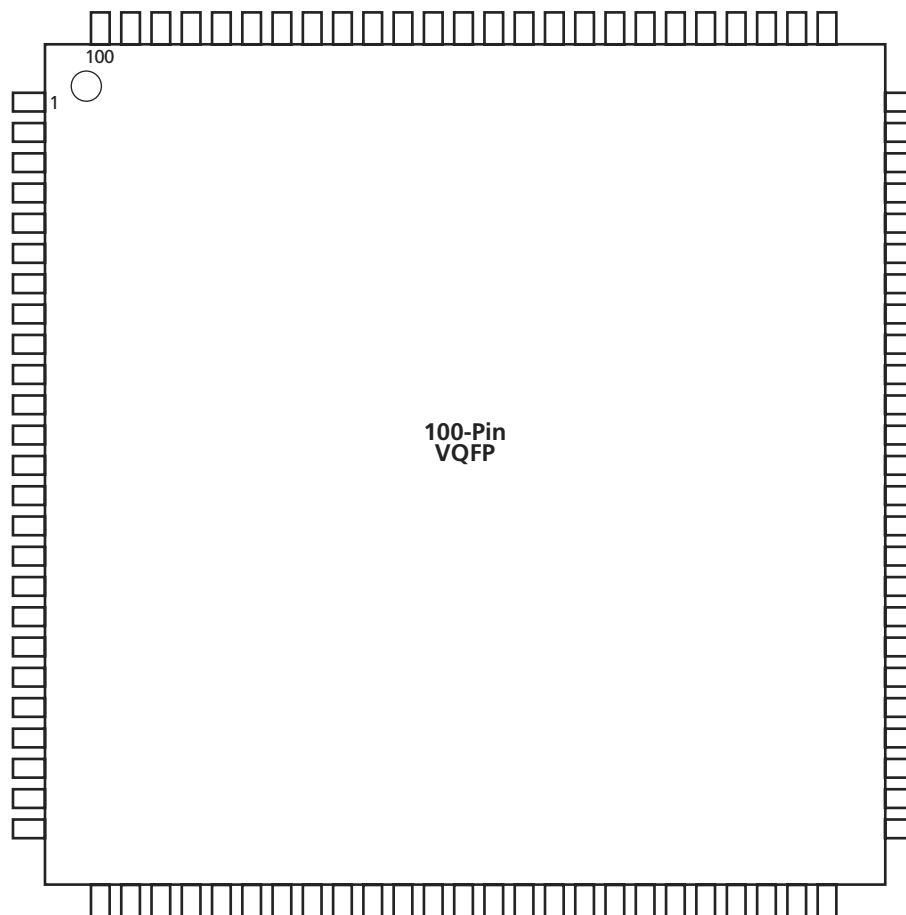


Figure 2-5 • 100-Pin VQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

313-Pin PBGA		313-Pin PBGA		313-Pin PBGA		313-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
H20	I/O	L25	I/O	R5	I/O	V10	I/O
H22	V _{CCI}	M2	I/O	R7	I/O	V12	I/O
H24	I/O	M4	I/O	R9	I/O	V14	I/O
J1	I/O	M6	I/O	R11	I/O	V16	NC
J3	I/O	M8	I/O	R13	GND	V18	I/O
J5	I/O	M10	I/O	R15	I/O	V20	I/O
J7	NC	M12	GND	R17	I/O	V22	V _{CCA}
J9	I/O	M14	GND	R19	I/O	V24	V _{CCI}
J11	I/O	M16	V _{CCI}	R21	I/O	W1	I/O
J13	CLKA	M18	I/O	R23	I/O	W3	I/O
J15	I/O	M20	I/O	R25	I/O	W5	I/O
J17	I/O	M22	I/O	T2	I/O	W7	NC
J19	I/O	M24	I/O	T4	I/O	W9	I/O
J21	GND	N1	I/O	T6	I/O	W11	I/O
J23	I/O	N3	V _{CCA}	T8	I/O	W13	V _{CCI}
J25	I/O	N5	V _{CCR}	T10	I/O	W15	I/O
K2	I/O	N7	I/O	T12	I/O	W17	I/O
K4	I/O	N9	V _{CCI}	T14	HCLK	W19	I/O
K6	I/O	N11	GND	T16	I/O	W21	I/O
K8	V _{CCI}	N13	GND	T18	I/O	W23	I/O
K10	I/O	N15	GND	T20	I/O	W25	I/O
K12	I/O	N17	I/O	T22	I/O	Y2	I/O
K14	I/O	N19	I/O	T24	I/O	Y4	I/O
K16	I/O	N21	I/O	U1	I/O	Y6	I/O
K18	I/O	N23	V _{CCR}	U3	I/O	Y8	I/O
K20	V _{CCA}	N25	V _{CCA}	U5	V _{CCI}	Y10	I/O
K22	I/O	P2	I/O	U7	I/O	Y12	I/O
K24	I/O	P4	I/O	U9	I/O	Y14	I/O
L1	I/O	P6	I/O	U11	I/O	Y16	I/O
L3	I/O	P8	I/O	U13	I/O	Y18	I/O
L5	I/O	P10	I/O	U15	I/O	Y20	NC
L7	I/O	P12	GND	U17	I/O	Y22	I/O
L9	I/O	P14	GND	U19	I/O	Y24	NC
L11	I/O	P16	I/O	U21	I/O		
L13	GND	P18	I/O	U23	I/O		
L15	I/O	P20	NC	U25	I/O		
L17	I/O	P22	I/O	V2	V _{CCA}		
L19	I/O	P24	I/O	V4	I/O		
L21	I/O	R1	I/O	V6	I/O		
L23	I/O	R3	I/O	V8	I/O		

329-Pin PBGA

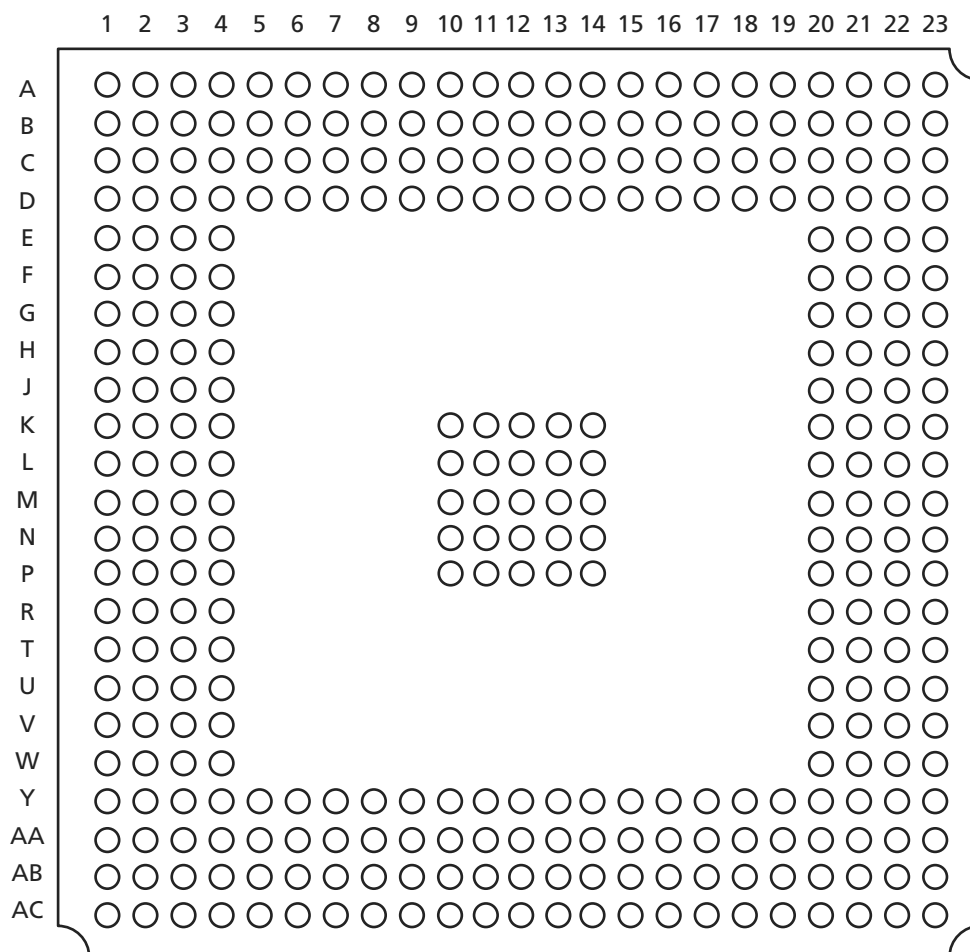


Figure 2-7 • 329-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

144-Pin FBGA

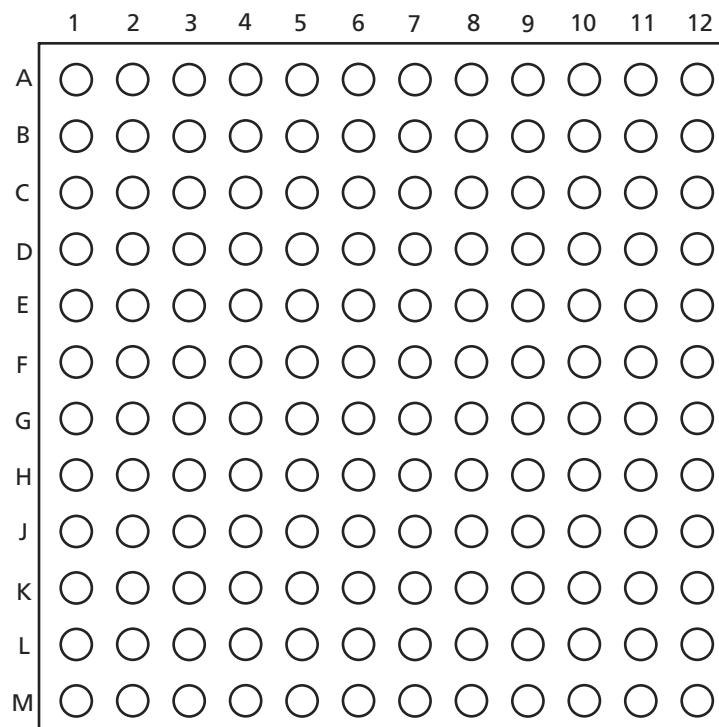


Figure 2-8 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.