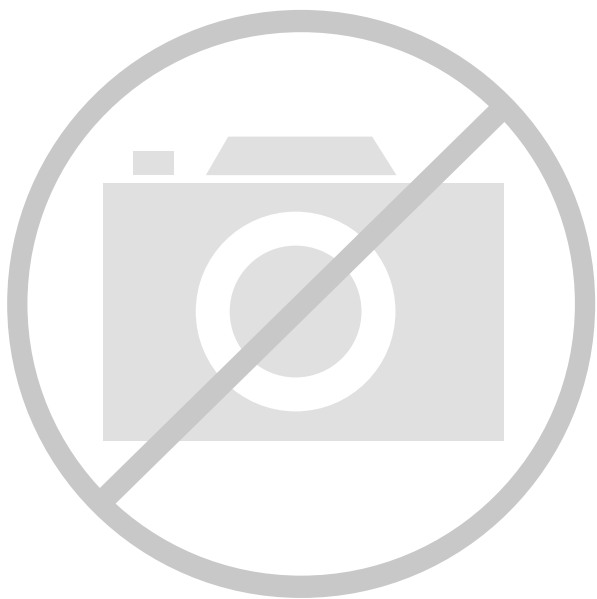




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	249
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	313-BBGA
Supplier Device Package	313-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx32-1bg313i

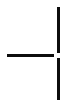


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The SX family chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *clusters*. There are two types of *clusters*: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (Figure 1-4). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

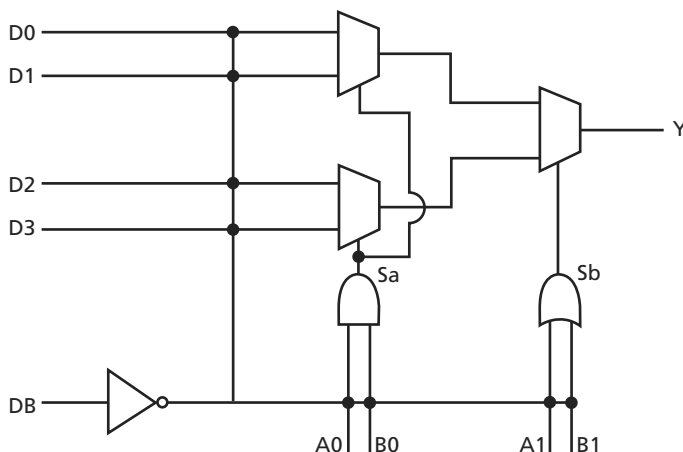


Figure 1-3 • C-Cell

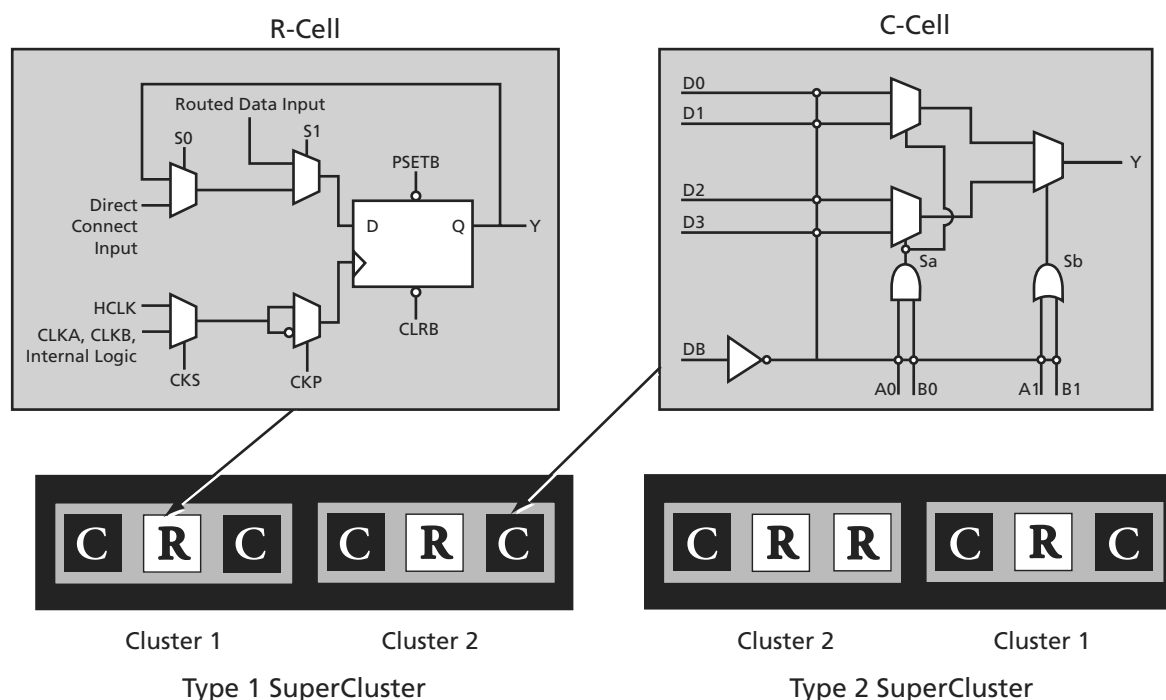


Figure 1-4 • Cluster Organization

A54SX16P DC Specifications (3.3 V PCI Operation)

Table 1-8 • A54SX16P DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		3.0	3.6	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CC}$	V
I_{IPU}	Input Pull-up Voltage ¹		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current ²	$0 < V_{IN} < V_{CC}$		± 10	μA
V_{OH}	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OUT} = 1500 \mu A$		$0.1V_{CC}$	V
C_{IN}	Input Pin Capacitance ³			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance ⁴			8	pF

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

Power-Up Sequencing

Table 1-10 • Power-Up Sequencing

V _{CCA}	V _{CCR}	V _{CCI}	Power-Up Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Note: No inputs should be driven (high or low) before completion of power-up.

Power-Down Sequencing

Table 1-11 • Power-Down Sequencing

V _{CCA}	V _{CCR}	V _{CCI}	Power-Down Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Note: No inputs should be driven (high or low) after the beginning of the power-down sequence.

Register Cell Timing Characteristics

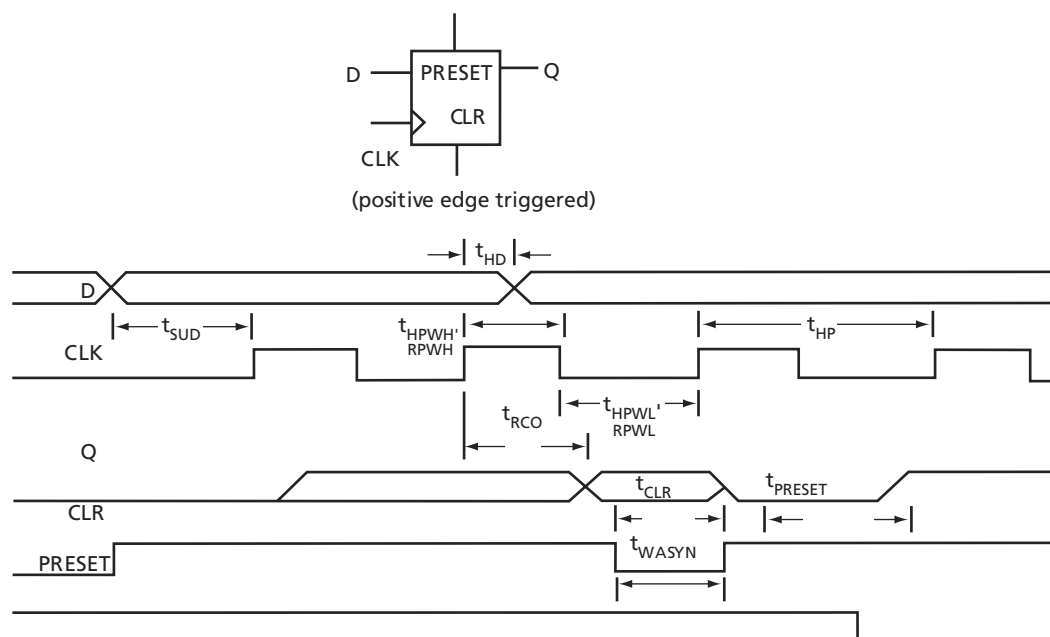


Figure 1-17 • Flip-Flops

Timing Characteristics

Timing characteristics for SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout ($FO = 24$) routing delays in the datasheet specifications section.

Timing Derating

SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Table 1-18 • A54SX16 Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t _{HCKH}	Input LOW to HIGH (pad to R-Cell input)	1.2		1.4		1.5		1.8		ns
t _{HCKL}	Input HIGH to LOW (pad to R-Cell input)	1.2		1.4		1.6		1.9		ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew	0.2		0.2		0.3		0.3		ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t _{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)	1.6		1.8		2.1		2.5		ns
t _{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell input)	1.8		2.0		2.3		2.7		ns
t _{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)	1.8		2.1		2.5		2.8		ns
t _{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t _{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)	1.8		2.1		2.4		2.8		ns
t _{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (light load)	0.5		0.5		0.5		0.7		ns
t _{RCKSW}	Maximum Skew (50% load)	0.5		0.6		0.7		0.8		ns
t _{RCKSW}	Maximum Skew (100% load)	0.5		0.6		0.7		0.8		ns
TTL Output Module Timing ³										
t _{DLH}	Data-to-Pad LOW to HIGH	1.6		1.9		2.1		2.5		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.6		1.9		2.1		2.5		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.8		3.2		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3		2.7		3.1		3.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	1.4		1.7		1.9		2.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	1.3		1.5		1.7		2.0		ns

Notes:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} , the loading is 5 pF.

Table 1-19 • A54SX16P Timing Characteristics (Continued)

(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t _{HCKH}	Input LOW to HIGH (pad to R-Cell input)	1.2		1.4		1.5		1.8		ns
t _{HCKL}	Input HIGH to LOW (pad to R-Cell input)	1.2		1.4		1.6		1.9		ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew	0.2		0.2		0.3		0.3		ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t _{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)	1.6		1.8		2.1		2.5		ns
t _{RCKL}	Input HIGH to LOW (Light Load) (pad to R-Cell input)	1.8		2.0		2.3		2.7		ns
t _{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)	1.8		2.1		2.5		2.8		ns
t _{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t _{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)	1.8		2.1		2.4		2.8		ns
t _{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (light load)	0.5		0.5		0.5		0.7		ns
t _{RCKSW}	Maximum Skew (50% load)	0.5		0.6		0.7		0.8		ns
t _{RCKSW}	Maximum Skew (100% load)	0.5		0.6		0.7		0.8		ns
TTL Output Module Timing										
t _{DLH}	Data-to-Pad LOW to HIGH	2.4		2.8		3.1		3.7		ns
t _{DHL}	Data-to-Pad HIGH to LOW	2.3		2.9		3.2		3.8		ns
t _{ENZL}	Enable-to-Pad, Z to L	3.0		3.4		3.9		4.6		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.3		3.8		4.3		5.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.3		2.7		3.0		3.5		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.8		3.2		3.7		4.3		ns

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 10 pF loading.

A54SX32 Timing Characteristics

Table 1-20 • **A54SX32 Timing Characteristics**
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ¹										
t _{PD}	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays ²										
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{RD2}	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t _{RD3}	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{RD4}	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t _{RD8}	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t _{RD12}	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns
R-Cell Timing										
t _{RCO}	Sequential Clock-to-Q	0.8		1.1		1.3		1.4		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t _{INYH}	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t _{INYL}	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays ²										
t _{IRD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{IRD2}	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t _{IRD3}	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{IRD4}	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t _{IRD8}	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t _{IRD12}	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} the loading is 5 pF.

Pin Description

CLKA/B Clock A and B

These pins are 3.3 V / 5.0 V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as bidirectional.)

GND Ground

LOW supply voltage.

HCLK Dedicated (hardwired) Array Clock

This pin is the 3.3 V / 5.0 V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, 3.3 V PCI or 5.0 V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

PRB, I/O Probe B

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-2 on page 1-6). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See Table 1-1 on page 1-5.

V_{CCA} Supply Voltage

Supply voltage for Array. See Table 1-1 on page 1-5.

V_{CCR} Supply Voltage

Supply voltage for input tolerance (required for internal biasing). See Table 1-1 on page 1-5.

84-Pin PLCC	
Pin Number	A54SX08 Function
1	V _{CCR}
2	GND
3	V _{CCA}
4	PRA, I/O
5	I/O
6	I/O
7	V _{CCI}
8	I/O
9	I/O
10	I/O
11	TCK, I/O
12	TDI, I/O
13	I/O
14	I/O
15	I/O
16	TMS
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V _{CCI}
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O

84-Pin PLCC	
Pin Number	A54SX08 Function
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V _{CCA}
42	GND
43	V _{CCR}
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V _{CCA}
60	V _{CCI}
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V _{CCA}
69	GND
70	I/O

84-Pin PLCC	
Pin Number	A54SX08 Function
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	CLKA
84	CLKB

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
73	NC	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND
78	V _{CCA}	V _{CCA}	V _{CCA}
79	GND	GND	GND
80	V _{CCR}	V _{CCR}	V _{CCR}
81	I/O	I/O	I/O
82	HCLK	HCLK	HCLK
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	NC	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	NC	I/O	I/O
89	I/O	I/O	I/O
90	I/O	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	NC	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	NC	I/O	I/O
98	V _{CCI}	V _{CCI}	V _{CCI}
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	I/O	I/O
107	I/O	I/O	I/O
108	NC	I/O	I/O

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	V _{CCA}	V _{CCA}	V _{CCA}
115	V _{CCI}	V _{CCI}	V _{CCI}
116	NC	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	NC	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	NC	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	NC	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	GND	GND	GND
130	V _{CCA}	V _{CCA}	V _{CCA}
131	GND	GND	GND
132	V _{CCR}	V _{CCR}	V _{CCR}
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	I/O	I/O	I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V _{CCI}	V _{CCI}	V _{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	V _{CCR}	V _{CCR}	V _{CCR}
20	V _{CCA}	V _{CCA}	V _{CCA}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V _{CCI}	V _{CCI}	V _{CCI}
30	V _{CCA}	V _{CCA}	V _{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V _{CCI}	V _{CCI}	V _{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V _{CCA}	V _{CCA}	V _{CCA}
57	GND	GND	GND
58	V _{CCR}	V _{CCR}	V _{CCR}
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V _{CCI}	V _{CCI}	V _{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V _{CCA}	V _{CCA}	V _{CCA}
80	V _{CCI}	V _{CCI}	V _{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V _{CCA}	V _{CCA}	V _{CCA}
90	V _{CCR}	V _{CCR}	V _{CCR}
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V _{CCI}	V _{CCI}	V _{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
109	GND	GND	GND
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V _{CCI}	V _{CCI}	V _{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	V _{CCR}	V _{CCR}	V _{CCR}
128	GND	GND	GND
129	V _{CCA}	V _{CCA}	V _{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

176-Pin TQFP

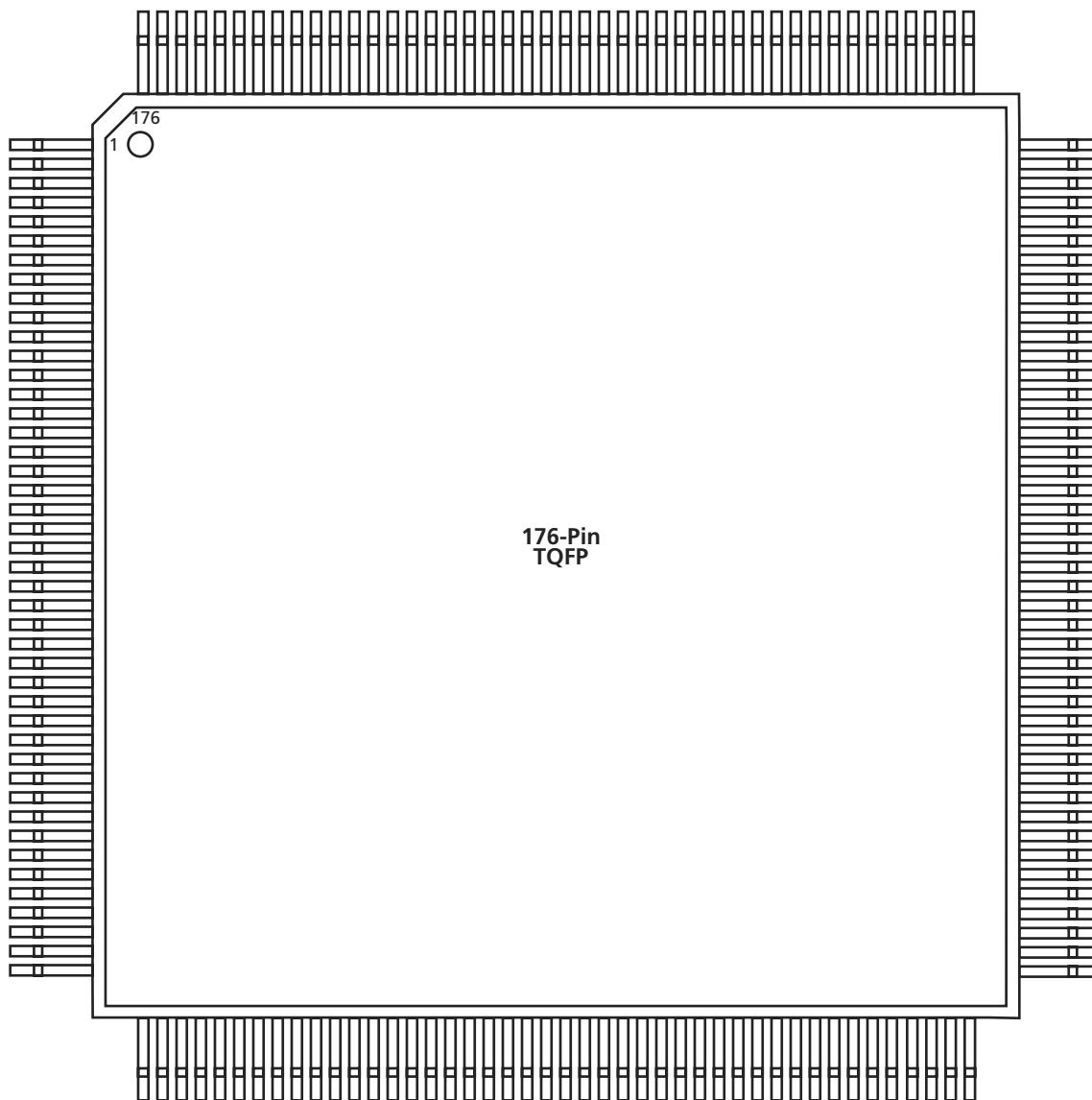


Figure 2-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V _{CCI}	V _{CCI}	V _{CCI}
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V _{CCA}	V _{CCA}	V _{CCA}
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V _{CCI}	V _{CCI}	V _{CCI}
33	V _{CCA}	V _{CCA}	V _{CCA}
34	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V _{CCI}	V _{CCI}	V _{CCI}
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V _{CCA}	V _{CCA}	V _{CCA}
67	V _{CCR}	V _{CCR}	V _{CCR}
68	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	I/O	I/O	I/O
146	I/O	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	CLKA	CLKA	CLKA
153	CLKB	CLKB	CLKB
154	V _{CCR}	V _{CCR}	V _{CCR}
155	GND	GND	GND
156	V _{CCA}	V _{CCA}	V _{CCA}

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
157	PRA, I/O	PRA, I/O	PRA, I/O
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	V _{CCI}	V _{CCI}	V _{CCI}
170	I/O	I/O	I/O
171	NC	I/O	I/O
172	NC	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	TCK, I/O	TCK, I/O	TCK, I/O

100-Pin VQFP		
Pin Number	A545X08 Function	A545X16, A545X16P Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	TMS	TMS
8	V _{CCI}	V _{CCI}
9	GND	GND
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	V _{CCI}	V _{CCI}
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	PRB, I/O	PRB, I/O

100-Pin VQFP		
Pin Number	A545X08 Function	A545X16, A545X16P Function
35	V _{CCA}	V _{CCA}
36	GND	GND
37	V _{CCR}	V _{CCR}
38	I/O	I/O
39	HCLK	HCLK
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	V _{CCI}	V _{CCI}
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	TDO, I/O	TDO, I/O
50	I/O	I/O
51	GND	GND
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	V _{CCA}	V _{CCA}
58	V _{CCI}	V _{CCI}
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	V _{CCA}	V _{CCA}
68	GND	GND

100-Pin VQFP		
Pin Number	A545X08 Function	A545X16, A545X16P Function
69	GND	GND
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	V _{CCI}	V _{CCI}
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	CLKA	CLKA
88	CLKB	CLKB
89	V _{CCR}	V _{CCR}
90	V _{CCA}	V _{CCA}
91	GND	GND
92	PRA, I/O	PRA, I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	TCK, I/O	TCK, I/O

313-Pin PBGA

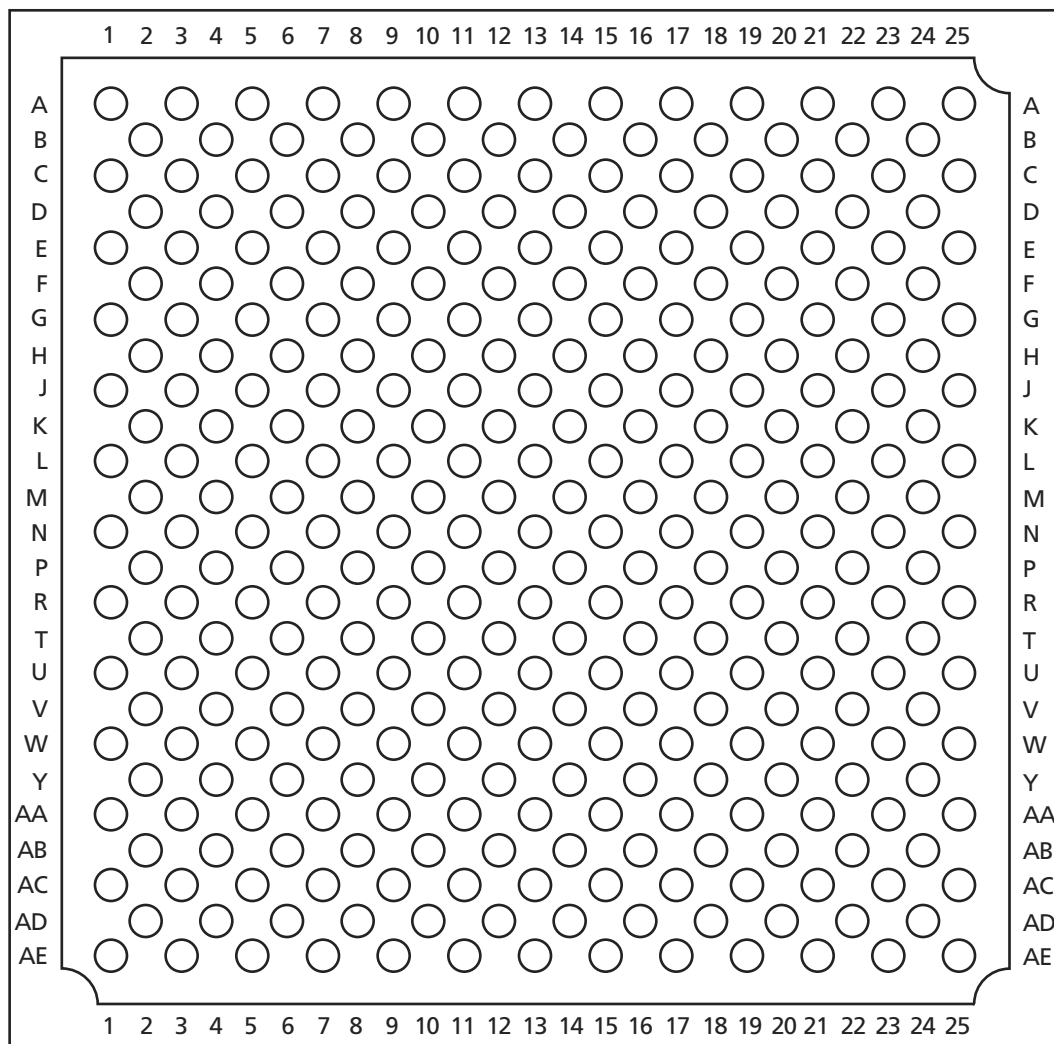


Figure 2-6 • 313-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function
D3	I/O	F22	I/O	K20	I/O	N11	GND
D4	TCK, I/O	F23	I/O	K21	I/O	N12	GND
D5	I/O	G1	I/O	K22	I/O	N13	GND
D6	I/O	G2	I/O	K23	I/O	N14	GND
D7	I/O	G3	I/O	L1	I/O	N20	NC
D8	I/O	G4	I/O	L2	I/O	N21	I/O
D9	I/O	G20	I/O	L3	I/O	N22	I/O
D10	I/O	G21	I/O	L4	V _{CCR}	N23	I/O
D11	V _{CCA}	G22	I/O	L10	GND	P1	I/O
D12	V _{CCR}	G23	GND	L11	GND	P2	I/O
D13	I/O	H1	I/O	L12	GND	P3	I/O
D14	I/O	H2	I/O	L13	GND	P4	I/O
D15	I/O	H3	I/O	L14	GND	P10	GND
D16	I/O	H4	I/O	L20	V _{CCR}	P11	GND
D17	I/O	H20	V _{CCA}	L21	I/O	P12	GND
D18	I/O	H21	I/O	L22	I/O	P13	GND
D19	I/O	H22	I/O	L23	NC	P14	GND
D20	I/O	H23	I/O	M1	I/O	P20	I/O
D21	I/O	J1	NC	M2	I/O	P21	I/O
D22	I/O	J2	I/O	M3	I/O	P22	I/O
D23	I/O	J3	I/O	M4	V _{CCA}	P23	I/O
E1	V _{CCI}	J4	I/O	M10	GND	R1	I/O
E2	I/O	J20	I/O	M11	GND	R2	I/O
E3	I/O	J21	I/O	M12	GND	R3	I/O
E4	I/O	J22	I/O	M13	GND	R4	I/O
E20	I/O	J23	I/O	M14	GND	R20	I/O
E21	I/O	K1	I/O	M20	V _{CCA}	R21	I/O
E22	I/O	K2	I/O	M21	I/O	R22	I/O
E23	I/O	K3	I/O	M22	I/O	R23	I/O
F1	I/O	K4	I/O	M23	V _{CCI}	T1	I/O
F2	TMS	K10	GND	N1	I/O	T2	I/O
F3	I/O	K11	GND	N2	I/O	T3	I/O
F4	I/O	K12	GND	N3	I/O	T4	I/O
F20	I/O	K13	GND	N4	I/O	T20	I/O
F21	I/O	K14	GND	N10	GND	T21	I/O

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v3.2)	Page
v3.1 (June 2003)	The "Ordering Information" was updated to include RoHS information.	1-ii
	The Product Plan was removed since all products have been released.	N/A
	Information concerning the TRST pin in the "Probe Circuit Control Pins" section was removed.	1-6
	The "Dedicated Test Mode" section is new.	1-6
	The "Programming" section is new.	1-7
	A note was added to the "Power-Up Sequencing" table.	1-15
	A note was added to the "Power-Down Sequencing" table. The 3.3 V comments were updated for the following devices: A545X08, A545X16, A545X32.	1-15
	U11 and U13 were added to the "313-Pin PBGA" table.	2-17
v3.0.1	Storage temperature in Table 1-3 was updated.	1-7
	Table 1-1 was updated.	1-5

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

The products described in this datasheet are subject to the International Traffic in Arms Regulations (ITAR) or the Export Administration Regulations (EAR). They may require an approved export license prior to their export. An export can include a release or disclosure to a foreign national inside or outside the United States.