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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	249
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	329-BBGA
Supplier Device Package	329-PBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-1bgg329

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Ordering Information



Plastic Device Resources

Device	PLCC 84-Pin	VQFP 100-Pin	PQFP 208-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 313-Pin	PBGA 329-Pin	FBGA 144-Pin
A54SX08	69	81	130	113	128	_	-	111
A54SX16	-	81	175	-	147	_	-	-
A54SX16P	-	81	175	113	147	_	-	-
A54SX32	-	_	174	113	147	249	249	-

Note: Package Definitions (Consult your local Actel sales representative for product availability):

PLCC = Plastic Leaded Chip Carrier

PQFP = Plastic Quad Flat Pack

TQFP = Thin Quad Flat Pack

VQFP = Very Thin Quad Flat Pack

PBGA = Plastic Ball Grid Array

FBGA = Fine Pitch (1.0 mm) Ball Grid Array



General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX's flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clockto-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

SX Family Architecture

The SX family architecture was designed to satisfy nextgeneration performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

Logic Module Design

The SX family architecture is described as a "sea-ofmodules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.



Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters



Figure 1-6 • **DirectConnect and FastConnect for Type 2 SuperClusters**





Figure 1-8 • Probe Setup

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II are compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability. The procedure for programming an SX device using Silicon Sculptor II are as follows:

- 1. Load the .AFM file
- 2. Select the device to be programmed
- 3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming SX devices, refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

3.3 V / 5 V Operating Conditions *Table 1-3* • Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
V _{CCR} ²	DC Supply Voltage ³	-0.3 to + 6.0	V
V _{CCA} ²	DC Supply Voltage	-0.3 to + 4.0	V
V _{CCI} ²	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	-0.3 to + 4.0	V
V _{CCI} ²	DC Supply Voltage (A54SX16P)	-0.3 to + 6.0	V
VI	Input Voltage	–0.5 to + 5.5	V
V _O	Output Voltage	-0.5 to + 3.6	V
I _{IO}	I/O Source Sink Current ³	-30 to + 5.0	mA
T _{STG}	Storage Temperature	-65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.

2. V_{CCR} in the A54SX16P must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.

3. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward-bias and can draw excessive current.



Figure 1-9 shows the 5.0 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.



Figure 1-9 • 5.0 V PCI Curve for A54SX16P Device

 $I_{OH} = 11.9 \times (V_{OUT} - 5.25) \times (V_{OUT} + 2.45)$ for V_{CC} > V_{OUT} > 3.1 V $I_{OL} = 78.5 \times V_{OUT} \times (4.4 - V_{OUT})$ for 0 V < V_{OUT} < 0.71 V

EQ 1-1

EQ 1-2

Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

- 1. Estimate the power consumption of the application.
- 2. Calculate the maximum power allowed for the device and package.
- 3. Compare the estimated power and maximum power values.

Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{Total} = P_{DC} + P_{AC}$$

EQ 1-5

р

х

у

r₁

fn

fp

f_{s1}

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12	٠	Standby	Power

I _{CC}	V _{cc}	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

 $P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} +$ $(I_{standbv}) \times V_{CCI} + xV_{OL} \times I_{OL} + y(V_{CCI} - V_{OH}) \times V_{OH}$

EQ 1-6

AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

EQ 1-7

 $P_{AC} = V_{CCA}^2 \times [(m \times C_{EOM} \times f_m)_{Module} +$ $(n \times C_{EOI} \times f_n)_{Input Buffer} + (p \times (C_{EOO} + C_L) \times f_p)_{Output Buffer} +$ $(0.5 \times (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} +$ $(0.5 \times (q2 \times CEQCR \times f_{q2}) + (r2 \times f_{q2}))RCLKB +$ $(0.5 \times (s_1 \times C_{EOHV} \times f_{s1}) + (C_{EOHF} \times f_{s1}))_{HCLK}]$

EQ 1-8

Definition of Terms Used in Formula

m	=	Number of logic modules switching at f _m
n	=	Number of input buffers switching at f

- = Number of input buffers switching at f_n
- Number of output buffers switching at fp =
- Number of clock loads on the first routed array q_1 clock
- Number of clock loads on the second routed array = q_2 clock
 - = Number of I/Os at logic low
 - Number of I/Os at logic high =
 - = Fixed capacitance due to first routed array clock
- Fixed capacitance due to second routed array = r₂ clock
- Number of clock loads on the dedicated array = S_1 clock

$$C_{EQM}$$
 = Equivalent capacitance of logic modules in pF

- Equivalent capacitance of input buffers in pF = C_{EQI}
- Equivalent capacitance of output buffers in pF CEOO =
- Equivalent capacitance of routed array clock in pF $C_{EOCR} =$
- Variable capacitance of dedicated array clock $C_{EOHV} =$
- Fixed capacitance of dedicated array clock $C_{EOHF} =$
- C = Output lead capacitance in pF
- Average logic module switching rate in MHz fm =
 - = Average input buffer switching rate in MHz
 - = Average output buffer switching rate in MHz
- = Average first routed array clock rate in MHz f_{q1}
- Average second routed array clock rate in MHz f_{q2} =
 - = Average dedicated array clock rate in MHz

Table 1-13 shows capacitance values for various devices.

	A54SX08	A54SX16	A54SX16P	A54SX32
C _{EQM} (pF)	4.0	4.0	4.0	4.0
C _{EQI} (pF)	3.4	3.4	3.4	3.4
C _{EQO} (pF)	4.7	4.7	4.7	4.7
C _{EQCR} (pF)	1.6	1.6	1.6	1.6
C _{EQHV}	0.615	0.615	0.615	0.615
C _{EQHF}	60	96	96	140
r ₁ (pF)) 87 138		138	171
r ₂ (pF)	87	138	138	171

 Table 1-13
 Capacitance Values for Devices

Table 1-14 • Power Consumption Guidelines

Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A54SX16P device. A pattern of 0101... was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101... caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

Description	Power Consumption Guideline
Logic Modules (m)	20% of modules
Inputs Switching (n)	# inputs/4
Outputs Switching (p)	# outputs/4
First Routed Array Clock Loads (q ₁)	20% of register cells
Second Routed Array Clock Loads (q ₂)	20% of register cells
Load Capacitance (C _L)	35 pF
Average Logic Module Switching Rate (f _m)	f/10
Average Input Switching Rate (f _n)	f/5
Average Output Switching Rate (f _p)	f/10
Average First Routed Array Clock Rate (f _{q1})	f/2
Average Second Routed Array Clock Rate (f _{q2})	f/2
Average Dedicated Array Clock Rate (f _{s1})	f
Dedicated Clock Array Clock Loads (s ₁)	20% of regular modules

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{Total} = P_{AC}$$
 (dynamic power) + P_{DC} (static power)

EQ 1-9

AC Power Dissipation

 $P_{AC} = P_{Module} + P_{RCLKA Net} + P_{RCLKB Net} + P_{HCLK Net} + P_{Output Buffer} + P_{Input Buffer}$

$$\begin{split} P_{AC} &= V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + \\ (n \times C_{EQI} \times f_n)_{Input Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output Buffer} + \\ (0.5 & (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + \\ (0.5 & (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2}))_{RCLKB} + \\ (0.5 & (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}] \end{split}$$

EQ 1-11

Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.



Figure 1-11 • Power Dissipation

Junction Temperature (T_J)

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

Junction Temperature =
$$\Delta T + T_a$$

Where:

 $T_a = Ambient Temperature$

 ΔT = Temperature gradient between junction (silicon) and ambient

 $\Delta T = \theta_{ja} \times P$

- P = Power calculated from Estimating Power Consumption section
- θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc} , and the junction to ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150 °C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

Maximum Power Allowed =
$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}} = \frac{150^{\circ}\text{C} - 70^{\circ}\text{C}}{28^{\circ}\text{C/W}} = 2.86 \text{ W}$$

EQ 1-13

EQ 1-14











Figure 1-15 • Input Buffer Delays

Figure 1-16 • C-Cell Delays

A54SX08 Timing Characteristics

Table 1-17 • A54SX08 Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 70°C)

		'-3' 9	Speed	'-2' 9	Speed	'-1' 9	Speed	'Std'	Speed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
C-Cell Propa	agation Delays ¹									
t _{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted R	outing Delays ²									
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t _{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t _{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t _{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t _{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t _{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t _{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timir	ng									
t _{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t _{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Modu	le Propagation Delays									
t _{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t _{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Input Modu	le Predicted Routing Delays ²									
t _{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t _{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t _{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t _{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t _{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t _{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn'}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD'}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A54SX16 Timing Characteristics

Table 1-18 • A54SX16 Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 70°C)

		'-3' 9	Speed	'-2' 9	Speed	'-1' S	Speed	'Std'	Speed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
C-Cell Propa	agation Delays ¹									
t _{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted R	outing Delays ²									
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t _{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t _{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t _{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t _{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t _{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t _{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timin	ig									
t _{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t _{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Modu	le Propagation Delays									
t _{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t _{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Ir	put Routing Delays ²									
t _{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t _{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t _{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t _{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t _{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t _{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn'}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD'}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

3. Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} , the loading is 5 pF.

A54SX32 Timing Characteristics

Table 1-20 • A54SX32 Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA} , V_{CCI} = 3.0 V, T_J = 70°C)

		'-3' 9	5peed	'-2' \$	Speed	'-1' \$	5peed	'Std'	Speed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
C-Cell Propa	ngation Delays ¹									
t _{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted R	outing Delays ²									
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t _{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t _{RD2}	FO = 2 Routing Delay		0.7		0.8		0.9		1.0	ns
t _{RD3}	FO = 3 Routing Delay		1.0		1.2		1.4		1.6	ns
t _{RD4}	FO = 4 Routing Delay		1.4		1.6		1.8		2.1	ns
t _{RD8}	FO = 8 Routing Delay		2.7		3.1		3.5		4.1	ns
t _{RD12}	FO = 12 Routing Delay		4.0		4.7		5.3		6.2	ns
R-Cell Timin	g									
t _{RCO}	Sequential Clock-to-Q		0.8		1.1		1.3		1.4	ns
t _{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Modu	le Propagation Delays									
t _{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t _{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted In	put Routing Delays ²									
t _{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t _{IRD2}	FO = 2 Routing Delay		0.7		0.8		0.9		1.0	ns
t _{IRD3}	FO = 3 Routing Delay		1.0		1.2		1.4		1.6	ns
t _{IRD4}	FO = 4 Routing Delay		1.4		1.6		1.8		2.1	ns
t _{IRD8}	FO = 8 Routing Delay		2.7		3.1		3.5		4.1	ns
t _{IRD12}	FO = 12 Routing Delay		4.0		4.7		5.3		6.2	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

3. Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} the loading is 5 pF.

Table 1-20 • A54SX32 Timing Characteristics (Continued)

(Worst-Case Commercial Conditions, V_{CCR}= 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 70°C)

		'-3' \$	Speed	'-2' \$	Speed	'-1' \$	Speed	'Std'	Speed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Network									
t _{HCKH}	Input LOW to HIGH (pad to R-Cell input)		1.9		2.1		2.4		2.8	ns
t _{HCKL}	Input HIGH to LOW (pad to R-Cell input)		1.9		2.1		2.4		2.8	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5	ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Arra	ay Clock Networks									
t _{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)		2.4		2.7		3.0		3.5	ns
t _{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell input)		2.4		2.7		3.1		3.6	ns
t _{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)		2.7		3.0		3.5		4.1	ns
t _{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)		2.7		3.1		3.6		4.2	ns
t _{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)		2.7		3.1		3.5		4.1	ns
t _{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)		2.8		3.2		3.6		4.3	ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (light load)		0.85		0.98		1.1		1.3	ns
t _{RCKSW}	Maximum Skew (50% load)		1.23		1.4		1.6		1.9	ns
t _{RCKSW}	Maximum Skew (100% load)		1.30		1.5		1.7		2.0	ns
TTL Output	Module Timing ³									
t _{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t _{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

3. Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} the loading is 5 pF.

Pin Description

CLKA/B Clock A and B

These pins are 3.3 V / 5.0 V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A545X72A, these clocks can be configured as bidirectional.)

GND Ground

LOW supply voltage.

HCLK Dedicated (hardwired) Array Clock

This pin is the 3.3 V / 5.0 V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3 V PCI or 5.0 V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A

The Probe A pin is used to output data from any userdefined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

PRB, I/O Probe B

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-2 on page 1-6). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See Table 1-1 on page 1-5.

V_{CCA} Supply Voltage

Supply voltage for Array. See Table 1-1 on page 1-5.

V_{CCR} Supply Voltage

Supply voltage for input tolerance (required for internal biasing). See Table 1-1 on page 1-5.



Package Pin Assignments

84-Pin PLCC



Figure 2-1 • 84-Pin PLCC (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

84-Pin PLCC					
Pin Number	A54SX08 Function				
1	V _{CCR}				
2	GND				
3	V _{CCA}				
4	PRA, I/O				
5	I/O				
6	I/O				
7	V _{CCI}				
8	I/O				
9	I/O				
10	I/O				
11	TCK, I/O				
12	TDI, I/O				
13	I/O				
14	I/O				
15	I/O				
16	TMS				
17	1/0 1/0 1/0				
18					
19					
20	I/O				
21	I/O				
22	I/O				
23	I/O				
24	I/O				
25	I/O				
26	I/O				
27	GND				
28	V _{CCI}				
29	I/O				
30	I/O				
31	I/O				
32	I/O				
33	I/O				
34	I/O				
35	I/O				

Pin Number	A54SX08 Function
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V _{CCA}
42	GND
43	V _{CCR}
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V _{CCA}
60	V _{CCI}
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V _{CCA}
69	GND
70	I/O

84-Pin PLCC					
Pin Number	A54SX08 Function				
71	I/O				
72	I/O				
73	I/O				
74	I/O				
75	I/O				
76	I/O				
77	I/O				
78	I/O				
79	I/O				
80	I/O				
81	I/O				
82	I/O				
83	CLKA				
84	CLKB				

144-Pin TQFP			144-Pin TQFP				
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function	Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
1	GND	GND	GND	37	I/O	I/O	I/O
2	TDI, I/O	TDI, I/O	TDI, I/O	38	I/O	I/O	I/O
3	I/O	I/O	I/O	39	I/O	I/O	I/O
4	I/O	I/O	I/O	40	I/O	I/O	I/O
5	I/O	I/O	I/O	41	I/O	I/O	I/O
6	I/O	I/O	I/O	42	I/O	I/O	I/O
7	I/O	I/O	I/O	43	I/O	I/O	I/O
8	I/O	I/O	I/O	44	V _{CCI}	V _{CCI}	V _{CCI}
9	TMS	TMS	TMS	45	I/O	I/O	I/O
10	V _{CCI}	V _{CCI}	V _{CCI}	46	I/O	I/O	I/O
11	GND	GND	GND	47	I/O	I/O	I/O
12	I/O	I/O	I/O	48	I/O	I/O	I/O
13	I/O	I/O	I/O	49	I/O	I/O	I/O
14	I/O	I/O	I/O	50	I/O	I/O	I/O
15	I/O	I/O	I/O	51	I/O	I/O	I/O
16	I/O	I/O	I/O	52	I/O	I/O	I/O
17	I/O	I/O	I/O	53	I/O	I/O	I/O
18	I/O	I/O	I/O	54	PRB, I/O	PRB, I/O	PRB, I/O
19	V _{CCR}	V _{CCR}	V _{CCR}	55	I/O	I/O	I/O
20	V _{CCA}	V _{CCA}	V _{CCA}	56	V _{CCA}	V _{CCA}	V _{CCA}
21	I/O	I/O	I/O	57	GND	GND	GND
22	I/O	I/O	I/O	58	V _{CCR}	V _{CCR}	V _{CCR}
23	I/O	I/O	I/O	59	I/O	I/O	I/O
24	I/O	I/O	I/O	60	HCLK	HCLK	HCLK
25	I/O	I/O	I/O	61	I/O	I/O	I/O
26	I/O	I/O	I/O	62	I/O	I/O	I/O
27	I/O	I/O	I/O	63	I/O	I/O	I/O
28	GND	GND	GND	64	I/O	I/O	I/O
29	V _{CCI}	V _{CCI}	V _{CCI}	65	I/O	I/O	I/O
30	V _{CCA}	V _{CCA}	V _{CCA}	66	I/O	I/O	I/O
31	I/O	I/O	I/O	67	I/O	I/O	I/O
32	I/O	I/O	I/O	68	V _{CCI}	V _{CCI}	V _{CCI}
33	I/O	I/O	I/O	69	I/O	I/O	I/O
34	I/O	I/O	I/O	70	I/O	I/O	I/O
35	I/O	I/O	I/O	71	TDO, I/O	TDO, I/O	TDO, I/O
36	GND	GND	GND	72	I/O	I/O	I/O

176-Pin TQFP



Figure 2-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

313-Pin PBGA		313-Pi	313-Pin PBGA		313-Pin PBGA		313-Pin PBGA	
Pin	A54SX32	Pin	A54SX32	Pin	A54SX32	Pin	A54SX32	
Number	Function	Number	Function	Number	Function	Number	Function	
H20	I/O	L25	I/O	R5	I/O	V10	I/O	
H22	V _{CCI}	M2	I/O	R7	I/O	V12	I/O	
H24	I/O	M4	I/O	R9	I/O	V14	I/O	
J1	I/O	M6	I/O	R11	I/O	V16	NC	
J3	I/O	M8	I/O	R13	GND	V18	I/O	
J5	I/O	M10	I/O	R15	I/O	V20	I/O	
J7	NC	M12	GND	R17	I/O	V22	V _{CCA}	
J9	I/O	M14	GND	R19	I/O	V24	V _{CCI}	
J11	I/O	M16	V _{CCI}	R21	I/O	W1	I/O	
J13	CLKA	M18	I/O	R23	I/O	W3	I/O	
J15	I/O	M20	I/O	R25	I/O	W5	I/O	
J17	I/O	M22	I/O	T2	I/O	W7	NC	
J19	I/O	M24	I/O	T4	I/O	W9	I/O	
J21	GND	N1	I/O	T6	I/O	W11	I/O	
J23	I/O	N3	V _{CCA}	T8	I/O	W13	V _{CCI}	
J25	I/O	N5	V _{CCR}	T10	ΙΟ	W15	I/O	
К2	I/O	N7	I/O	T12	ΙΟ	W17	I/O	
К4	I/O	N9	V _{CCI}	T14	HCLK	W19	I/O	
K6	I/O	N11	GND	T16	ΙΟ	W21	I/O	
K8	V _{CCI}	N13	GND	T18	ΙΟ	W23	I/O	
K10	I/O	N15	GND	T20	ΙΟ	W25	I/O	
K12	I/O	N17	ΙΟ	T22	ΙΟ	Y2	I/O	
K14	I/O	N19	ΙΟ	T24	ΙΟ	Y4	I/O	
K16	I/O	N21	ΙΟ	U1	I/O	Y6	I/O	
K18	I/O	N23	V _{CCR}	U3	I/O	Y8	I/O	
K20	V _{CCA}	N25	V _{CCA}	U5	V _{CCI}	Y10	I/O	
K22	I/O	P2	I/O	U7	I/O	Y12	I/O	
K24	I/O	P4	I/O	U9	I/O	Y14	I/O	
L1	I/O	P6	I/O	U11	ΙΟ	Y16	I/O	
L3	I/O	P8	I/O	U13	ΙΟ	Y18	I/O	
L5	I/O	P10	I/O	U15	ΙΟ	Y20	NC	
L7	1/0	P12	GND	U17	1/0	Y22	I/O	
L9	I/O	P14	GND	U19	ΙΟ	Y24	NC	
L11	I/O	P16	I/O	U21	ΙΟ			
L13	GND	P18	I/O	U23	I/O			
L15	I/O	P20	NC	U25	1/0			
L17	I/O	P22	I/O	V2	V _{CCA}			
L19	I/O	P24	I/O	V4	I/O			
L21	I/O	R1	I/O	V6	I/O			
L23	1/0	R3	I/O	V8	1/0			

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