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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	174
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	208-BFCQFP with Tie Bar
Supplier Device Package	208-CQFP (75x75)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-1cq208m">https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-1cq208m</a>

## Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

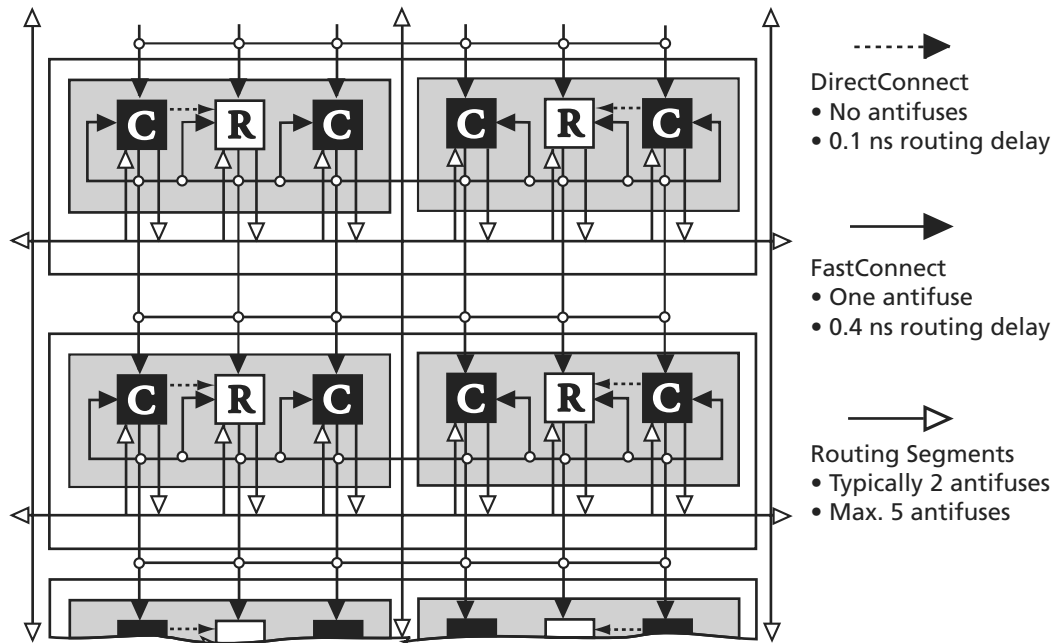


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

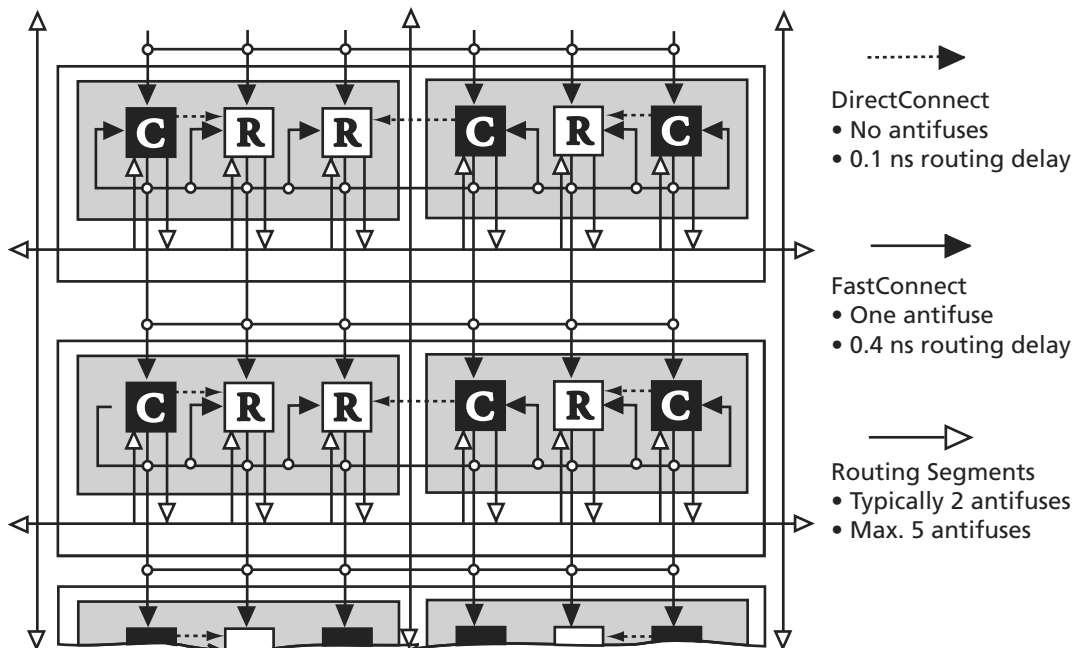


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

The Actel high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hardwired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

## Other Architectural Features

### Technology

The Actel SX family is implemented on a high-voltage twin-well CMOS process using 0.35  $\mu$  design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25  $\Omega$  with a capacitance of 1.0 fF for low signal impedance.

## Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

## I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin.

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

## Power Requirements

The SX family supports 3.3 V operation and is designed to tolerate 5.0 V inputs. (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest power architecture on the market.

Table 1-1 • Supply Voltages

Device	V <sub>CCA</sub>	V <sub>CCI</sub>	V <sub>CCR</sub>	Maximum Input Tolerance	Maximum Output Drive
A54SX08 A54SX16 A54SX32	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
A54SX16-P*	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V

**Note:** \*A54SX16-P has three different entries because it is capable of both a 3.3 V and a 5.0 V drive.

## PCI Compliance for the SX Family

The SX family supports 3.3 V and 5.0 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 1-6 • A54SX16P DC Specifications (5.0 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$V_{CCA}$	Supply Voltage for Array		3.0	3.6	V
$V_{CCR}$	Supply Voltage required for Internal Biasing		4.75	5.25	V
$V_{CCI}$	Supply Voltage for I/Os		4.75	5.25	V
$V_{IH}$	Input High Voltage <sup>1</sup>		2.0	$V_{CC} + 0.5$	V
$V_{IL}$	Input Low Voltage <sup>1</sup>		-0.5	0.8	V
$I_{IH}$	Input High Leakage Current	$V_{IN} = 2.7$		70	$\mu A$
$I_{IL}$	Input Low Leakage Current	$V_{IN} = 0.5$		-70	$\mu A$
$V_{OH}$	Output High Voltage	$I_{OUT} = -2 \text{ mA}$	2.4		V
$V_{OL}$	Output Low Voltage <sup>2</sup>	$I_{OUT} = 3 \text{ mA}, 6 \text{ mA}$		0.55	V
$C_{IN}$	Input Pin Capacitance <sup>3</sup>			10	pF
$C_{CLK}$	CLK Pin Capacitance		5	12	pF
$C_{IDSEL}$	IDSEL Pin Capacitance <sup>4</sup>			8	pF

### Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used, AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

## Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

## Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}}$$

EQ 1-5

## DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • Standby Power

I <sub>CC</sub>	V <sub>CC</sub>	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

$$P_{\text{DC}} = (I_{\text{standby}}) \times V_{\text{CCA}} + (I_{\text{standby}}) \times V_{\text{CCR}} + (I_{\text{standby}}) \times V_{\text{CCI}} + xV_{\text{OL}} \times I_{\text{OL}} + y(V_{\text{CCI}} - V_{\text{OH}}) \times V_{\text{OH}}$$

EQ 1-6

## AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-7

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 \times (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 \times (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 \times (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-8

## Definition of Terms Used in Formula

- m = Number of logic modules switching at  $f_m$
- n = Number of input buffers switching at  $f_n$
- p = Number of output buffers switching at  $f_p$
- $q_1$  = Number of clock loads on the first routed array clock
- $q_2$  = Number of clock loads on the second routed array clock
- x = Number of I/Os at logic low
- y = Number of I/Os at logic high
- $r_1$  = Fixed capacitance due to first routed array clock
- $r_2$  = Fixed capacitance due to second routed array clock
- $s_1$  = Number of clock loads on the dedicated array clock
- $C_{\text{EQM}}$  = Equivalent capacitance of logic modules in pF
- $C_{\text{EQI}}$  = Equivalent capacitance of input buffers in pF
- $C_{\text{EQO}}$  = Equivalent capacitance of output buffers in pF
- $C_{\text{EQCR}}$  = Equivalent capacitance of routed array clock in pF
- $C_{\text{EQHV}}$  = Variable capacitance of dedicated array clock
- $C_{\text{EQHF}}$  = Fixed capacitance of dedicated array clock
- $C_L$  = Output lead capacitance in pF
- $f_m$  = Average logic module switching rate in MHz
- $f_n$  = Average input buffer switching rate in MHz
- $f_p$  = Average output buffer switching rate in MHz
- $f_{q1}$  = Average first routed array clock rate in MHz
- $f_{q2}$  = Average second routed array clock rate in MHz
- $f_{s1}$  = Average dedicated array clock rate in MHz

Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.

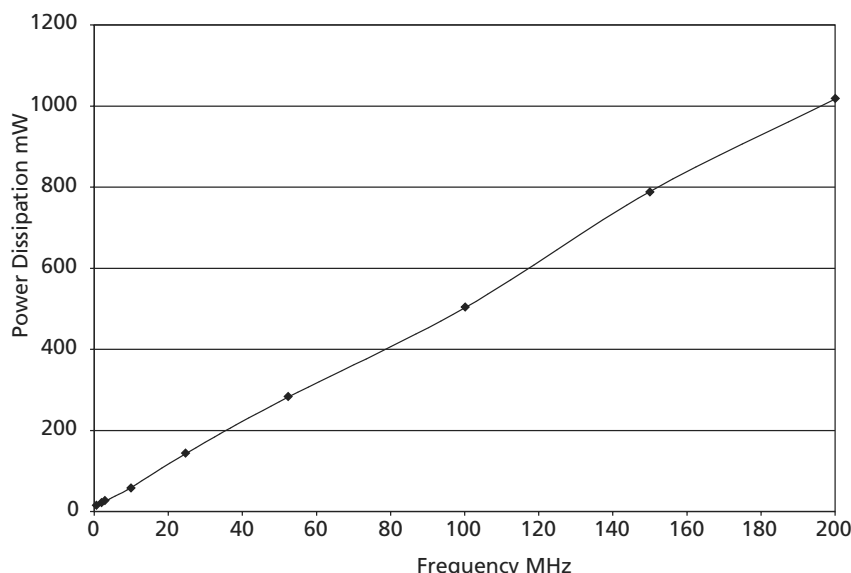


Figure 1-11 • Power Dissipation

## Junction Temperature ( $T_j$ )

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a$$

EQ 1-13

Where:

$T_a$  = Ambient Temperature

$\Delta T$  = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} \times P$$

$P$  = Power calculated from Estimating Power Consumption section

$\theta_{ja}$  = Junction to ambient of package.  $\theta_{ja}$  numbers are located in the "Package Thermal Characteristics" section.

## Package Thermal Characteristics

The device junction to case thermal characteristic is  $\theta_{jc}$ , and the junction to ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

The maximum junction temperature is 150 °C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ (°C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{28^\circ\text{C/W}} = 2.86 \text{ W}$$

EQ 1-14

Table 1-17 • A54SX08 Timing Characteristics (Continued)

(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t <sub>HCKH</sub>	Input LOW to HIGH (pad to R-Cell input)	1.0		1.1		1.3		1.5		ns
t <sub>HCKL</sub>	Input HIGH to LOW (pad to R-Cell input)	1.0		1.2		1.4		1.6		ns
t <sub>HPWH</sub>	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t <sub>HPWL</sub>	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t <sub>HCKSW</sub>	Maximum Skew	0.1		0.2		0.2		0.2		ns
t <sub>HP</sub>	Minimum Period	2.7		3.1		3.6		4.2		ns
f <sub>HMAX</sub>	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t <sub>RCKH</sub>	Input LOW to HIGH (light load) (pad to R-Cell input)	1.3		1.5		1.7		2.0		ns
t <sub>RCKL</sub>	Input HIGH to LOW (light load) (pad to R-Cell Input)	1.4		1.6		1.8		2.1		ns
t <sub>RCKH</sub>	Input LOW to HIGH (50% load) (pad to R-Cell input)	1.4		1.7		1.9		2.2		ns
t <sub>RCKL</sub>	Input HIGH to LOW (50% load) (pad to R-Cell input)	1.5		1.7		2.0		2.3		ns
t <sub>RCKH</sub>	Input LOW to HIGH (100% load) (pad to R-Cell input)	1.5		1.7		1.9		2.2		ns
t <sub>RCKL</sub>	Input HIGH to LOW (100% load) (pad to R-Cell input)	1.5		1.8		2.0		2.3		ns
t <sub>RPWH</sub>	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t <sub>RPWL</sub>	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t <sub>RCKSW</sub>	Maximum Skew (light load)	0.1		0.2		0.2		0.2		ns
t <sub>RCKSW</sub>	Maximum Skew (50% load)	0.3		0.3		0.4		0.4		ns
t <sub>RCKSW</sub>	Maximum Skew (100% load)	0.3		0.3		0.4		0.4		ns
TTL Output Module Timing <sup>1</sup>										
t <sub>DLH</sub>	Data-to-Pad LOW to HIGH	1.6		1.9		2.1		2.5		ns
t <sub>DHL</sub>	Data-to-Pad HIGH to LOW	1.6		1.9		2.1		2.5		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	2.1		2.4		2.8		3.2		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	2.3		2.7		3.1		3.6		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	1.4		1.7		1.9		2.2		ns

**Note:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics**  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>1</sup>										
t <sub>PD</sub>	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays <sup>2</sup>										
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t <sub>RCO</sub>	Sequential Clock-to-Q	0.8		1.1		1.2		1.4		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t <sub>INYH</sub>	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t <sub>INYL</sub>	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays <sup>2</sup>										
t <sub>IRD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>IRD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

### Notes:

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except  $t_{ENZL}$  and  $t_{ENZH}$ . For  $t_{ENZL}$  and  $t_{ENZH}$ , the loading is 5 pF.



**Table 1-18 • A54SX16 Timing Characteristics (Continued)**  
**(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t <sub>HCKH</sub>	Input LOW to HIGH (pad to R-Cell input)	1.2		1.4		1.5		1.8		ns
t <sub>HCKL</sub>	Input HIGH to LOW (pad to R-Cell input)	1.2		1.4		1.6		1.9		ns
t <sub>HPWH</sub>	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t <sub>HPWL</sub>	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t <sub>HCKSW</sub>	Maximum Skew	0.2		0.2		0.3		0.3		ns
t <sub>HP</sub>	Minimum Period	2.7		3.1		3.6		4.2		ns
f <sub>HMAX</sub>	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t <sub>RCKH</sub>	Input LOW to HIGH (light load) (pad to R-Cell input)	1.6		1.8		2.1		2.5		ns
t <sub>RCKL</sub>	Input HIGH to LOW (light load) (pad to R-Cell input)	1.8		2.0		2.3		2.7		ns
t <sub>RCKH</sub>	Input LOW to HIGH (50% load) (pad to R-Cell input)	1.8		2.1		2.5		2.8		ns
t <sub>RCKL</sub>	Input HIGH to LOW (50% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t <sub>RCKH</sub>	Input LOW to HIGH (100% load) (pad to R-Cell input)	1.8		2.1		2.4		2.8		ns
t <sub>RCKL</sub>	Input HIGH to LOW (100% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t <sub>RPWH</sub>	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t <sub>RPWL</sub>	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t <sub>RCKSW</sub>	Maximum Skew (light load)	0.5		0.5		0.5		0.7		ns
t <sub>RCKSW</sub>	Maximum Skew (50% load)	0.5		0.6		0.7		0.8		ns
t <sub>RCKSW</sub>	Maximum Skew (100% load)	0.5		0.6		0.7		0.8		ns
TTL Output Module Timing <sup>3</sup>										
t <sub>DLH</sub>	Data-to-Pad LOW to HIGH	1.6		1.9		2.1		2.5		ns
t <sub>DHL</sub>	Data-to-Pad HIGH to LOW	1.6		1.9		2.1		2.5		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	2.1		2.4		2.8		3.2		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	2.3		2.7		3.1		3.6		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	1.4		1.7		1.9		2.2		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	1.3		1.5		1.7		2.0		ns

**Notes:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except  $t_{ENZL}$  and  $t_{ENZH}$ . For  $t_{ENZL}$  and  $t_{ENZH}$ , the loading is 5 pF.

**Table 1-19 • A54SX16P Timing Characteristics (Continued)**  
**(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t <sub>HCKH</sub>	Input LOW to HIGH (pad to R-Cell input)	1.2		1.4		1.5		1.8		ns
t <sub>HCKL</sub>	Input HIGH to LOW (pad to R-Cell input)	1.2		1.4		1.6		1.9		ns
t <sub>HPWH</sub>	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t <sub>HPWL</sub>	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t <sub>HCKSW</sub>	Maximum Skew	0.2		0.2		0.3		0.3		ns
t <sub>HP</sub>	Minimum Period	2.7		3.1		3.6		4.2		ns
f <sub>HMAX</sub>	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t <sub>RCKH</sub>	Input LOW to HIGH (light load) (pad to R-Cell input)	1.6		1.8		2.1		2.5		ns
t <sub>RCKL</sub>	Input HIGH to LOW (Light Load) (pad to R-Cell input)	1.8		2.0		2.3		2.7		ns
t <sub>RCKH</sub>	Input LOW to HIGH (50% load) (pad to R-Cell input)	1.8		2.1		2.5		2.8		ns
t <sub>RCKL</sub>	Input HIGH to LOW (50% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t <sub>RCKH</sub>	Input LOW to HIGH (100% load) (pad to R-Cell input)	1.8		2.1		2.4		2.8		ns
t <sub>RCKL</sub>	Input HIGH to LOW (100% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t <sub>RPWH</sub>	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t <sub>RPWL</sub>	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t <sub>RCKSW</sub>	Maximum Skew (light load)	0.5		0.5		0.5		0.7		ns
t <sub>RCKSW</sub>	Maximum Skew (50% load)	0.5		0.6		0.7		0.8		ns
t <sub>RCKSW</sub>	Maximum Skew (100% load)	0.5		0.6		0.7		0.8		ns
TTL Output Module Timing										
t <sub>DLH</sub>	Data-to-Pad LOW to HIGH	2.4		2.8		3.1		3.7		ns
t <sub>DHL</sub>	Data-to-Pad HIGH to LOW	2.3		2.9		3.2		3.8		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	3.0		3.4		3.9		4.6		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	3.3		3.8		4.3		5.0		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	2.3		2.7		3.0		3.5		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	2.8		3.2		3.7		4.3		ns

**Note:**

1. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 10 pF loading.

Table 1-19 • A54SX16P Timing Characteristics (Continued)

(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL/PCI Output Module Timing										
t <sub>DLH</sub>	Data-to-Pad LOW to HIGH	1.5		1.7		2.0		2.3		ns
t <sub>DHL</sub>	Data-to-Pad HIGH to LOW	1.9		2.2		2.4		2.9		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	2.3		2.6		3.0		3.5		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	1.5		1.7		1.9		2.3		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	2.7		3.1		3.5		4.1		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	2.9		3.3		3.7		4.4		ns
PCI Output Module Timing <sup>3</sup>										
t <sub>DLH</sub>	Data-to-Pad LOW to HIGH	1.8		2.0		2.3		2.7		ns
t <sub>DHL</sub>	Data-to-Pad HIGH to LOW	1.7		2.0		2.2		2.6		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	0.8		1.0		1.1		1.3		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	1.2		1.2		1.5		1.8		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	1.0		1.1		1.3		1.5		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	1.1		1.3		1.5		1.7		ns
TTL Output Module Timing										
t <sub>DLH</sub>	Data-to-Pad LOW to HIGH	2.1		2.5		2.8		3.3		ns
t <sub>DHL</sub>	Data-to-Pad HIGH to LOW	2.0		2.3		2.6		3.1		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	2.5		2.9		3.2		3.8		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	3.0		3.5		3.9		4.6		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	2.3		2.7		3.1		3.6		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	2.9		3.3		3.7		4.4		ns

**Note:**

1. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 10 pF loading.

# 144-Pin TQFP

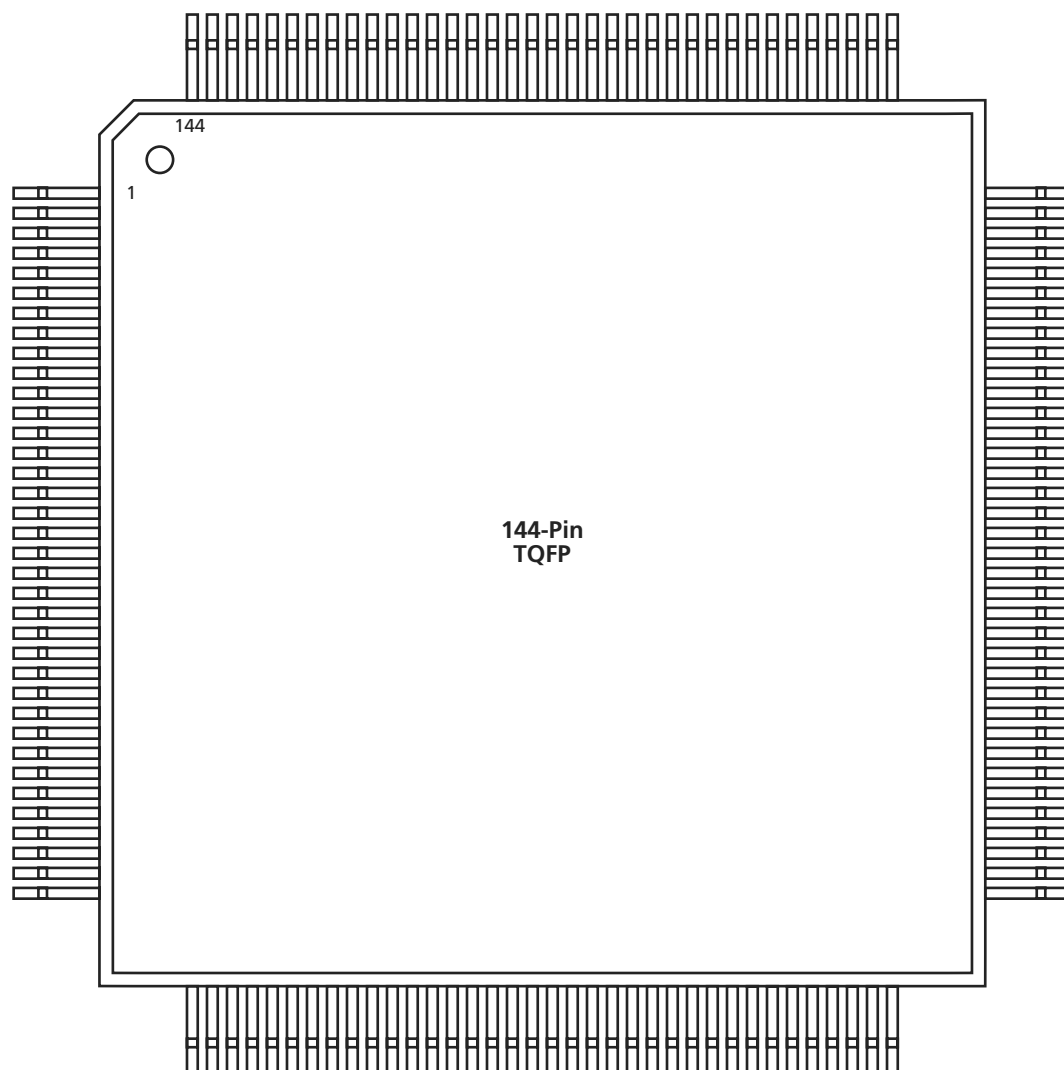


Figure 2-3 • 144-Pin TQFP (Top View)

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

## 176-Pin TQFP

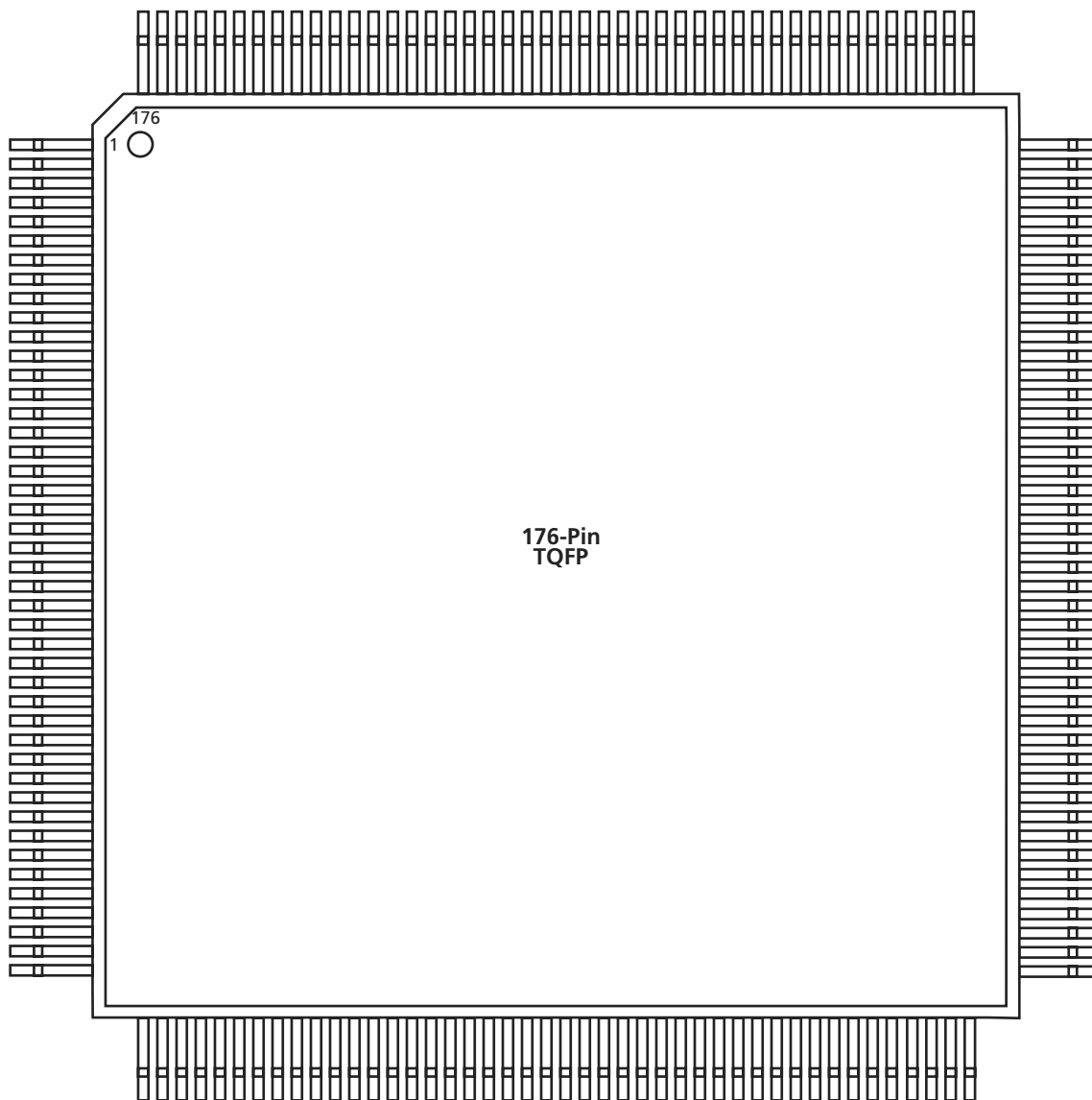


Figure 2-4 • 176-Pin TQFP (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

## 313-Pin PBGA

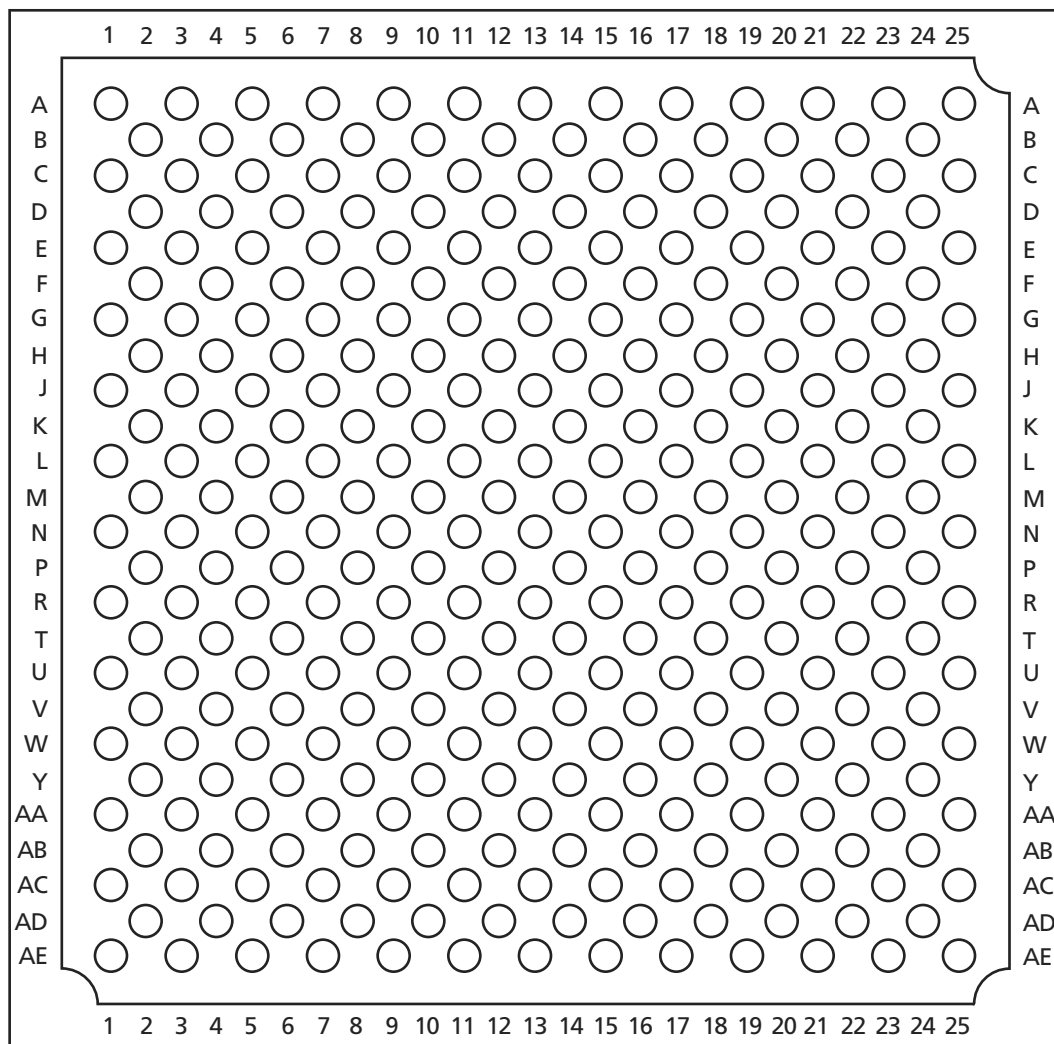


Figure 2-6 • 313-Pin PBGA (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

## 329-Pin PBGA

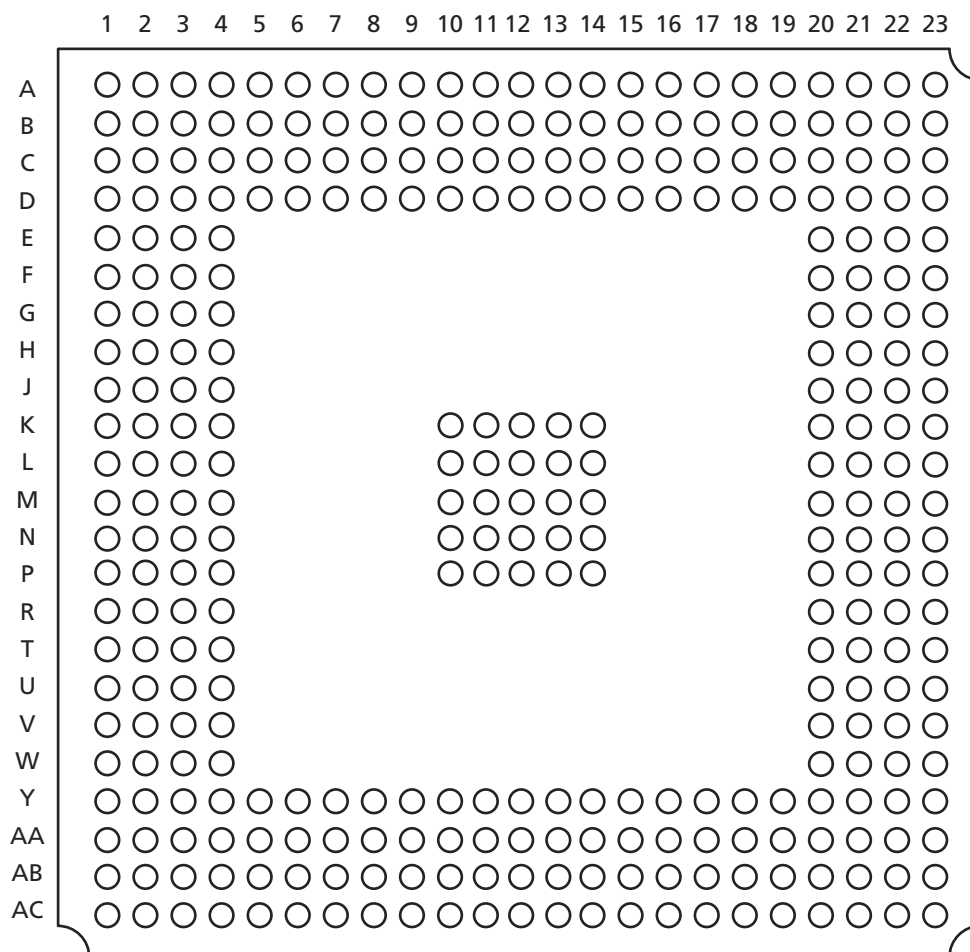


Figure 2-7 • 329-Pin PBGA (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
A1	GND	AA13	I/O	AC2	V <sub>CCI</sub>	B14	I/O
A2	GND	AA14	I/O	AC3	NC	B15	I/O
A3	V <sub>CCI</sub>	AA15	I/O	AC4	I/O	B16	I/O
A4	NC	AA16	I/O	AC5	I/O	B17	I/O
A5	I/O	AA17	I/O	AC6	I/O	B18	I/O
A6	I/O	AA18	I/O	AC7	I/O	B19	I/O
A7	V <sub>CCI</sub>	AA19	I/O	AC8	I/O	B20	I/O
A8	NC	AA20	TDO, I/O	AC9	V <sub>CCI</sub>	B21	I/O
A9	I/O	AA21	V <sub>CCI</sub>	AC10	I/O	B22	GND
A10	I/O	AA22	I/O	AC11	I/O	B23	V <sub>CCI</sub>
A11	I/O	AA23	V <sub>CCI</sub>	AC12	I/O	C1	NC
A12	I/O	AB1	I/O	AC13	I/O	C2	TDI, I/O
A13	CLKB	AB2	GND	AC14	I/O	C3	GND
A14	I/O	AB3	I/O	AC15	NC	C4	I/O
A15	I/O	AB4	I/O	AC16	I/O	C5	I/O
A16	I/O	AB5	I/O	AC17	I/O	C6	I/O
A17	I/O	AB6	I/O	AC18	I/O	C7	I/O
A18	I/O	AB7	I/O	AC19	I/O	C8	I/O
A19	I/O	AB8	I/O	AC20	I/O	C9	I/O
A20	I/O	AB9	I/O	AC21	NC	C10	I/O
A21	NC	AB10	I/O	AC22	V <sub>CCI</sub>	C11	I/O
A22	V <sub>CCI</sub>	AB11	PRB, I/O	AC23	GND	C12	I/O
A23	GND	AB12	I/O	B1	V <sub>CCI</sub>	C13	I/O
AA1	V <sub>CCI</sub>	AB13	HCLK	B2	GND	C14	I/O
AA2	I/O	AB14	I/O	B3	I/O	C15	I/O
AA3	GND	AB15	I/O	B4	I/O	C16	I/O
AA4	I/O	AB16	I/O	B5	I/O	C17	I/O
AA5	I/O	AB17	I/O	B6	I/O	C18	I/O
AA6	I/O	AB18	I/O	B7	I/O	C19	I/O
AA7	I/O	AB19	I/O	B8	I/O	C20	I/O
AA8	I/O	AB20	I/O	B9	I/O	C21	V <sub>CCI</sub>
AA9	I/O	AB21	I/O	B10	I/O	C22	GND
AA10	I/O	AB22	GND	B11	I/O	C23	NC
AA11	I/O	AB23	I/O	B12	PRA, I/O	D1	I/O
AA12	I/O	AC1	GND	B13	CLKA	D2	I/O



329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function
D3	I/O	F22	I/O	K20	I/O	N11	GND
D4	TCK, I/O	F23	I/O	K21	I/O	N12	GND
D5	I/O	G1	I/O	K22	I/O	N13	GND
D6	I/O	G2	I/O	K23	I/O	N14	GND
D7	I/O	G3	I/O	L1	I/O	N20	NC
D8	I/O	G4	I/O	L2	I/O	N21	I/O
D9	I/O	G20	I/O	L3	I/O	N22	I/O
D10	I/O	G21	I/O	L4	V <sub>CCR</sub>	N23	I/O
D11	V <sub>CCA</sub>	G22	I/O	L10	GND	P1	I/O
D12	V <sub>CCR</sub>	G23	GND	L11	GND	P2	I/O
D13	I/O	H1	I/O	L12	GND	P3	I/O
D14	I/O	H2	I/O	L13	GND	P4	I/O
D15	I/O	H3	I/O	L14	GND	P10	GND
D16	I/O	H4	I/O	L20	V <sub>CCR</sub>	P11	GND
D17	I/O	H20	V <sub>CCA</sub>	L21	I/O	P12	GND
D18	I/O	H21	I/O	L22	I/O	P13	GND
D19	I/O	H22	I/O	L23	NC	P14	GND
D20	I/O	H23	I/O	M1	I/O	P20	I/O
D21	I/O	J1	NC	M2	I/O	P21	I/O
D22	I/O	J2	I/O	M3	I/O	P22	I/O
D23	I/O	J3	I/O	M4	V <sub>CCA</sub>	P23	I/O
E1	V <sub>CCI</sub>	J4	I/O	M10	GND	R1	I/O
E2	I/O	J20	I/O	M11	GND	R2	I/O
E3	I/O	J21	I/O	M12	GND	R3	I/O
E4	I/O	J22	I/O	M13	GND	R4	I/O
E20	I/O	J23	I/O	M14	GND	R20	I/O
E21	I/O	K1	I/O	M20	V <sub>CCA</sub>	R21	I/O
E22	I/O	K2	I/O	M21	I/O	R22	I/O
E23	I/O	K3	I/O	M22	I/O	R23	I/O
F1	I/O	K4	I/O	M23	V <sub>CCI</sub>	T1	I/O
F2	TMS	K10	GND	N1	I/O	T2	I/O
F3	I/O	K11	GND	N2	I/O	T3	I/O
F4	I/O	K12	GND	N3	I/O	T4	I/O
F20	I/O	K13	GND	N4	I/O	T20	I/O
F21	I/O	K14	GND	N10	GND	T21	I/O

329-Pin PBGA	
Pin Number	A54SX32 Function
T22	I/O
T23	I/O
U1	I/O
U2	I/O
U3	V <sub>CCA</sub>
U4	I/O
U20	I/O
U21	V <sub>CCA</sub>
U22	I/O
U23	I/O
V1	V <sub>CCI</sub>
V2	I/O
V3	I/O

329-Pin PBGA	
Pin Number	A54SX32 Function
V4	I/O
V20	I/O
V21	I/O
V22	I/O
V23	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W20	I/O
W21	I/O
W22	I/O

329-Pin PBGA	
Pin Number	A54SX32 Function
W23	NC
Y1	NC
Y2	I/O
Y3	I/O
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O

329-Pin PBGA	
Pin Number	A54SX32 Function
Y12	V <sub>CCA</sub>
Y13	V <sub>CCR</sub>
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O

# 144-Pin FBGA

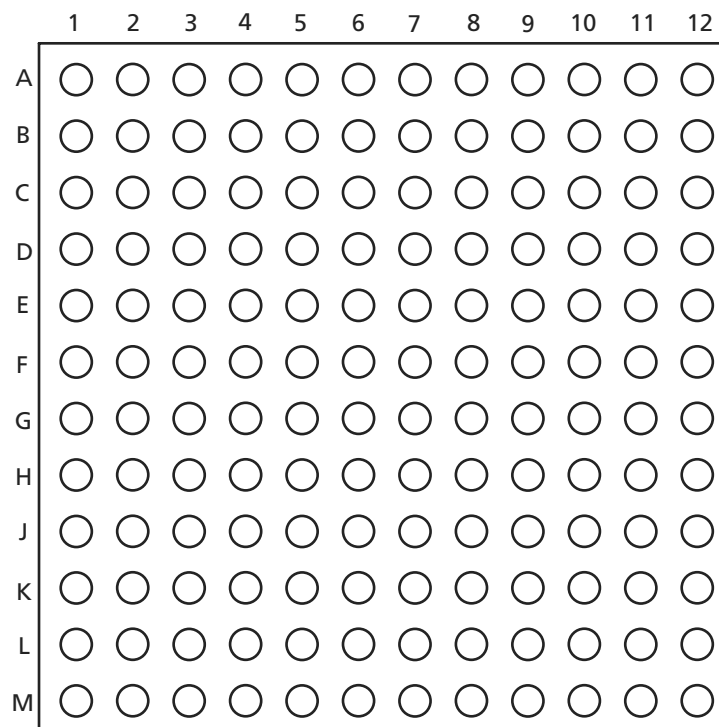


Figure 2-8 • 144-Pin FBGA (Top View)

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	A54SX08 Function	Pin Number	A54SX08 Function	Pin Number	A54SX08 Function	Pin Number	A54SX08 Function
A1	I/O	D1	I/O	G1	I/O	K1	I/O
A2	I/O	D2	V <sub>CCI</sub>	G2	GND	K2	I/O
A3	I/O	D3	TDI, I/O	G3	I/O	K3	I/O
A4	I/O	D4	I/O	G4	I/O	K4	I/O
A5	V <sub>CCA</sub>	D5	I/O	G5	GND	K5	I/O
A6	GND	D6	I/O	G6	GND	K6	I/O
A7	CLKA	D7	I/O	G7	GND	K7	GND
A8	I/O	D8	I/O	G8	V <sub>CCI</sub>	K8	I/O
A9	I/O	D9	I/O	G9	I/O	K9	I/O
A10	I/O	D10	I/O	G10	I/O	K10	GND
A11	I/O	D11	I/O	G11	I/O	K11	I/O
A12	I/O	D12	I/O	G12	I/O	K12	I/O
B1	I/O	E1	I/O	H1	I/O	L1	GND
B2	GND	E2	I/O	H2	I/O	L2	I/O
B3	I/O	E3	I/O	H3	I/O	L3	I/O
B4	I/O	E4	I/O	H4	I/O	L4	I/O
B5	I/O	E5	TMS	H5	V <sub>CCA</sub>	L5	I/O
B6	I/O	E6	V <sub>CCI</sub>	H6	V <sub>CCA</sub>	L6	I/O
B7	CLKB	E7	V <sub>CCI</sub>	H7	V <sub>CCI</sub>	L7	HCLK
B8	I/O	E8	V <sub>CCI</sub>	H8	V <sub>CCI</sub>	L8	I/O
B9	I/O	E9	V <sub>CCA</sub>	H9	V <sub>CCA</sub>	L9	I/O
B10	I/O	E10	I/O	H10	I/O	L10	I/O
B11	GND	E11	GND	H11	I/O	L11	I/O
B12	I/O	E12	I/O	H12	V <sub>CCR</sub>	L12	I/O
C1	I/O	F1	I/O	J1	I/O	M1	I/O
C2	I/O	F2	I/O	J2	I/O	M2	I/O
C3	TCK, I/O	F3	V <sub>CCR</sub>	J3	I/O	M3	I/O
C4	I/O	F4	I/O	J4	I/O	M4	I/O
C5	I/O	F5	GND	J5	I/O	M5	I/O
C6	PRA, I/O	F6	GND	J6	PRB, I/O	M6	I/O
C7	I/O	F7	GND	J7	I/O	M7	V <sub>CCA</sub>
C8	I/O	F8	V <sub>CCI</sub>	J8	I/O	M8	I/O
C9	I/O	F9	I/O	J9	I/O	M9	I/O
C10	I/O	F10	GND	J10	I/O	M10	I/O
C11	I/O	F11	I/O	J11	I/O	M11	TDO, I/O
C12	I/O	F12	I/O	J12	V <sub>CCA</sub>	M12	I/O

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