**Welcome to E-XFL.COM**

**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.
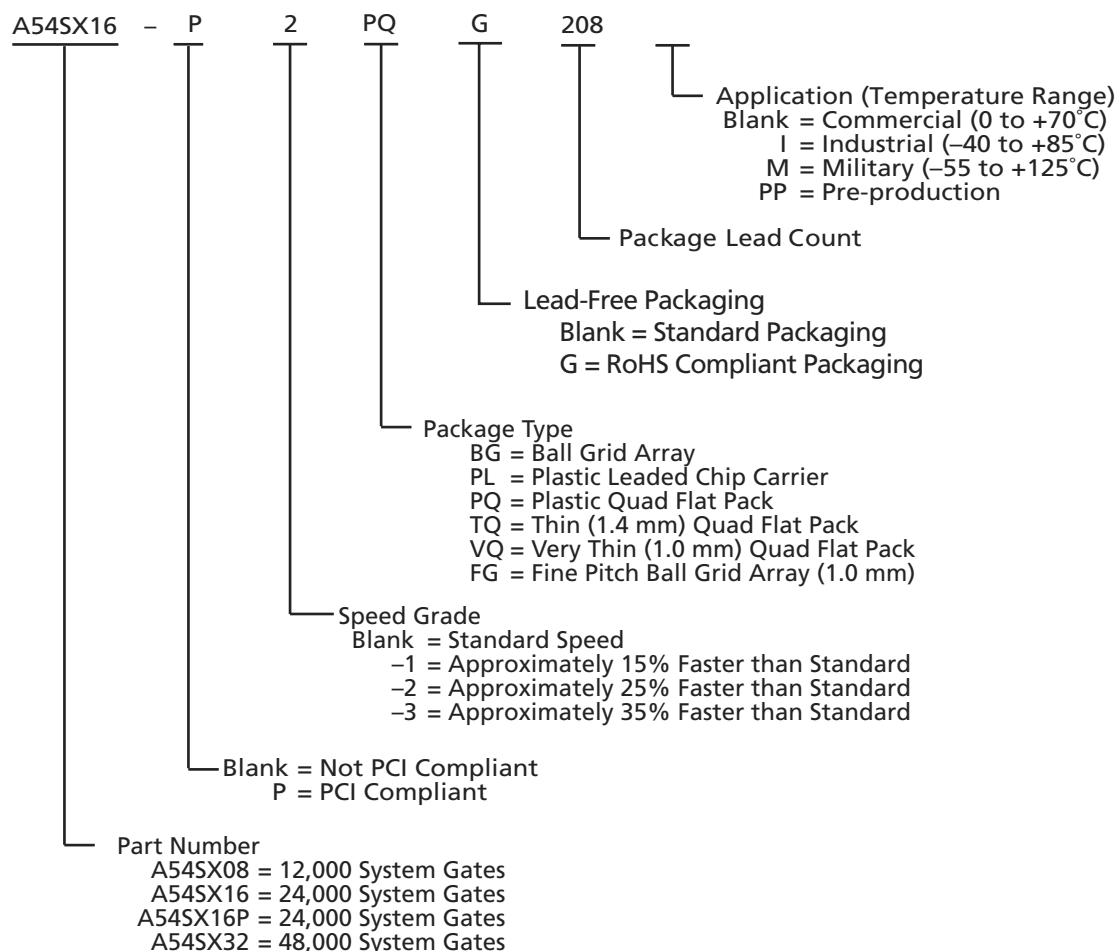
**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2880 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 174 |
| Number of Gates | 48000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -55°C ~ 125°C (TC) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-1pq208m |

# Ordering Information

```
A54SX16  –  P  2  PQ  G  208
```

Application (Temperature Range)
Blank = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
PP = Pre-production

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
BG = Ball Grid Array
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flat Pack
TQ = Thin (1.4 mm) Quad Flat Pack
VQ = Very Thin (1.0 mm) Quad Flat Pack
FG = Fine Pitch Ball Grid Array (1.0 mm)

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% Faster than Standard
–2 = Approximately 25% Faster than Standard
–3 = Approximately 35% Faster than Standard

Blank = Not PCI Compliant
P = PCI Compliant

Part Number
A54SX08 = 12,000 System Gates
A54SX16 = 24,000 System Gates
A54SX16P = 24,000 System Gates
A54SX32 = 48,000 System Gates

# Plastic Device Resources

| Device | User I/Os (including clock buffers) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | PLCC 84-Pin | VQFP 100-Pin | PQFP 208-Pin | TQFP 144-Pin | TQFP 176-Pin | PBGA 313-Pin | PBGA 329-Pin | FBGA 144-Pin |
| A54SX08 | 69 | 81 | 130 | 113 | 128 | – | – | 111 |
| A54SX16 | – | 81 | 175 | – | 147 | – | – | – |
| A54SX16P | – | 81 | 175 | 113 | 147 | – | – | – |
| A54SX32 | – | – | 174 | 113 | 147 | 249 | 249 | – |

**Note:** *Package Definitions (Consult your local Actel sales representative for product availability):*
*PLCC = Plastic Leaded Chip Carrier*
*PQFP = Plastic Quad Flat Pack*
*TQFP = Thin Quad Flat Pack*
*VQFP = Very Thin Quad Flat Pack*
*PBGA = Plastic Ball Grid Array*
*FBGA = Fine Pitch (1.0 mm) Ball Grid Array*

# SX Family FPGAs

## General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX's flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

## SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

### Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

### Logic Module Design

The SX family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.
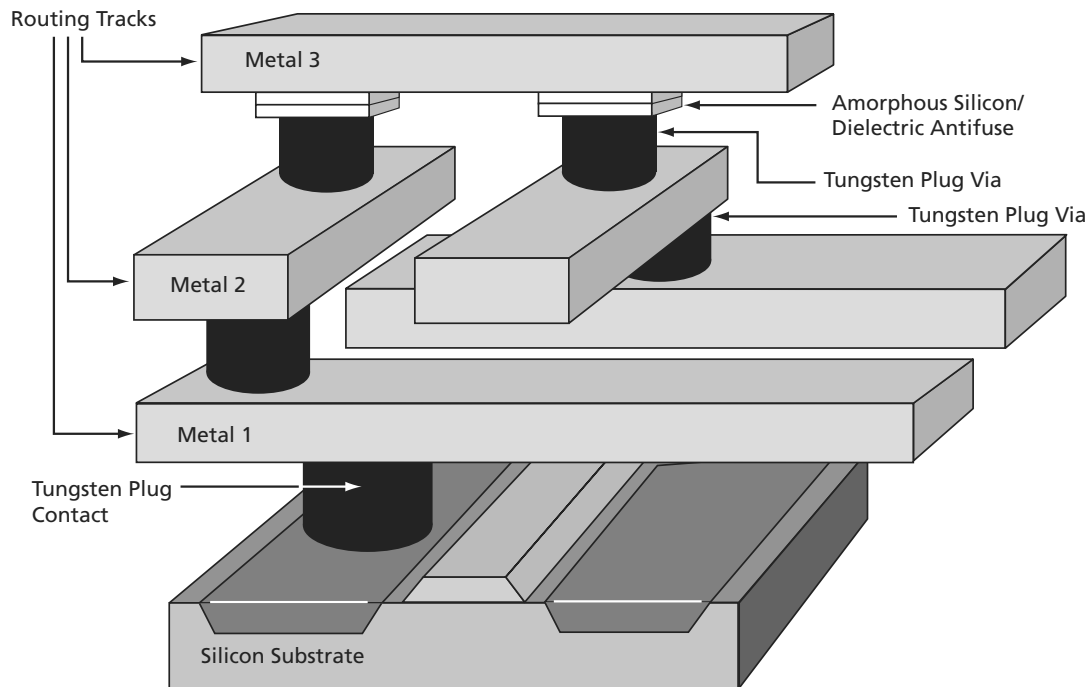


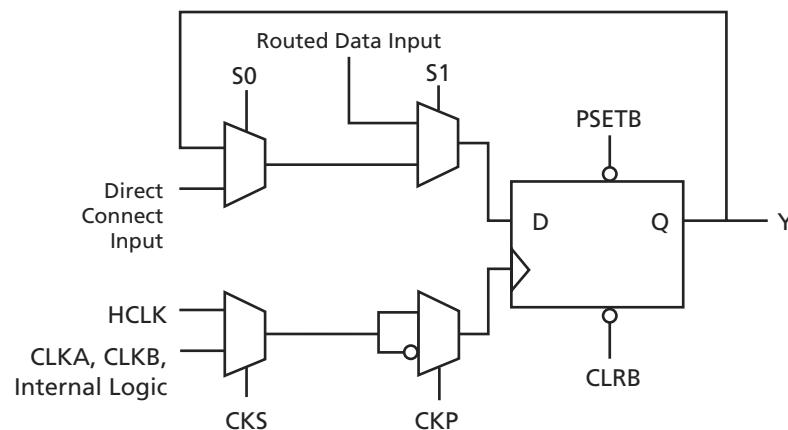*Figure 1-1* • **SX Family Interconnect Elements**



*Figure 1-2* • **R-Cell**

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

## Boundary Scan Testing (BST)

All SX devices are IEEE 1149.1 compliant. SX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 1-2. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10 kΩ. TMS can be pulled LOW to initiate the test sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

*Table 1-2* • **Boundary Scan Pin Functionality**

| Program Fuse Blown (Dedicated Test Mode) | Program Fuse Not Blown (Flexible Mode) |
|---|---|
| TCK, TDI, TDO are dedicated BST pins. | TCK, TDI, TDO are flexible and may be used as I/Os. |
| No need for pull-up resistor for TMS | Use a pull-up resistor of 10 kΩ on TMS. |

## Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software by checking the "Reserve JTAG" box in "Device Selection Wizard" (Figure 1-7). JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the Table 1-5 on page 1-8 for detailed specifications.

*Figure 1-7* • **Device Selection Wizard**

## Development Tool Support

The SX family of FPGAs is fully supported by both the Actel Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the Libero IDE flow diagram (located on the Actel website) for more information.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators, and the simulation results can be cross-probed with Silicon Explorer II, Actel integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Actel Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys®, and Cadence® Design Systems. The Designer software is available for both the Windows® and UNIX® operating systems.

## Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-8 on page 1-7 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

## Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuitry.

*Table 1-4 •* **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature Range* | 0 to + 70 | −40 to + 85 | −55 to +125 | °C |
| 3.3 V Power Supply Tolerance | ±10 | ±10 | ±10 | %$V_{CC}$ |
| 5.0 V Power Supply Tolerance | ±5 | ±10 | ±10 | %$V_{CC}$ |

**Note:** *Ambient temperature ($T_A$) is used for commercial and industrial; case temperature ($T_C$) is used for military.*

*Table 1-5 •* **Electrical Specifications**

| Symbol | Parameter | Commercial | | Industrial | | Units |
|---|---|---|---|---|---|---|
| | | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $V_{OH}$ | ($I_{OH}$ = −20 µA) (CMOS) | ($V_{CCI}$ − 0.1) | $V_{CCI}$ | ($V_{CCI}$ − 0.1) | $V_{CCI}$ | V |
| | ($I_{OH}$ = −8 mA) (TTL) | 2.4 | $V_{CCI}$ | | | |
| | ($I_{OH}$ = −6 mA) (TTL) | | | 2.4 | $V_{CCI}$ | |
| $V_{OL}$ | ($I_{OL}$ = 20 µA) (CMOS) | | 0.10 | | | V |
| | ($I_{OL}$ = 12 mA) (TTL) | | 0.50 | | | |
| | ($I_{OL}$ = 8 mA) (TTL) | | | | 0.50 | |
| $V_{IL}$ | | | 0.8 | | 0.8 | V |
| $V_{IH}$ | | 2.0 | | 2.0 | | V |
| $t_R$, $t_F$ | Input Transition Time $t_R$, $t_F$ | | 50 | | 50 | ns |
| $C_{IO}$ | $C_{IO}$ I/O Capacitance | | 10 | | 10 | pF |
| $I_{CC}$ | Standby Current, $I_{CC}$ | | 4.0 | | 4.0 | mA |
| $I_{CC(D)}$ | $I_{CC(D)}$ $I_{Dynamic}$ $V_{CC}$ Supply Current | See "Evaluating Power in SX Devices" on page 1-16. | | | | |

# A54SX16P AC Specifications for (PCI Operation)

*Table 1-7 •* **A54SX16P AC Specifications for (PCI Operation)**

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 1.4$[1] | –44 | | mA |
| | | $1.4 \leq V_{OUT} < 2.4$[1, 2] | $-44 + (V_{OUT} - 1.4)/0.024$ | | mA |
| | | $3.1 < V_{OUT} < V_{CC}$[1, 3] | | EQ 1-1 on page 1-11 | |
| | (Test Point) | $V_{OUT} = 3.1$[3] | | –142 | mA |
| $I_{OL(AC)}$ | Switching Current High | $V_{OUT} \geq 2.2$[1] | 95 | | mA |
| | | $2.2 > V_{OUT} > 0.55$[1] | $V_{OUT}/0.023$ | | |
| | | $0.71 > V_{OUT} > 0$[1, 3] | | EQ 1-2 on page 1-11 | mA |
| | (Test Point) | $V_{OUT} = 0.71$[3] | | 206 | mA |
| $I_{CL}$ | Low Clamp Current | $-5 < V_{IN} \leq -1$ | $-25 + (V_{IN} + 1)/0.015$ | | mA |
| $slew_R$ | Output Rise Slew Rate | 0.4 V to 2.4 V load[4] | 1 | 5 | V/ns |
| $slew_F$ | Output Fall Slew Rate | 2.4 V to 0.4 V load[4] | 1 | 5 | V/ns |

***Notes:***

1. *Refer to the V/I curves in Figure 1-9 on page 1-11. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half-size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*

2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*

3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 1-9 on page 1-11. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*

4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*
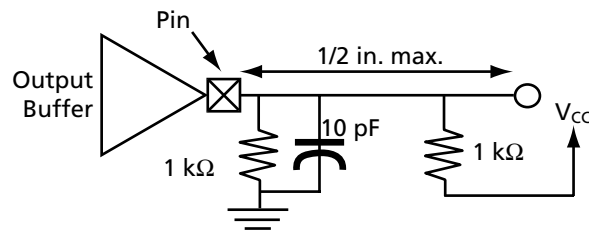
# A54SX16P AC Specifications (3.3 V PCI Operation)

*Table 1-9 •* **A54SX16P AC Specifications (3.3 V PCI Operation)**

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 0.3V_{CC}$[1] | | | mA |
| | | $0.3V_{CC} \leq V_{OUT} < 0.9V_{CC}$[1] | $-12V_{CC}$ | | mA |
| | | $0.7V_{CC} < V_{OUT} < V_{CC}$[1,2] | $-17.1 + (V_{CC} - V_{OUT})$ | EQ 1-3 on page 1-14 | |
| | (Test Point) | $V_{OUT} = 0.7V_{CC}$[2] | | $-32V_{CC}$ | mA |
| $I_{OL(AC)}$ | Switching Current High | $V_{CC} > V_{OUT} \geq 0.6V_{CC}$[1] | | | mA |
| | | $0.6V_{CC} > V_{OUT} > 0.1V_{CC}$[1] | $16V_{CC}$ | | mA |
| | | $0.18V_{CC} > V_{OUT} > 0$[1,2] | $26.7V_{OUT}$ | EQ 1-4 on page 1-14 | mA |
| | (Test Point) | $V_{OUT} = 0.18V_{CC}$[2] | | $38V_{CC}$ | |
| $I_{CL}$ | Low Clamp Current | $-3 < V_{IN} \leq -1$ | $-25 + (V_{IN} + 1)/0.015$ | | mA |
| $I_{CH}$ | High Clamp Current | $-3 < V_{IN} \leq -1$ | $25 + (V_{IN} - V_{OUT} - 1)/0.015$ | | mA |
| $slew_R$ | Output Rise Slew Rate[3] | $0.2V_{CC}$ to $0.6V_{CC}$ load | 1 | 4 | V/ns |
| $slew_F$ | Output Fall Slew Rate[3] | $0.6V_{CC}$ to $0.2V_{CC}$ load | 1 | 4 | V/ns |

***Notes:***

1. *Refer to the V/I curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*

2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*

3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*
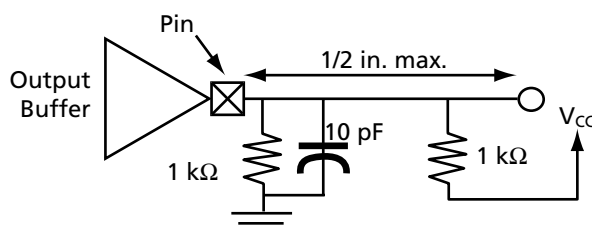
# Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

## Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{Total} = P_{DC} + P_{AC}$$

*EQ 1-5*

## DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

*Table 1-12 • **Standby Power***

| $I_{CC}$ | $V_{CC}$ | Power |
|----------|----------|---------|
| 4 mA | 3.6 V | 14.4 mW |

The DC power dissipation is defined in EQ 1-6.

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + xV_{OL} \times I_{OL} + y(V_{CCI} - V_{OH}) \times V_{OH}$$

*EQ 1-6*

## AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

*EQ 1-7*

$$P_{AC} = V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + (n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + (0.5 \times (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + (0.5 \times (q2 \times CEQCR \times f_{q2}) + (r2 \times f_{q2}))RCLKB + (0.5 \times (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]$$

*EQ 1-8*

**Definition of Terms Used in Formula**

| | | |
|---|---|---|
| m | = | Number of logic modules switching at $f_m$ |
| n | = | Number of input buffers switching at $f_n$ |
| p | = | Number of output buffers switching at $f_p$ |
| $q_1$ | = | Number of clock loads on the first routed array clock |
| $q_2$ | = | Number of clock loads on the second routed array clock |
| x | = | Number of I/Os at logic low |
| y | = | Number of I/Os at logic high |
| $r_1$ | = | Fixed capacitance due to first routed array clock |
| $r_2$ | = | Fixed capacitance due to second routed array clock |
| $s_1$ | = | Number of clock loads on the dedicated array clock |
| $C_{EQM}$ | = | Equivalent capacitance of logic modules in pF |
| $C_{EQI}$ | = | Equivalent capacitance of input buffers in pF |
| $C_{EQO}$ | = | Equivalent capacitance of output buffers in pF |
| $C_{EQCR}$ | = | Equivalent capacitance of routed array clock in pF |
| $C_{EQHV}$ | = | Variable capacitance of dedicated array clock |
| $C_{EQHF}$ | = | Fixed capacitance of dedicated array clock |
| $C_L$ | = | Output lead capacitance in pF |
| $f_m$ | = | Average logic module switching rate in MHz |
| $f_n$ | = | Average input buffer switching rate in MHz |
| $f_p$ | = | Average output buffer switching rate in MHz |
| $f_{q1}$ | = | Average first routed array clock rate in MHz |
| $f_{q2}$ | = | Average second routed array clock rate in MHz |
| $f_{s1}$ | = | Average dedicated array clock rate in MHz |

*Table 1-15 •* **Package Thermal Characteristics**

| Package Type | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ Still Air | $\theta_{ja}$ 300 ft/min. | Units |
|---|---|---|---|---|---|
| Plastic Leaded Chip Carrier (PLCC) | 84 | 12 | 32 | 22 | °C/W |
| Thin Quad Flat Pack (TQFP) | 144 | 11 | 32 | 24 | °C/W |
| Thin Quad Flat Pack (TQFP) | 176 | 11 | 28 | 21 | °C/W |
| Very Thin Quad Flatpack (VQFP) | 100 | 10 | 38 | 32 | °C/W |
| Plastic Quad Flat Pack (PQFP) without Heat Spreader | 208 | 8 | 30 | 23 | °C/W |
| Plastic Quad Flat Pack (PQFP) with Heat Spreader | 208 | 3.8 | 20 | 17 | °C/W |
| Plastic Ball Grid Array (PBGA) | 272 | 3 | 20 | 14.5 | °C/W |
| Plastic Ball Grid Array (PBGA) | 313 | 3 | 23 | 17 | °C/W |
| Plastic Ball Grid Array (PBGA) | 329 | 3 | 18 | 13.5 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 144 | 3.8 | 38.8 | 26.7 | °C/W |

**Note:** *SX08 does not have a heat spreader.*

*Table 1-16 •* **Temperature and Voltage Derating Factors\***

| $V_{CCA}$ | Junction Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| | **–55** | **–40** | **0** | **25** | **70** | **85** | **125** |
| **3.0** | 0.75 | 0.78 | 0.87 | 0.89 | 1.00 | 1.04 | 1.16 |
| **3.3** | 0.70 | 0.73 | 0.82 | 0.83 | 0.93 | 0.97 | 1.08 |
| **3.6** | 0.66 | 0.69 | 0.77 | 0.78 | 0.87 | 0.92 | 1.02 |

**Note:** *\*Normalized to worst-case commercial, $T_J$ = 70°C, $V_{CCA}$ = 3.0 V*

# A54SX08 Timing Characteristics

*Table 1-17 •* **A54SX08 Timing Characteristics**
**(Worst-Case Commercial Conditions, $V_{CCR}$ = 4.75 V, $V_{CCA}$, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | '–3' Speed Min. | '–3' Speed Max. | '–2' Speed Min. | '–2' Speed Max. | '–1' Speed Min. | '–1' Speed Max. | 'Std' Speed Min. | 'Std' Speed Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| **C-Cell Propagation Delays[1]** | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| **Predicted Routing Delays[2]** | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |
| **R-Cell Timing** | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.8 | | 1.1 | | 1.2 | | 1.4 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.0 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.5 | | 0.5 | | 0.7 | | 0.8 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y HIGH | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y LOW | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |

*Note:*

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

# A54SX16P Timing Characteristics

*Table 1-19* • **A54SX16P Timing Characteristics**
**(Worst-Case Commercial Conditions, $V_{CCR}$ = 4.75 V, $V_{CCA}$, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | '–3' Speed Min. | '–3' Speed Max. | '–2' Speed Min. | '–2' Speed Max. | '–1' Speed Min. | '–1' Speed Max. | 'Std' Speed Min. | 'Std' Speed Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| **C-Cell Propagation Delays**[1] | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| **Predicted Routing Delays**[2] | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |
| **R-Cell Timing** | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.9 | | 1.1 | | 1.3 | | 1.4 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.0 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.5 | | 0.5 | | 0.7 | | 0.8 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y HIGH | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y LOW | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| **Predicted Input Routing Delays**[2] | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |

***Note:***

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

3. *Delays based on 10 pF loading.*

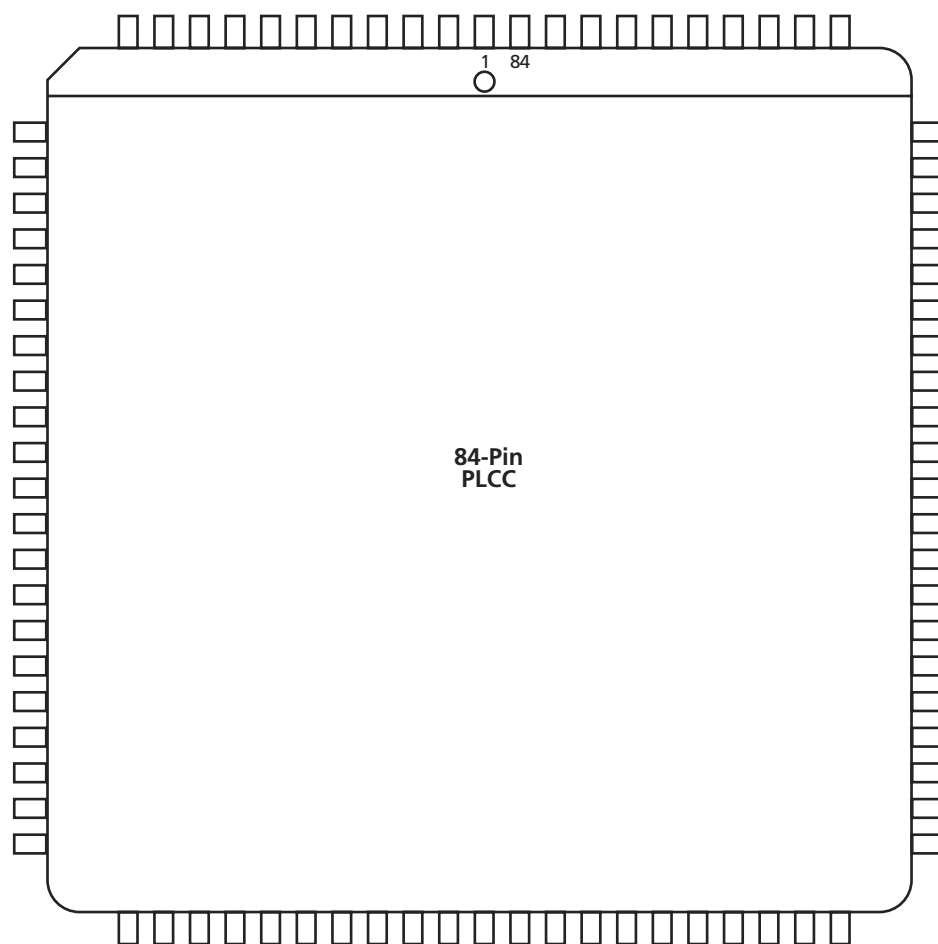# Package Pin Assignments

## 84-Pin PLCC



*Figure 2-1* • **84-Pin PLCC (Top View)**

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 208-Pin PQFP | | | | 208-Pin PQFP | | | |
|---|---|---|---|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function | Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 145 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | 181 | CLKB | CLKB | CLKB |
| 146 | GND | GND | GND | 182 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 147 | I/O | I/O | I/O | 183 | GND | GND | GND |
| 148 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | 184 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 149 | I/O | I/O | I/O | 185 | GND | GND | GND |
| 150 | I/O | I/O | I/O | 186 | PRA, I/O | PRA, I/O | PRA, I/O |
| 151 | I/O | I/O | I/O | 187 | I/O | I/O | I/O |
| 152 | I/O | I/O | I/O | 188 | I/O | I/O | I/O |
| 153 | I/O | I/O | I/O | 189 | NC | I/O | I/O |
| 154 | I/O | I/O | I/O | 190 | I/O | I/O | I/O |
| 155 | NC | I/O | I/O | 191 | I/O | I/O | I/O |
| 156 | NC | I/O | I/O | 192 | NC | I/O | I/O |
| 157 | GND | GND | GND | 193 | I/O | I/O | I/O |
| 158 | I/O | I/O | I/O | 194 | I/O | I/O | I/O |
| 159 | I/O | I/O | I/O | 195 | NC | I/O | I/O |
| 160 | I/O | I/O | I/O | 196 | I/O | I/O | I/O |
| 161 | I/O | I/O | I/O | 197 | I/O | I/O | I/O |
| 162 | I/O | I/O | I/O | 198 | NC | I/O | I/O |
| 163 | I/O | I/O | I/O | 199 | I/O | I/O | I/O |
| 164 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | 200 | I/O | I/O | I/O |
| 165 | I/O | I/O | I/O | 201 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 166 | I/O | I/O | I/O | 202 | NC | I/O | I/O |
| 167 | NC | I/O | I/O | 203 | NC | I/O | I/O |
| 168 | I/O | I/O | I/O | 204 | I/O | I/O | I/O |
| 169 | I/O | I/O | I/O | 205 | NC | I/O | I/O |
| 170 | NC | I/O | I/O | 206 | I/O | I/O | I/O |
| 171 | I/O | I/O | I/O | 207 | I/O | I/O | I/O |
| 172 | I/O | I/O | I/O | 208 | TCK, I/O | TCK, I/O | TCK, I/O |
| 173 | NC | I/O | I/O | | | | |
| 174 | I/O | I/O | I/O | | | | |
| 175 | I/O | I/O | I/O | | | | |
| 176 | NC | I/O | I/O | | | | |
| 177 | I/O | I/O | I/O | | | | |
| 178 | I/O | I/O | I/O | | | | |
| 179 | I/O | I/O | I/O | | | | |
| 180 | CLKA | CLKA | CLKA | | | | |

**Note:** *Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

| 176-Pin TQFP | | | | 176-Pin TQFP | | | |
|---|---|---|---|---|---|---|---|
| **Pin Number** | **A54SX08 Function** | **A54SX16, A54SX16P Function** | **A54SX32 Function** | **Pin Number** | **A54SX08 Function** | **A54SX16, A54SX16P Function** | **A54SX32 Function** |
| 69 | HCLK | HCLK | HCLK | 103 | I/O | I/O | I/O |
| 70 | I/O | I/O | I/O | 104 | I/O | I/O | I/O |
| 71 | I/O | I/O | I/O | 105 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O | 106 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O | 107 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O | 108 | GND | GND | GND |
| 75 | I/O | I/O | I/O | 109 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 76 | I/O | I/O | I/O | 110 | GND | GND | GND |
| 77 | I/O | I/O | I/O | 111 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O | 112 | I/O | I/O | I/O |
| 79 | NC | I/O | I/O | 113 | I/O | I/O | I/O |
| 80 | I/O | I/O | I/O | 114 | I/O | I/O | I/O |
| 81 | NC | I/O | I/O | 115 | I/O | I/O | I/O |
| 82 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | 116 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O | 117 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O | 118 | NC | I/O | I/O |
| 85 | I/O | I/O | I/O | 119 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O | 120 | NC | I/O | I/O |
| 87 | TDO, I/O | TDO, I/O | TDO, I/O | 121 | NC | I/O | I/O |
| 88 | I/O | I/O | I/O | 122 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 89 | GND | GND | GND | 123 | GND | GND | GND |
| 90 | NC | I/O | I/O | 124 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 91 | NC | I/O | I/O | 125 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O | 126 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O | 127 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O | 128 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O | 129 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O | 130 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O | 131 | NC | I/O | I/O |
| 98 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | 132 | NC | I/O | I/O |
| 99 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | 133 | GND | GND | GND |
| 100 | I/O | I/O | I/O | 134 | I/O | I/O | I/O |
| 101 | I/O | I/O | I/O | 135 | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O | 136 | I/O | I/O | I/O |

| 176-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | I/O | I/O | I/O |
| 145 | I/O | I/O | I/O |
| 146 | I/O | I/O | I/O |
| 147 | I/O | I/O | I/O |
| 148 | I/O | I/O | I/O |
| 149 | I/O | I/O | I/O |
| 150 | I/O | I/O | I/O |
| 151 | I/O | I/O | I/O |
| 152 | CLKA | CLKA | CLKA |
| 153 | CLKB | CLKB | CLKB |
| 154 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 155 | GND | GND | GND |
| 156 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |

| 176-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 157 | PRA, I/O | PRA, I/O | PRA, I/O |
| 158 | I/O | I/O | I/O |
| 159 | I/O | I/O | I/O |
| 160 | I/O | I/O | I/O |
| 161 | I/O | I/O | I/O |
| 162 | I/O | I/O | I/O |
| 163 | I/O | I/O | I/O |
| 164 | I/O | I/O | I/O |
| 165 | I/O | I/O | I/O |
| 166 | I/O | I/O | I/O |
| 167 | I/O | I/O | I/O |
| 168 | NC | I/O | I/O |
| 169 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 170 | I/O | I/O | I/O |
| 171 | NC | I/O | I/O |
| 172 | NC | I/O | I/O |
| 173 | NC | I/O | I/O |
| 174 | I/O | I/O | I/O |
| 175 | I/O | I/O | I/O |
| 176 | TCK, I/O | TCK, I/O | TCK, I/O |

| 100-Pin VQFP | | |
|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function |
| 1 | GND | GND |
| 2 | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | TMS | TMS |
| 8 | $V_{CCI}$ | $V_{CCI}$ |
| 9 | GND | GND |
| 10 | I/O | I/O |
| 11 | I/O | I/O |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | I/O | I/O |
| 15 | I/O | I/O |
| 16 | I/O | I/O |
| 17 | I/O | I/O |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | $V_{CCI}$ | $V_{CCI}$ |
| 21 | I/O | I/O |
| 22 | I/O | I/O |
| 23 | I/O | I/O |
| 24 | I/O | I/O |
| 25 | I/O | I/O |
| 26 | I/O | I/O |
| 27 | I/O | I/O |
| 28 | I/O | I/O |
| 29 | I/O | I/O |
| 30 | I/O | I/O |
| 31 | I/O | I/O |
| 32 | I/O | I/O |
| 33 | I/O | I/O |
| 34 | PRB, I/O | PRB, I/O |

| 100-Pin VQFP | | |
|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function |
| 35 | $V_{CCA}$ | $V_{CCA}$ |
| 36 | GND | GND |
| 37 | $V_{CCR}$ | $V_{CCR}$ |
| 38 | I/O | I/O |
| 39 | HCLK | HCLK |
| 40 | I/O | I/O |
| 41 | I/O | I/O |
| 42 | I/O | I/O |
| 43 | I/O | I/O |
| 44 | $V_{CCI}$ | $V_{CCI}$ |
| 45 | I/O | I/O |
| 46 | I/O | I/O |
| 47 | I/O | I/O |
| 48 | I/O | I/O |
| 49 | TDO, I/O | TDO, I/O |
| 50 | I/O | I/O |
| 51 | GND | GND |
| 52 | I/O | I/O |
| 53 | I/O | I/O |
| 54 | I/O | I/O |
| 55 | I/O | I/O |
| 56 | I/O | I/O |
| 57 | $V_{CCA}$ | $V_{CCA}$ |
| 58 | $V_{CCI}$ | $V_{CCI}$ |
| 59 | I/O | I/O |
| 60 | I/O | I/O |
| 61 | I/O | I/O |
| 62 | I/O | I/O |
| 63 | I/O | I/O |
| 64 | I/O | I/O |
| 65 | I/O | I/O |
| 66 | I/O | I/O |
| 67 | $V_{CCA}$ | $V_{CCA}$ |
| 68 | GND | GND |

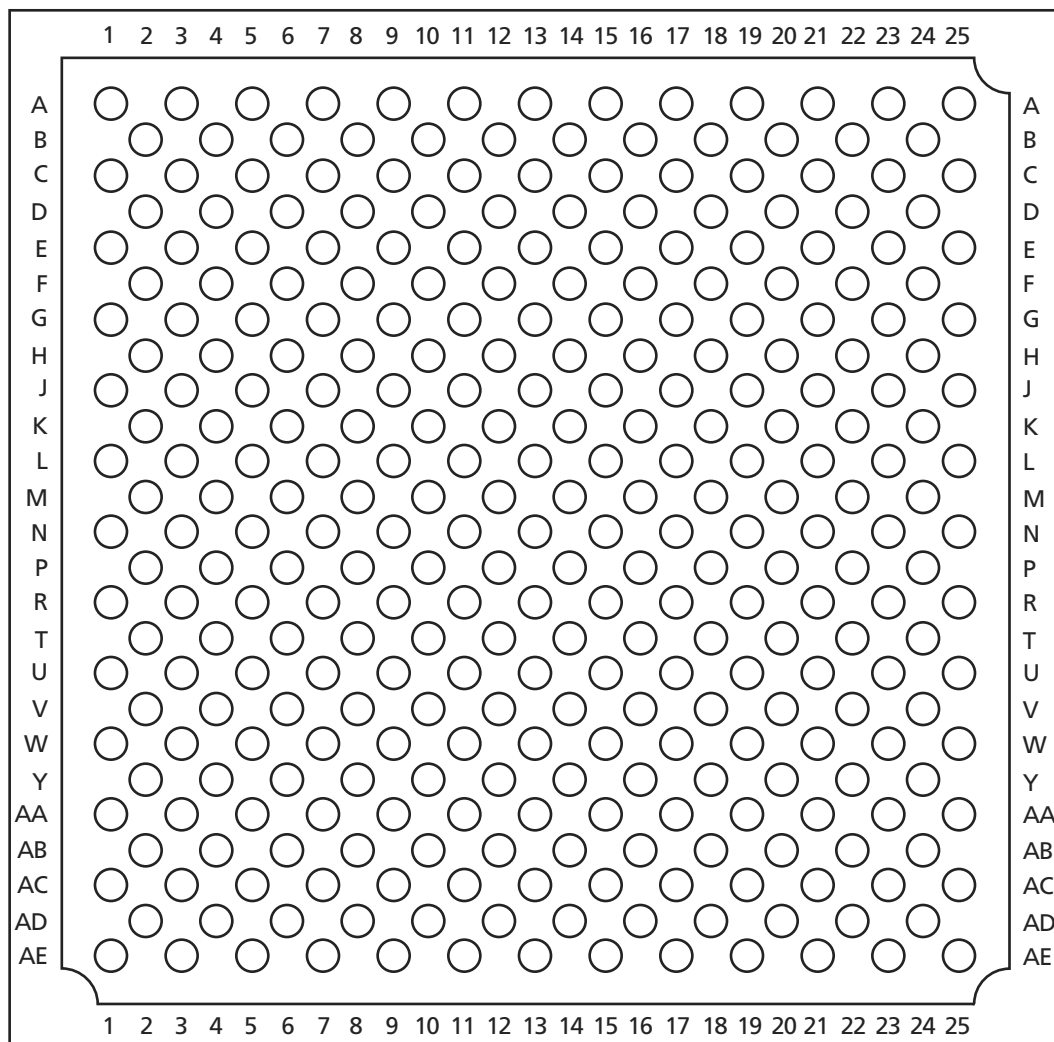| 100-Pin VQFP | | |
|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function |
| 69 | GND | GND |
| 70 | I/O | I/O |
| 71 | I/O | I/O |
| 72 | I/O | I/O |
| 73 | I/O | I/O |
| 74 | I/O | I/O |
| 75 | I/O | I/O |
| 76 | I/O | I/O |
| 77 | I/O | I/O |
| 78 | I/O | I/O |
| 79 | I/O | I/O |
| 80 | I/O | I/O |
| 81 | I/O | I/O |
| 82 | $V_{CCI}$ | $V_{CCI}$ |
| 83 | I/O | I/O |
| 84 | I/O | I/O |
| 85 | I/O | I/O |
| 86 | I/O | I/O |
| 87 | CLKA | CLKA |
| 88 | CLKB | CLKB |
| 89 | $V_{CCR}$ | $V_{CCR}$ |
| 90 | $V_{CCA}$ | $V_{CCA}$ |
| 91 | GND | GND |
| 92 | PRA, I/O | PRA, I/O |
| 93 | I/O | I/O |
| 94 | I/O | I/O |
| 95 | I/O | I/O |
| 96 | I/O | I/O |
| 97 | I/O | I/O |
| 98 | I/O | I/O |
| 99 | I/O | I/O |
| 100 | TCK, I/O | TCK, I/O |

# 313-Pin PBGA



*Figure 2-6* • **313-Pin PBGA (Top View)**

## Note

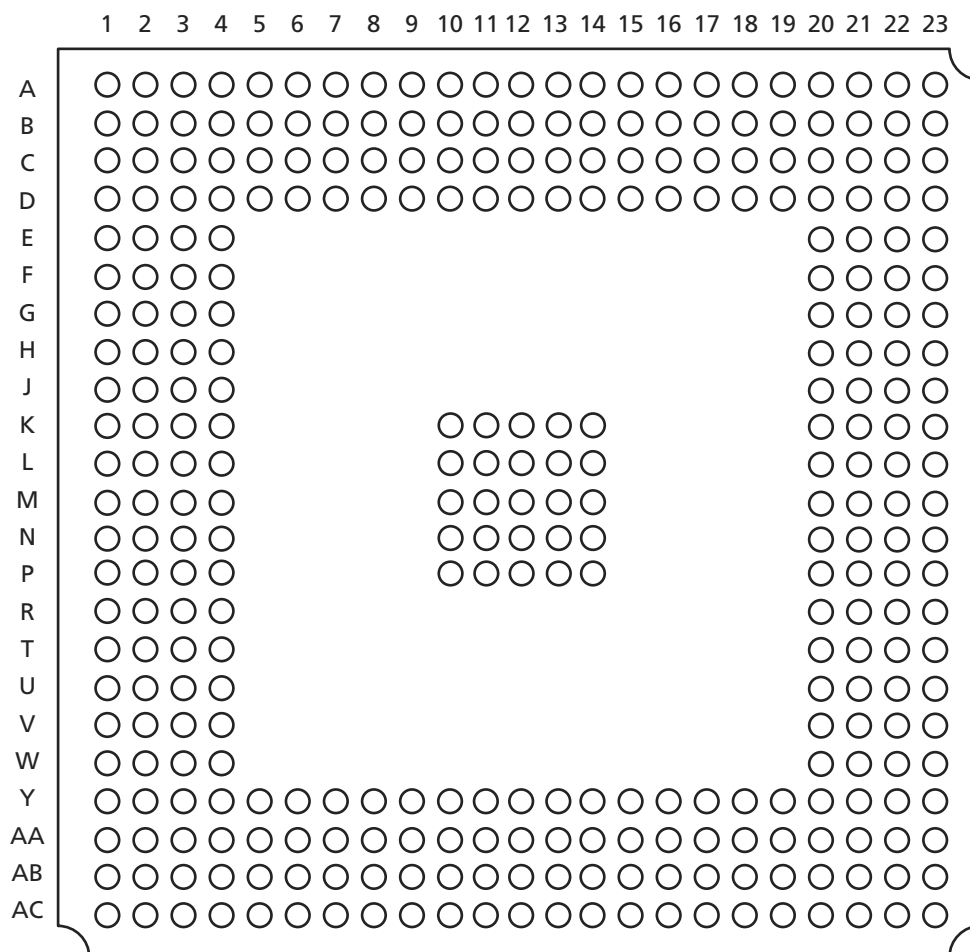For Package Manufacturing and Environmental information, visit the Package Resource center at
http://www.actel.com/products/rescenter/package/index.html.

# 329-Pin PBGA



*Figure 2-7* • **329-Pin PBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.
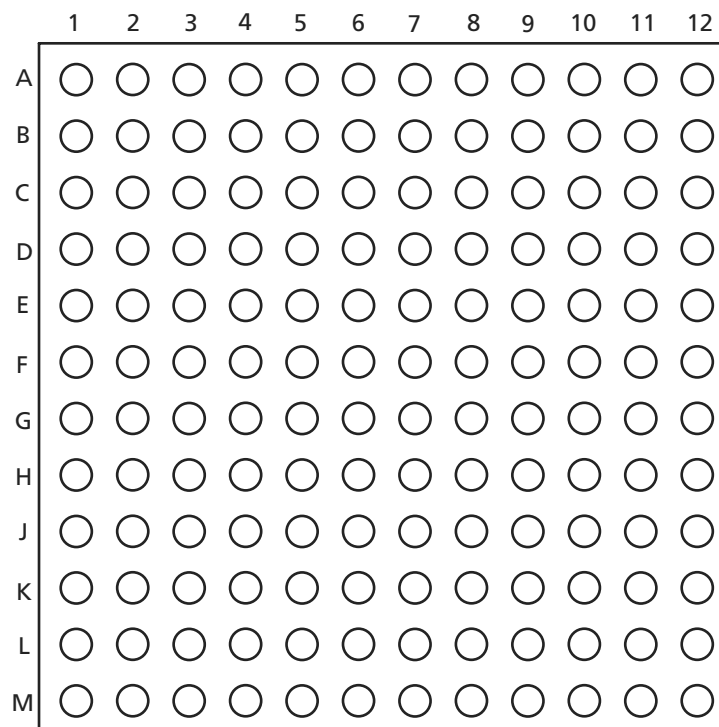
## 144-Pin FBGA



*Figure 2-8 •* **144-Pin FBGA (Top View)**

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at
http://www.actel.com/products/rescenter/package/index.html.

Actel and the Actel logo are registered trademarks of Actel Corporation.
All other trademarks are the property of their owners.

www.actel.com

**Actel Corporation**

2061 Stierlin Court
Mountain View, CA
94043-4655  USA
**Phone** 650.318.4200
**Fax** 650.318.4600

**Actel Europe Ltd.**

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
**Phone** +44 (0) 1276 401 450
**Fax** +44 (0) 1276 401 490

**Actel Japan**
www.jp.actel.com
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150  Japan
**Phone** +81.03.3445.7671
**Fax** +81.03.3445.7668

**Actel Hong Kong**
www.actel.com.cn
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
**Phone** +852 2185 6460
**Fax** +852 2185 6488

5172137-5/6.06