



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

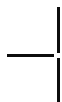
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	113
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-1tq144">https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-1tq144</a>



---

# Table of Contents

---

## **SX Family FPGAs**

General Description .....	1-1
SX Family Architecture .....	1-1
Programming .....	1-7
3.3 V / 5 V Operating Conditions .....	1-7
PCI Compliance for the SX Family .....	1-9
A54SX16P AC Specifications for (PCI Operation) .....	1-10
A54SX16P DC Specifications (3.3 V PCI Operation) .....	1-12
A54SX16P AC Specifications (3.3 V PCI Operation) .....	1-13
Power-Up Sequencing .....	1-15
Power-Down Sequencing .....	1-15
Evaluating Power in SX Devices .....	1-16
SX Timing Model .....	1-21
Timing Characteristics .....	1-23

## **Package Pin Assignments**

84-Pin PLCC .....	2-1
208-Pin PQFP .....	2-3
144-Pin TQFP .....	2-7
176-Pin TQFP .....	2-10
100-Pin VQFP .....	2-14
313-Pin PBGA .....	2-16
329-Pin PBGA .....	2-19
144-Pin FBGA .....	2-23

## **Datasheet Information**

List of Changes .....	3-1
Datasheet Categories .....	3-1
International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR) .....	3-1

## Chip Architecture

The SX family chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

## Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *clusters*. There are two types of *clusters*: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (Figure 1-4). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

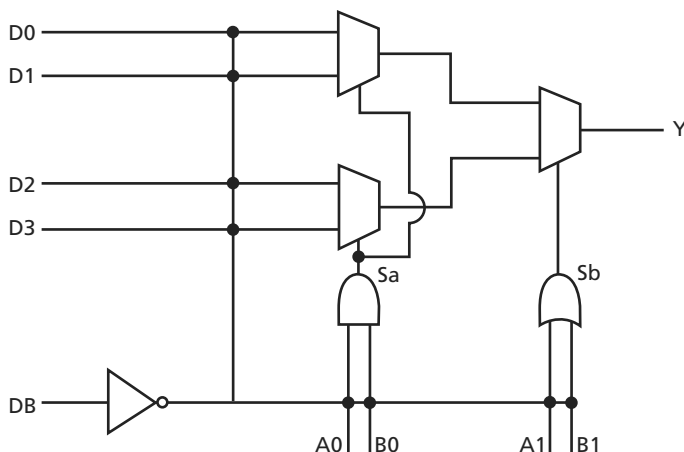


Figure 1-3 • C-Cell

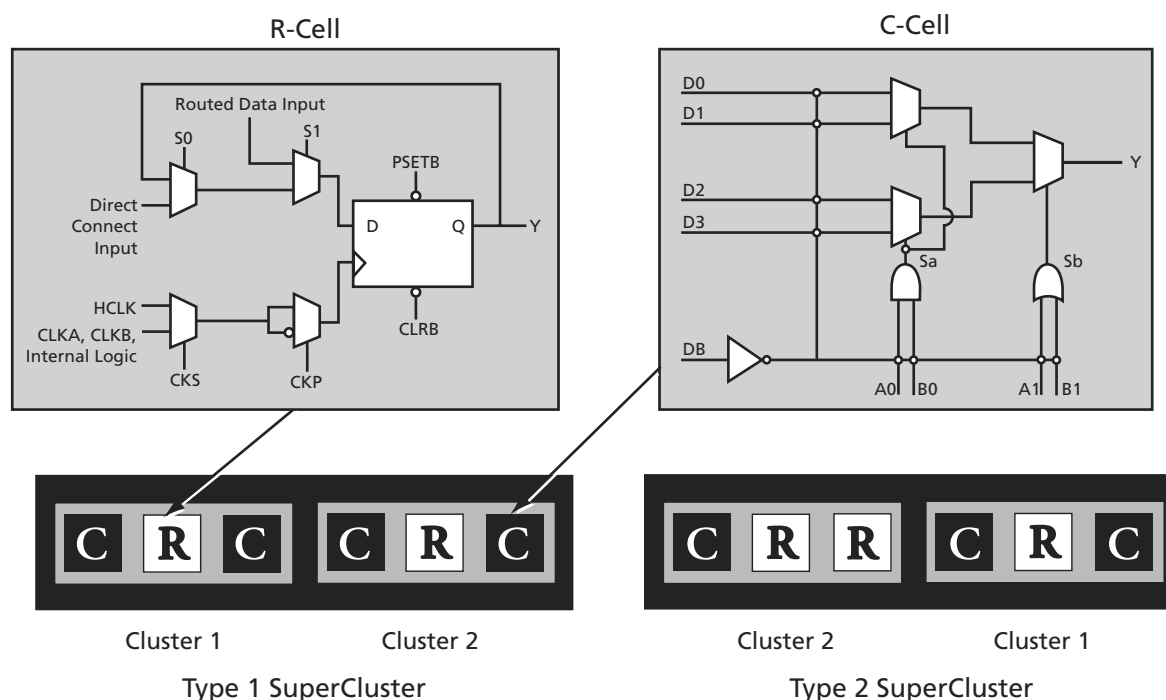


Figure 1-4 • Cluster Organization

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

The Actel high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hardwired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

## Other Architectural Features

### Technology

The Actel SX family is implemented on a high-voltage twin-well CMOS process using 0.35  $\mu$  design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25  $\Omega$  with a capacitance of 1.0 fF for low signal impedance.

## Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

## I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin.

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

## Power Requirements

The SX family supports 3.3 V operation and is designed to tolerate 5.0 V inputs. (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest power architecture on the market.

Table 1-1 • Supply Voltages

Device	V <sub>CCA</sub>	V <sub>CCI</sub>	V <sub>CCR</sub>	Maximum Input Tolerance	Maximum Output Drive
A54SX08 A54SX16 A54SX32	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
A54SX16-P*	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V

**Note:** \*A54SX16-P has three different entries because it is capable of both a 3.3 V and a 5.0 V drive.

Figure 1-9 shows the 5.0 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

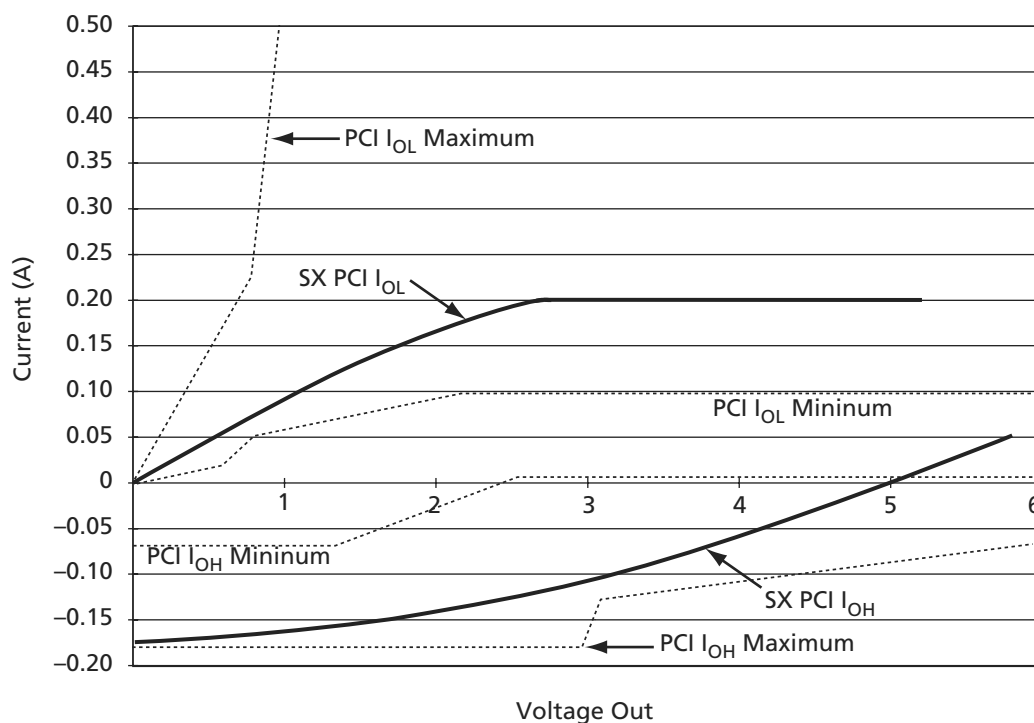


Figure 1-9 • 5.0 V PCI Curve for A54SX16P Device

$$I_{OH} = 11.9 \times (V_{OUT} - 5.25) \times (V_{OUT} + 2.45)$$

for  $V_{CC} > V_{OUT} > 3.1$  V

EQ 1-1

$$I_{OL} = 78.5 \times V_{OUT} \times (4.4 - V_{OUT})$$

for  $0$  V  $< V_{OUT} < 0.71$  V

EQ 1-2

## A54SX16P DC Specifications (3.3 V PCI Operation)

Table 1-8 • A54SX16P DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$V_{CCA}$	Supply Voltage for Array		3.0	3.6	V
$V_{CCR}$	Supply Voltage required for Internal Biasing		3.0	3.6	V
$V_{CCI}$	Supply Voltage for I/Os		3.0	3.6	V
$V_{IH}$	Input High Voltage		$0.5V_{CC}$	$V_{CC} + 0.5$	V
$V_{IL}$	Input Low Voltage		-0.5	$0.3V_{CC}$	V
$I_{IPU}$	Input Pull-up Voltage <sup>1</sup>		$0.7V_{CC}$		V
$I_{IL}$	Input Leakage Current <sup>2</sup>	$0 < V_{IN} < V_{CC}$		$\pm 10$	$\mu A$
$V_{OH}$	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CC}$		V
$V_{OL}$	Output Low Voltage	$I_{OUT} = 1500 \mu A$		$0.1V_{CC}$	V
$C_{IN}$	Input Pin Capacitance <sup>3</sup>			10	pF
$C_{CLK}$	CLK Pin Capacitance		5	12	pF
$C_{IDSEL}$	IDSEL Pin Capacitance <sup>4</sup>			8	pF

### Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

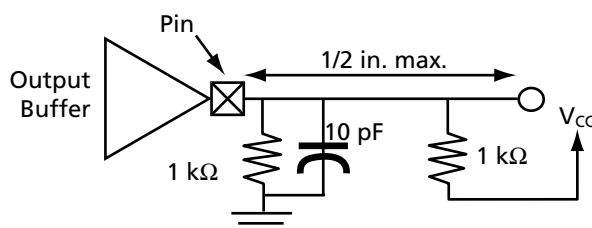
# A54SX16P AC Specifications (3.3 V PCI Operation)

Table 1-9 • A54SX16P AC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CC}^1$			mA
		$0.3V_{CC} \leq V_{OUT} < 0.9V_{CC}^1$	$-12V_{CC}$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}^{1,2}$	$-17.1 + (V_{CC} - V_{OUT})$	EQ 1-3 on page 1-14	
	(Test Point)	$V_{OUT} = 0.7V_{CC}^2$		$-32V_{CC}$	mA
$I_{OL(AC)}$	Switching Current High	$V_{CC} > V_{OUT} \geq 0.6V_{CC}^1$			mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}^1$	$16V_{CC}$		mA
		$0.18V_{CC} > V_{OUT} > 0^{1,2}$	$26.7V_{OUT}$	EQ 1-4 on page 1-14	mA
	(Test Point)	$V_{OUT} = 0.18V_{CC}^2$		$38V_{CC}$	
$I_{CL}$	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$I_{CH}$	High Clamp Current	$-3 < V_{IN} \leq -1$	$25 + (V_{IN} - V_{OUT} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate <sup>3</sup>	0.2V <sub>CC</sub> to 0.6V <sub>CC</sub> load	1	4	V/ns
$slew_F$	Output Fall Slew Rate <sup>3</sup>	0.6V <sub>CC</sub> to 0.2V <sub>CC</sub> load	1	4	V/ns

## Notes:

1. Refer to the V/I curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.



## Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

## Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}}$$

EQ 1-5

## DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • Standby Power

I <sub>CC</sub>	V <sub>CC</sub>	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

$$P_{\text{DC}} = (I_{\text{standby}}) \times V_{\text{CCA}} + (I_{\text{standby}}) \times V_{\text{CCR}} + (I_{\text{standby}}) \times V_{\text{CCI}} + xV_{\text{OL}} \times I_{\text{OL}} + y(V_{\text{CCI}} - V_{\text{OH}}) \times V_{\text{OH}}$$

EQ 1-6

## AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-7

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 \times (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 \times (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 \times (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-8

## Definition of Terms Used in Formula

- m = Number of logic modules switching at  $f_m$
- n = Number of input buffers switching at  $f_n$
- p = Number of output buffers switching at  $f_p$
- q<sub>1</sub> = Number of clock loads on the first routed array clock
- q<sub>2</sub> = Number of clock loads on the second routed array clock
- x = Number of I/Os at logic low
- y = Number of I/Os at logic high
- r<sub>1</sub> = Fixed capacitance due to first routed array clock
- r<sub>2</sub> = Fixed capacitance due to second routed array clock
- s<sub>1</sub> = Number of clock loads on the dedicated array clock
- C<sub>EQM</sub> = Equivalent capacitance of logic modules in pF
- C<sub>EQI</sub> = Equivalent capacitance of input buffers in pF
- C<sub>EQO</sub> = Equivalent capacitance of output buffers in pF
- C<sub>EQCR</sub> = Equivalent capacitance of routed array clock in pF
- C<sub>EQHV</sub> = Variable capacitance of dedicated array clock
- C<sub>EQHF</sub> = Fixed capacitance of dedicated array clock
- C<sub>L</sub> = Output lead capacitance in pF
- f<sub>m</sub> = Average logic module switching rate in MHz
- f<sub>n</sub> = Average input buffer switching rate in MHz
- f<sub>p</sub> = Average output buffer switching rate in MHz
- f<sub>q1</sub> = Average first routed array clock rate in MHz
- f<sub>q2</sub> = Average second routed array clock rate in MHz
- f<sub>s1</sub> = Average dedicated array clock rate in MHz



Table 1-13 shows capacitance values for various devices.

Table 1-13 • Capacitance Values for Devices

	<b>A545X08</b>	<b>A545X16</b>	<b>A545X16P</b>	<b>A545X32</b>
$C_{EQM}$ (pF)	4.0	4.0	4.0	4.0
$C_{EQI}$ (pF)	3.4	3.4	3.4	3.4
$C_{EQO}$ (pF)	4.7	4.7	4.7	4.7
$C_{EQCR}$ (pF)	1.6	1.6	1.6	1.6
$C_{EQHV}$	0.615	0.615	0.615	0.615
$C_{EQHF}$	60	96	96	140
$r_1$ (pF)	87	138	138	171
$r_2$ (pF)	87	138	138	171

Table 1-14 • Power Consumption Guidelines

<b>Description</b>	<b>Power Consumption Guideline</b>
Logic Modules (m)	20% of modules
Inputs Switching (n)	# inputs/4
Outputs Switching (p)	# outputs/4
First Routed Array Clock Loads ( $q_1$ )	20% of register cells
Second Routed Array Clock Loads ( $q_2$ )	20% of register cells
Load Capacitance ( $C_L$ )	35 pF
Average Logic Module Switching Rate ( $f_m$ )	$f/10$
Average Input Switching Rate ( $f_n$ )	$f/5$
Average Output Switching Rate ( $f_p$ )	$f/10$
Average First Routed Array Clock Rate ( $f_{q1}$ )	$f/2$
Average Second Routed Array Clock Rate ( $f_{q2}$ )	$f/2$
Average Dedicated Array Clock Rate ( $f_{s1}$ )	$f$
Dedicated Clock Array Clock Loads ( $s_1$ )	20% of regular modules

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{\text{Total}} = P_{\text{AC}} \text{ (dynamic power)} + P_{\text{DC}} \text{ (static power)}$$

EQ 1-9

## Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

### Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A545X16P device. A pattern of 0101... was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101... caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

### AC Power Dissipation

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-10

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-11

**Step 1: Define Terms Used in Formula**

	$V_{CCA}$	3.3
<b>Module</b>		
Number of logic modules switching at $f_m$ (Used 50%)	$m$	264
Average logic modules switching rate $f_m$ (MHz) (Guidelines: $f/10$ )	$f_m$	20
Module capacitance $C_{EQM}$ (pF)	$C_{EQM}$	4.0
<b>Input Buffer</b>		
Number of input buffers switching at $f_n$	$n$	1
Average input switching rate $f_n$ (MHz) (Guidelines: $f/5$ )	$f_n$	40
Input buffer capacitance $C_{EQI}$ (pF)	$C_{EQI}$	3.4
<b>Output Buffer</b>		
Number of output buffers switching at $f_p$	$p$	1
Average output buffers switching rate $f_p$ (MHz) (Guidelines: $f/10$ )	$f_p$	20
Output buffers buffer capacitance $C_{EQO}$ (pF)	$C_{EQO}$	4.7
Output Load capacitance $C_L$ (pF)	$C_L$	35
<b>RCLKA</b>		
Number of Clock loads $q_1$	$q_1$	528
Capacitance of routed array clock (pF)	$C_{EQCR}$	1.6
Average clock rate (MHz)	$f_{q1}$	200
Fixed capacitance (pF)	$r_1$	138
<b>RCLKB</b>		
Number of Clock loads $q_2$	$q_2$	0
Capacitance of routed array clock (pF)	$C_{EQCR}$	1.6
Average clock rate (MHz)	$f_{q2}$	0
Fixed capacitance (pF)	$r_2$	138
<b>HCLK</b>		
Number of Clock loads	$s_1$	0
Variable capacitance of dedicated array clock (pF)	$C_{EQHV}$	0.61 5
Fixed capacitance of dedicated array clock (pF)	$C_{EQHF}$	96
Average clock rate (MHz)	$f_{s1}$	0

**Step 2: Calculate Dynamic Power Consumption**

$V_{CCA} \times V_{CCA}$	10.89
$m \times f_m \times C_{EQM}$	0.02112
$n \times f_n \times C_{EQI}$	0.000136
$p \times f_p \times (C_{EQO} + C_L)$	0.000794
$0.5 (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1})$	0.11208
$0.5 (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2})$	0
$0.5 (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1})$	0
$P_{AC} = 1.461 \text{ W}$	

**Step 3: Calculate DC Power Dissipation****DC Power Dissipation**

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + X \times V_{OL} \times I_{OL} + Y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-12

For a rough estimate of DC Power Dissipation, only use  $P_{DC} = (I_{standby}) \times V_{CCA}$ . The rest of the formula provides a very small number that can be considered negligible.

$$P_{DC} = (I_{standby}) \times V_{CCA}$$

$$P_{DC} = .55 \text{ mA} \times 3.3 \text{ V}$$

$$P_{DC} = 0.001815 \text{ W}$$

**Step 4: Calculate Total Power Consumption**

$$P_{Total} = P_{AC} + P_{DC}$$

$$P_{Total} = 1.461 + 0.001815$$

$$P_{Total} = 1.4628 \text{ W}$$

**Step 5: Compare Estimated Power Consumption against Characterized Power Consumption**

The estimated total power consumption for this design is 1.46 W. The characterized power consumption for this design at 200 MHz is 1.0164 W.

## A54SX08 Timing Characteristics

Table 1-17 • **A54SX08 Timing Characteristics**  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>1</sup>										
t <sub>PD</sub>	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays <sup>2</sup>										
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t <sub>RCO</sub>	Sequential Clock-to-Q	0.8		1.1		1.2		1.4		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t <sub>INYH</sub>	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t <sub>INYL</sub>	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Input Module Predicted Routing Delays <sup>2</sup>										
t <sub>IRD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>IRD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

**Note:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics**  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>1</sup>										
t <sub>PD</sub>	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays <sup>2</sup>										
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t <sub>RCO</sub>	Sequential Clock-to-Q	0.8		1.1		1.2		1.4		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t <sub>INYH</sub>	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t <sub>INYL</sub>	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays <sup>2</sup>										
t <sub>IRD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>IRD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

### Notes:

1. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 35 pF loading, except  $t_{ENZL}$  and  $t_{ENZH}$ . For  $t_{ENZL}$  and  $t_{ENZH}$ , the loading is 5 pF.

## A54SX16P Timing Characteristics

Table 1-19 • **A54SX16P Timing Characteristics**  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>1</sup>										
t <sub>PD</sub>	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays <sup>2</sup>										
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t <sub>RCO</sub>	Sequential Clock-to-Q	0.9		1.1		1.3		1.4		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t <sub>INYH</sub>	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t <sub>INYL</sub>	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays <sup>2</sup>										
t <sub>IRD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>IRD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

**Note:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 10 pF loading.

**Table 1-19 • A54SX16P Timing Characteristics (Continued)**  
**(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t <sub>HCKH</sub>	Input LOW to HIGH (pad to R-Cell input)	1.2		1.4		1.5		1.8		ns
t <sub>HCKL</sub>	Input HIGH to LOW (pad to R-Cell input)	1.2		1.4		1.6		1.9		ns
t <sub>HPWH</sub>	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t <sub>HPWL</sub>	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t <sub>HCKSW</sub>	Maximum Skew	0.2		0.2		0.3		0.3		ns
t <sub>HP</sub>	Minimum Period	2.7		3.1		3.6		4.2		ns
f <sub>HMAX</sub>	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t <sub>RCKH</sub>	Input LOW to HIGH (light load) (pad to R-Cell input)	1.6		1.8		2.1		2.5		ns
t <sub>RCKL</sub>	Input HIGH to LOW (Light Load) (pad to R-Cell input)	1.8		2.0		2.3		2.7		ns
t <sub>RCKH</sub>	Input LOW to HIGH (50% load) (pad to R-Cell input)	1.8		2.1		2.5		2.8		ns
t <sub>RCKL</sub>	Input HIGH to LOW (50% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t <sub>RCKH</sub>	Input LOW to HIGH (100% load) (pad to R-Cell input)	1.8		2.1		2.4		2.8		ns
t <sub>RCKL</sub>	Input HIGH to LOW (100% load) (pad to R-Cell input)	2.0		2.2		2.5		3.0		ns
t <sub>RPWH</sub>	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t <sub>RPWL</sub>	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t <sub>RCKSW</sub>	Maximum Skew (light load)	0.5		0.5		0.5		0.7		ns
t <sub>RCKSW</sub>	Maximum Skew (50% load)	0.5		0.6		0.7		0.8		ns
t <sub>RCKSW</sub>	Maximum Skew (100% load)	0.5		0.6		0.7		0.8		ns
TTL Output Module Timing										
t <sub>DLH</sub>	Data-to-Pad LOW to HIGH	2.4		2.8		3.1		3.7		ns
t <sub>DHL</sub>	Data-to-Pad HIGH to LOW	2.3		2.9		3.2		3.8		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	3.0		3.4		3.9		4.6		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	3.3		3.8		4.3		5.0		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	2.3		2.7		3.0		3.5		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	2.8		3.2		3.7		4.3		ns

**Note:**

1. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 10 pF loading.

## A54SX32 Timing Characteristics

Table 1-20 • A54SX32 Timing Characteristics  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>1</sup>										
t <sub>PD</sub>	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays <sup>2</sup>										
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns
R-Cell Timing										
t <sub>RCO</sub>	Sequential Clock-to-Q	0.8		1.1		1.3		1.4		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t <sub>INYH</sub>	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t <sub>INYL</sub>	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays <sup>2</sup>										
t <sub>IRD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t <sub>IRD12</sub>	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns

### Note:

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except  $t_{ENZL}$  and  $t_{ENZH}$ . For  $t_{ENZL}$  and  $t_{ENZH}$  the loading is 5 pF.

Table 1-20 • **A54SX32 Timing Characteristics (Continued)**  
**(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t <sub>HCKH</sub>	Input LOW to HIGH (pad to R-Cell input)	1.9		2.1		2.4		2.8		ns
t <sub>HCKL</sub>	Input HIGH to LOW (pad to R-Cell input)	1.9		2.1		2.4		2.8		ns
t <sub>HPWH</sub>	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t <sub>HPWL</sub>	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t <sub>HCKSW</sub>	Maximum Skew	0.3		0.4		0.4		0.5		ns
t <sub>HP</sub>	Minimum Period	2.7		3.1		3.6		4.2		ns
f <sub>HMAX</sub>	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t <sub>RCKH</sub>	Input LOW to HIGH (light load) (pad to R-Cell input)	2.4		2.7		3.0		3.5		ns
t <sub>RCKL</sub>	Input HIGH to LOW (light load) (pad to R-Cell input)	2.4		2.7		3.1		3.6		ns
t <sub>RCKH</sub>	Input LOW to HIGH (50% load) (pad to R-Cell input)	2.7		3.0		3.5		4.1		ns
t <sub>RCKL</sub>	Input HIGH to LOW (50% load) (pad to R-Cell input)	2.7		3.1		3.6		4.2		ns
t <sub>RCKH</sub>	Input LOW to HIGH (100% load) (pad to R-Cell input)	2.7		3.1		3.5		4.1		ns
t <sub>RCKL</sub>	Input HIGH to LOW (100% load) (pad to R-Cell input)	2.8		3.2		3.6		4.3		ns
t <sub>RPWH</sub>	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t <sub>RPWL</sub>	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t <sub>RCKSW</sub>	Maximum Skew (light load)	0.85		0.98		1.1		1.3		ns
t <sub>RCKSW</sub>	Maximum Skew (50% load)	1.23		1.4		1.6		1.9		ns
t <sub>RCKSW</sub>	Maximum Skew (100% load)	1.30		1.5		1.7		2.0		ns
TTL Output Module Timing <sup>3</sup>										
t <sub>DLH</sub>	Data-to-Pad LOW to HIGH	1.6		1.9		2.1		2.5		ns
t <sub>DHL</sub>	Data-to-Pad HIGH to LOW	1.6		1.9		2.1		2.5		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	2.1		2.4		2.8		3.2		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	2.3		2.7		3.1		3.6		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	1.4		1.7		1.9		2.2		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	1.3		1.5		1.7		2.0		ns

**Note:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except  $t_{ENZL}$  and  $t_{ENZH}$ . For  $t_{ENZL}$  and  $t_{ENZH}$  the loading is 5 pF.



## 208-Pin PQFP

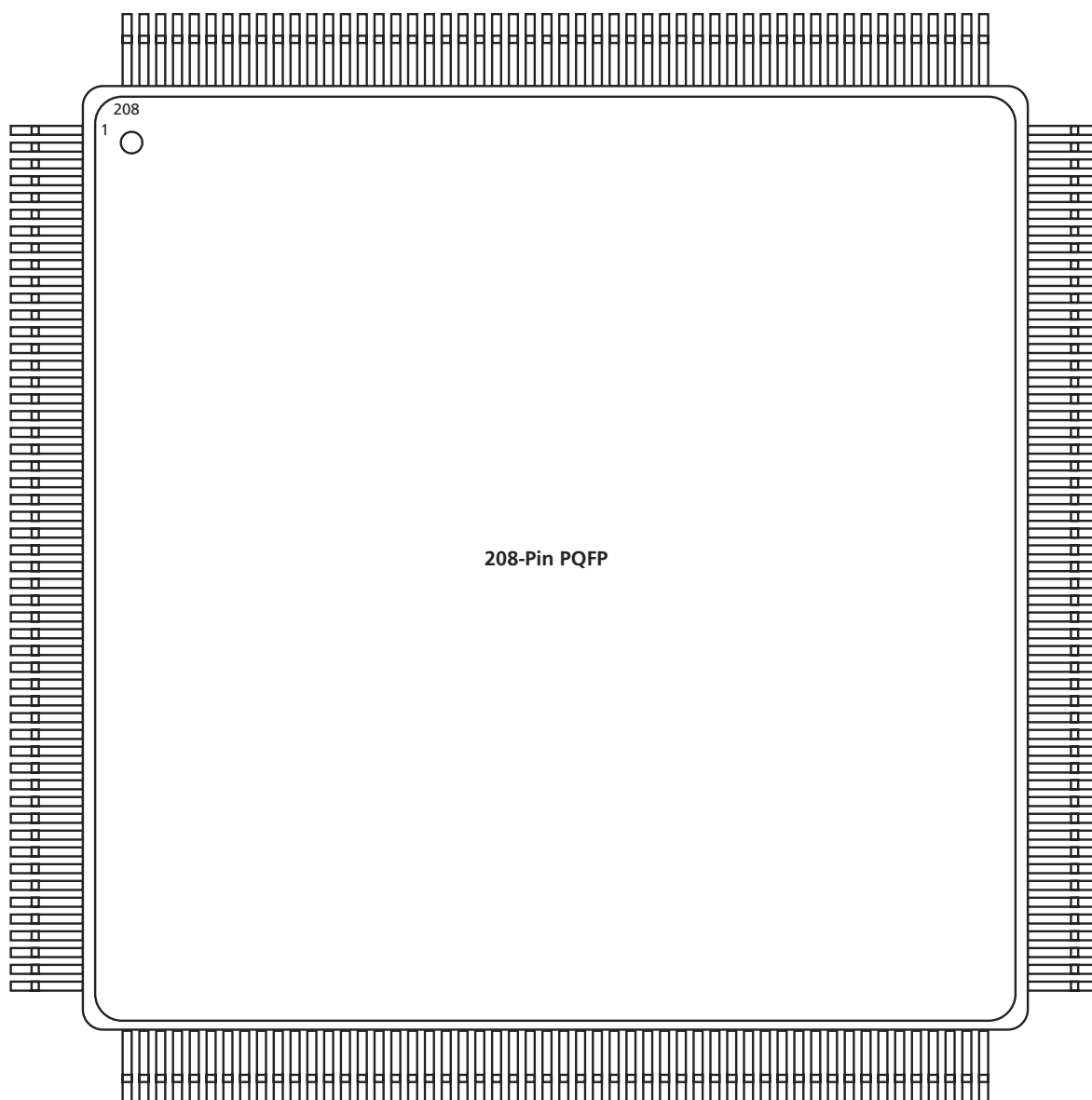


Figure 2-2 • 208-Pin PQFP (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

## 144-Pin TQFP

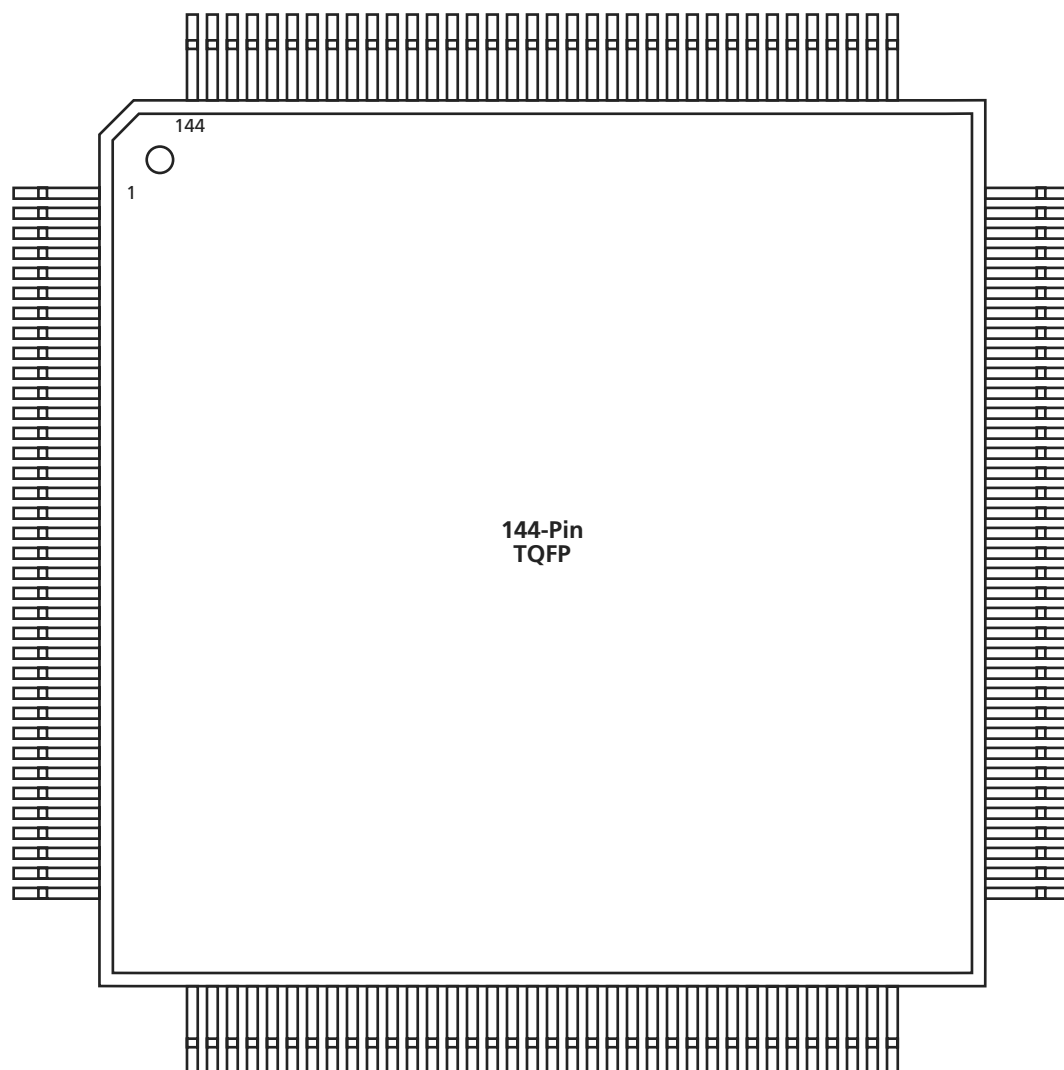


Figure 2-3 • 144-Pin TQFP (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

## 176-Pin TQFP

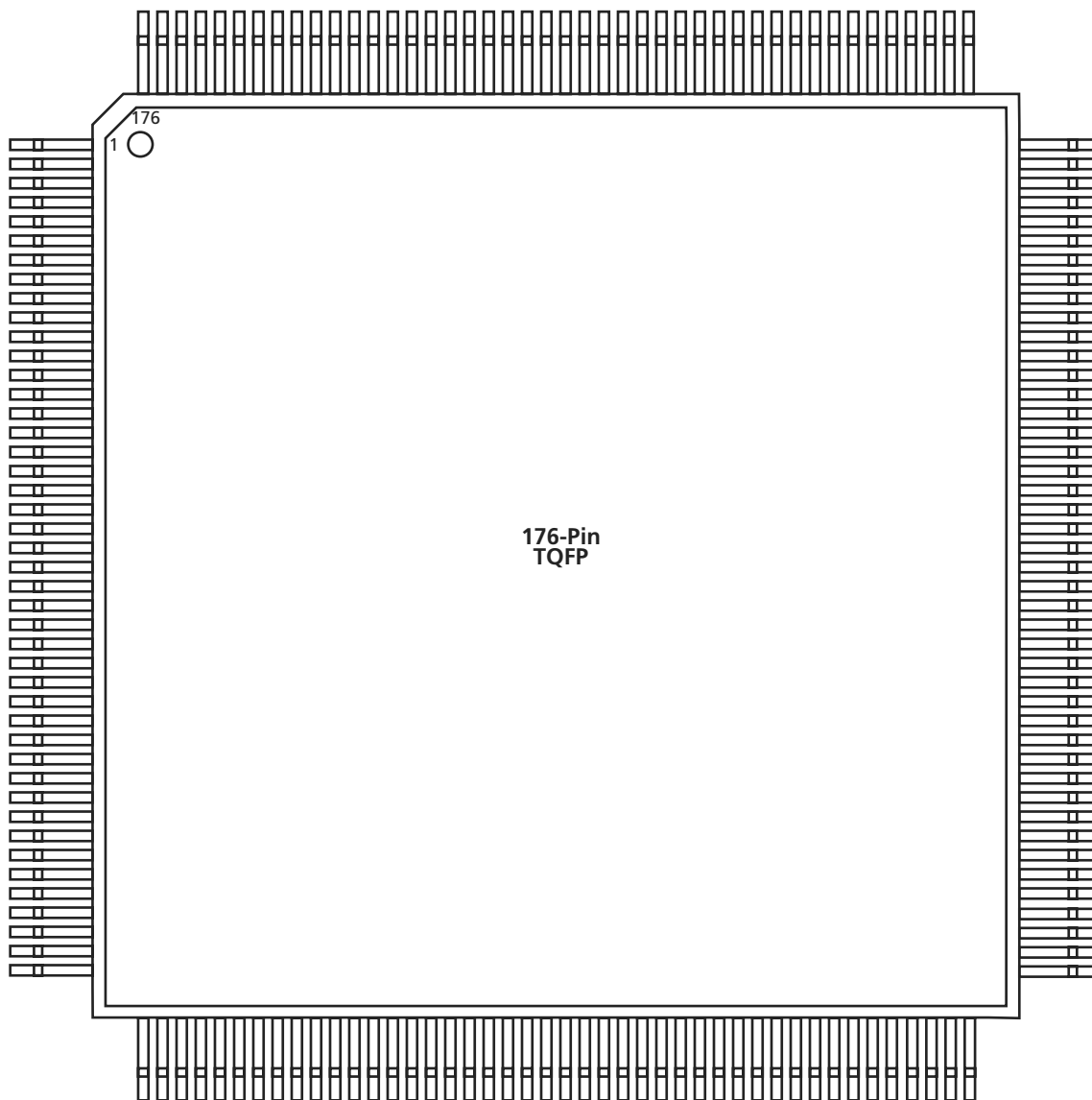


Figure 2-4 • 176-Pin TQFP (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

100-Pin VQFP		
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	TMS	TMS
8	V <sub>CCI</sub>	V <sub>CCI</sub>
9	GND	GND
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	V <sub>CCI</sub>	V <sub>CCI</sub>
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	PRB, I/O	PRB, I/O

100-Pin VQFP		
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
35	V <sub>CCA</sub>	V <sub>CCA</sub>
36	GND	GND
37	V <sub>CCR</sub>	V <sub>CCR</sub>
38	I/O	I/O
39	HCLK	HCLK
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	V <sub>CCI</sub>	V <sub>CCI</sub>
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	TDO, I/O	TDO, I/O
50	I/O	I/O
51	GND	GND
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	V <sub>CCA</sub>	V <sub>CCA</sub>
58	V <sub>CCI</sub>	V <sub>CCI</sub>
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	V <sub>CCA</sub>	V <sub>CCA</sub>
68	GND	GND

100-Pin VQFP		
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
69	GND	GND
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	V <sub>CCI</sub>	V <sub>CCI</sub>
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	CLKA	CLKA
88	CLKB	CLKB
89	V <sub>CCR</sub>	V <sub>CCR</sub>
90	V <sub>CCA</sub>	V <sub>CCA</sub>
91	GND	GND
92	PRA, I/O	PRA, I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	TCK, I/O	TCK, I/O

# 144-Pin FBGA

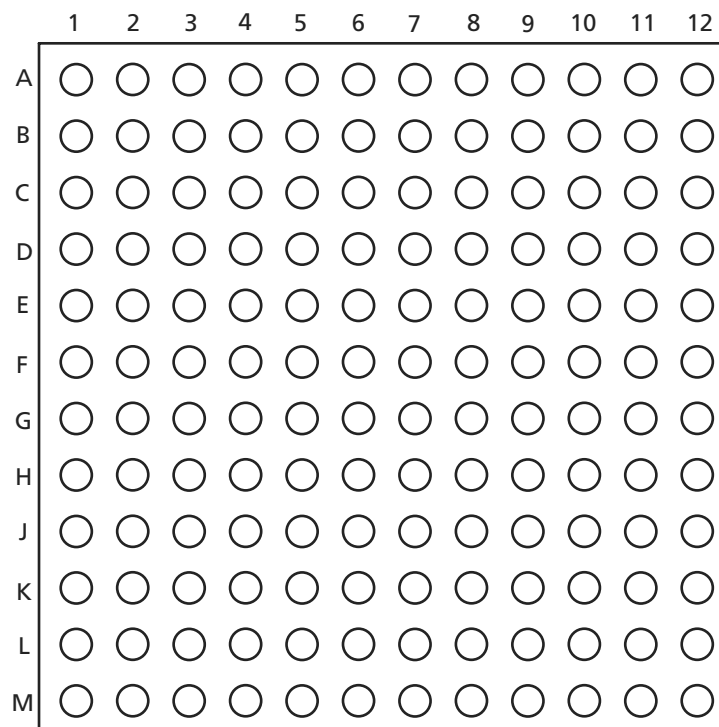


Figure 2-8 • 144-Pin FBGA (Top View)

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.