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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

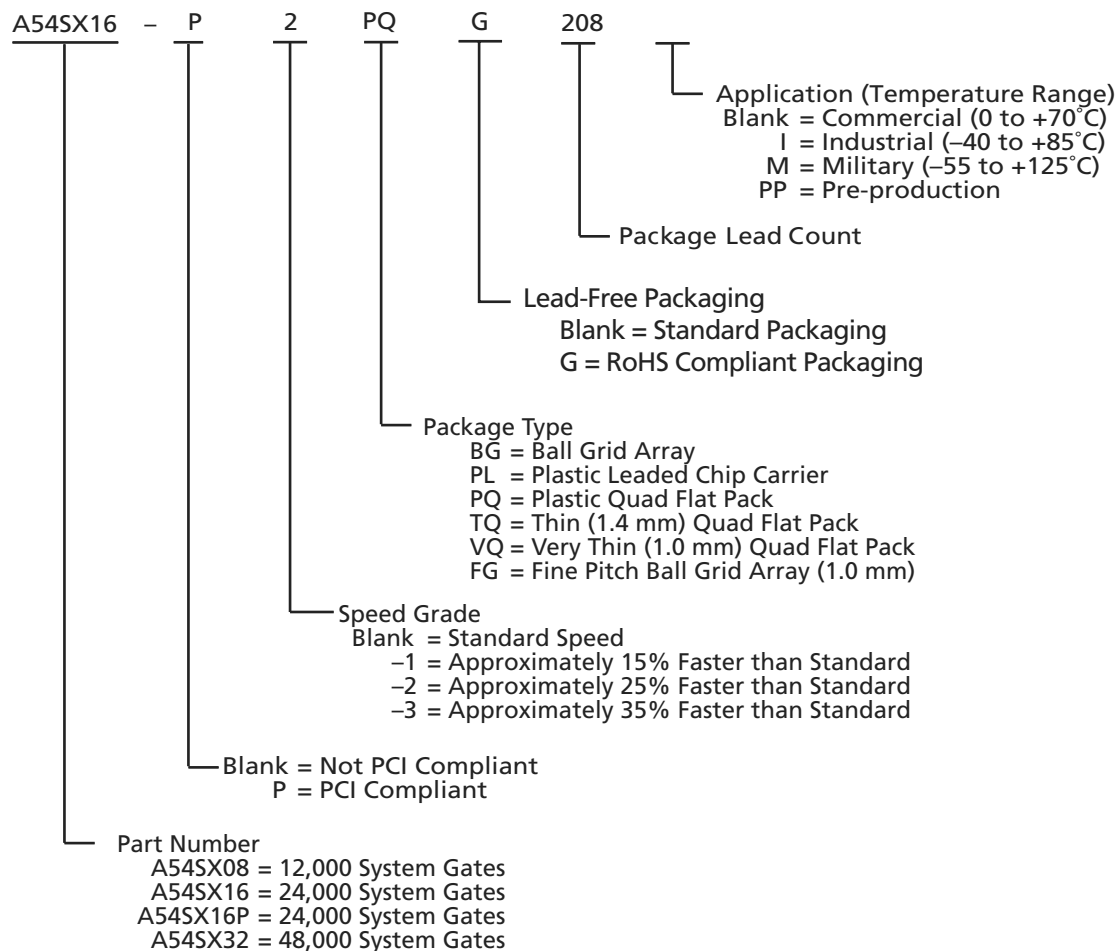
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	113
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-1tq144i

Ordering Information



Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PLCC 84-Pin	VQFP 100-Pin	PQFP 208-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 313-Pin	PBGA 329-Pin	FBGA 144-Pin
A54SX08	69	81	130	113	128	–	–	111
A54SX16	–	81	175	–	147	–	–	–
A54SX16P	–	81	175	113	147	–	–	–
A54SX32	–	–	174	113	147	249	249	–

Note: Package Definitions (Consult your local Actel sales representative for product availability):

PLCC = Plastic Leaded Chip Carrier

PQFP = Plastic Quad Flat Pack

TQFP = Thin Quad Flat Pack

VQFP = Very Thin Quad Flat Pack

PBGA = Plastic Ball Grid Array

FBGA = Fine Pitch (1.0 mm) Ball Grid Array

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

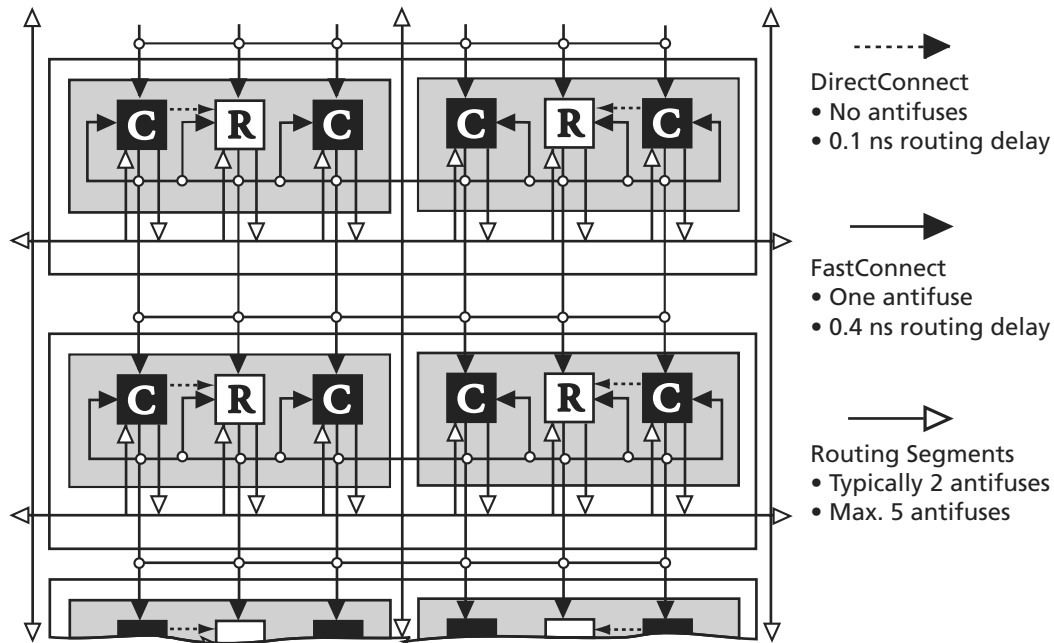


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

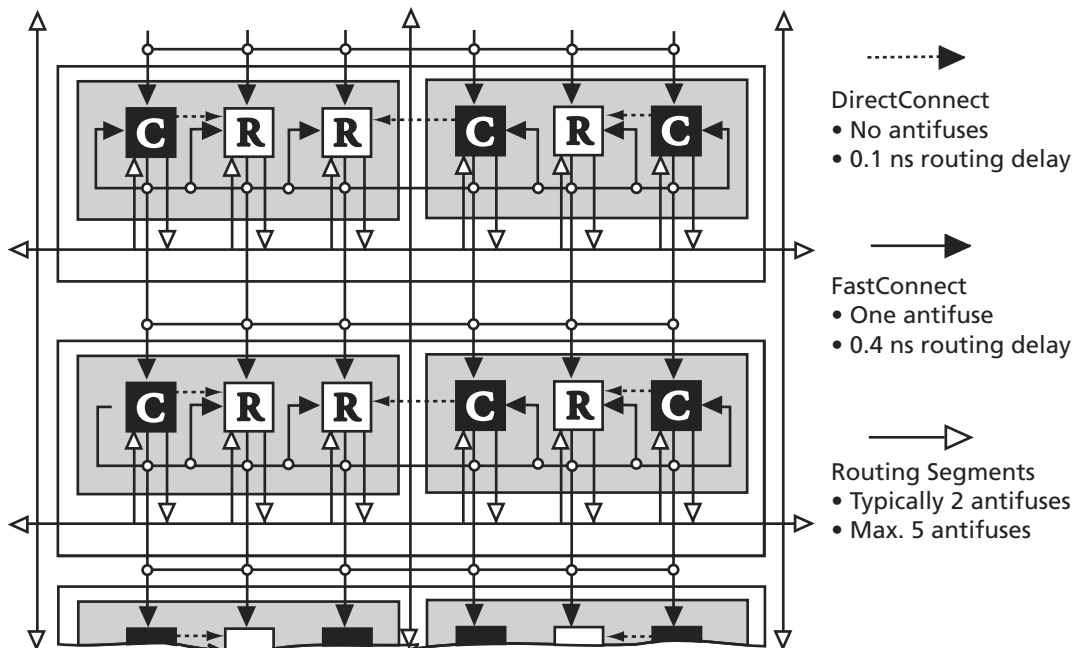


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

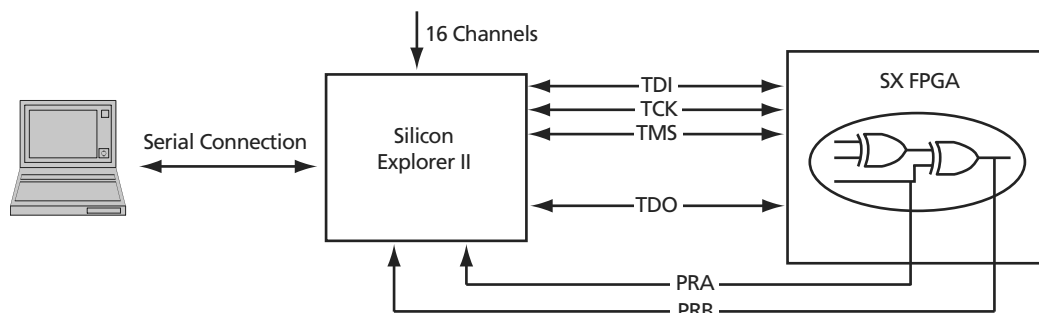


Figure 1-8 • Probe Setup

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II are compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an SX device using Silicon Sculptor II are as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming SX devices, refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

3.3 V / 5 V Operating Conditions

Table 1-3 • Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
V_{CCR}^2	DC Supply Voltage ³	-0.3 to + 6.0	V
V_{CCA}^2	DC Supply Voltage	-0.3 to + 4.0	V
V_{CCI}^2	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	-0.3 to + 4.0	V
V_{CCI}^2	DC Supply Voltage (A54SX16P)	-0.3 to + 6.0	V
V_I	Input Voltage	-0.5 to + 5.5	V
V_O	Output Voltage	-0.5 to + 3.6	V
I_{IO}	I/O Source Sink Current ³	-30 to + 5.0	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.
2. V_{CCR} in the A54SX16P must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.
3. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than $V_{CC} + 0.5$ V or less than $GND - 0.5$ V, the internal protection diodes will forward-bias and can draw excessive current.

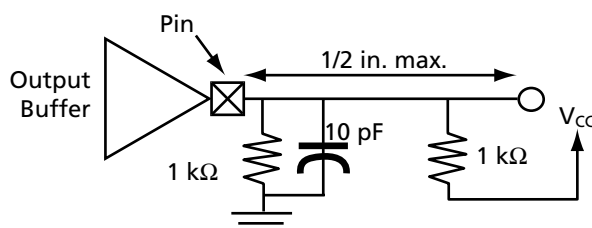
A54SX16P AC Specifications (3.3 V PCI Operation)

Table 1-9 • A54SX16P AC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CC}^1$			mA
		$0.3V_{CC} \leq V_{OUT} < 0.9V_{CC}^1$	$-12V_{CC}$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}^{1,2}$	$-17.1 + (V_{CC} - V_{OUT})$	EQ 1-3 on page 1-14	
	(Test Point)	$V_{OUT} = 0.7V_{CC}^2$		$-32V_{CC}$	mA
$I_{OL(AC)}$	Switching Current High	$V_{CC} > V_{OUT} \geq 0.6V_{CC}^1$			mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}^1$	$16V_{CC}$		mA
		$0.18V_{CC} > V_{OUT} > 0^{1,2}$	$26.7V_{OUT}$	EQ 1-4 on page 1-14	mA
	(Test Point)	$V_{OUT} = 0.18V_{CC}^2$		$38V_{CC}$	
I_{CL}	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$-3 < V_{IN} \leq -1$	$25 + (V_{IN} - V_{OUT} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate ³	0.2V _{CC} to 0.6V _{CC} load	1	4	V/ns
$slew_F$	Output Fall Slew Rate ³	0.6V _{CC} to 0.2V _{CC} load	1	4	V/ns

Notes:

1. Refer to the V/I curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.



Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}}$$

EQ 1-5

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • Standby Power

I _{CC}	V _{CC}	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

$$P_{\text{DC}} = (I_{\text{standby}}) \times V_{\text{CCA}} + (I_{\text{standby}}) \times V_{\text{CCR}} + (I_{\text{standby}}) \times V_{\text{CCI}} + xV_{\text{OL}} \times I_{\text{OL}} + y(V_{\text{CCI}} - V_{\text{OH}}) \times V_{\text{OH}}$$

EQ 1-6

AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-7

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 \times (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 \times (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 \times (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-8

Definition of Terms Used in Formula

- m = Number of logic modules switching at f_m
- n = Number of input buffers switching at f_n
- p = Number of output buffers switching at f_p
- q_1 = Number of clock loads on the first routed array clock
- q_2 = Number of clock loads on the second routed array clock
- x = Number of I/Os at logic low
- y = Number of I/Os at logic high
- r_1 = Fixed capacitance due to first routed array clock
- r_2 = Fixed capacitance due to second routed array clock
- s_1 = Number of clock loads on the dedicated array clock
- C_{EQM} = Equivalent capacitance of logic modules in pF
- C_{EQI} = Equivalent capacitance of input buffers in pF
- C_{EQO} = Equivalent capacitance of output buffers in pF
- C_{EQCR} = Equivalent capacitance of routed array clock in pF
- C_{EQHV} = Variable capacitance of dedicated array clock
- C_{EQHF} = Fixed capacitance of dedicated array clock
- C_L = Output lead capacitance in pF
- f_m = Average logic module switching rate in MHz
- f_n = Average input buffer switching rate in MHz
- f_p = Average output buffer switching rate in MHz
- f_{q1} = Average first routed array clock rate in MHz
- f_{q2} = Average second routed array clock rate in MHz
- f_{s1} = Average dedicated array clock rate in MHz

Step 1: Define Terms Used in Formula

Module	V_{CCA}	3.3
Number of logic modules switching at f_m (Used 50%)	m	264
Average logic modules switching rate f_m (MHz) (Guidelines: $f/10$)	f_m	20
Module capacitance C_{EQM} (pF)	C_{EQM}	4.0
Input Buffer		
Number of input buffers switching at f_n	n	1
Average input switching rate f_n (MHz) (Guidelines: $f/5$)	f_n	40
Input buffer capacitance C_{EQI} (pF)	C_{EQI}	3.4
Output Buffer		
Number of output buffers switching at f_p	p	1
Average output buffers switching rate f_p (MHz) (Guidelines: $f/10$)	f_p	20
Output buffers buffer capacitance C_{EQO} (pF)	C_{EQO}	4.7
Output Load capacitance C_L (pF)	C_L	35
RCLKA		
Number of Clock loads q_1	q_1	528
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q1}	200
Fixed capacitance (pF)	r_1	138
RCLKB		
Number of Clock loads q_2	q_2	0
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q2}	0
Fixed capacitance (pF)	r_2	138
HCLK		
Number of Clock loads	s_1	0
Variable capacitance of dedicated array clock (pF)	C_{EQHV}	0.61 5
Fixed capacitance of dedicated array clock (pF)	C_{EQHF}	96
Average clock rate (MHz)	f_{s1}	0

Step 2: Calculate Dynamic Power Consumption

$V_{CCA} \times V_{CCA}$	10.89
$m \times f_m \times C_{EQM}$	0.02112
$n \times f_n \times C_{EQI}$	0.000136
$p \times f_p \times (C_{EQO} + C_L)$	0.000794
$0.5 (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1})$	0.11208
$0.5 (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2})$	0
$0.5 (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1})$	0
$P_{AC} = 1.461 \text{ W}$	

Step 3: Calculate DC Power Dissipation**DC Power Dissipation**

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + X \times V_{OL} \times I_{OL} + Y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-12

For a rough estimate of DC Power Dissipation, only use $P_{DC} = (I_{standby}) \times V_{CCA}$. The rest of the formula provides a very small number that can be considered negligible.

$$P_{DC} = (I_{standby}) \times V_{CCA}$$

$$P_{DC} = .55 \text{ mA} \times 3.3 \text{ V}$$

$$P_{DC} = 0.001815 \text{ W}$$

Step 4: Calculate Total Power Consumption

$$P_{Total} = P_{AC} + P_{DC}$$

$$P_{Total} = 1.461 + 0.001815$$

$$P_{Total} = 1.4628 \text{ W}$$

Step 5: Compare Estimated Power Consumption against Characterized Power Consumption

The estimated total power consumption for this design is 1.46 W. The characterized power consumption for this design at 200 MHz is 1.0164 W.

Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.

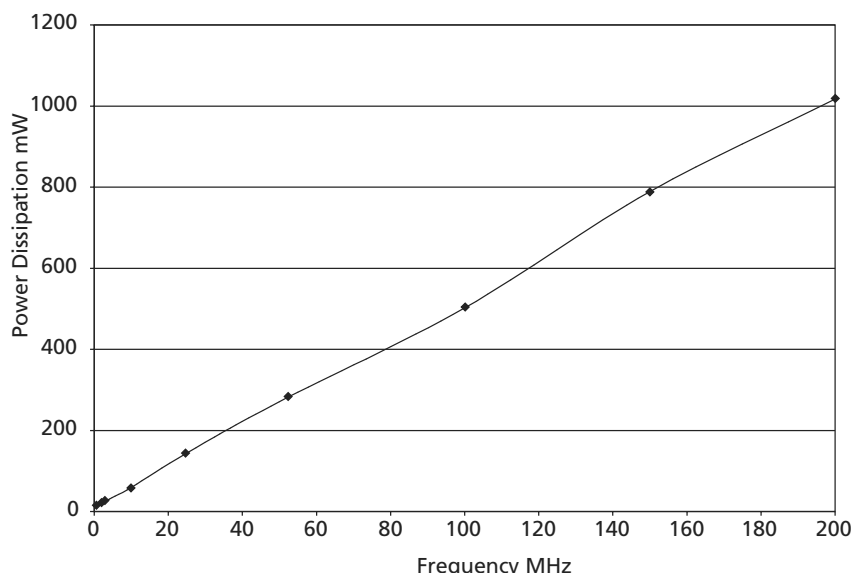


Figure 1-11 • Power Dissipation

Junction Temperature (T_j)

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a$$

EQ 1-13

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} \times P$$

P = Power calculated from Estimating Power Consumption section

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc} , and the junction to ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150 °C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ (°C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{28^\circ\text{C/W}} = 2.86 \text{ W}$$

EQ 1-14

Table 1-15 • Package Thermal Characteristics

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min.	Units
Plastic Leaded Chip Carrier (PLCC)	84	12	32	22	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Very Thin Quad Flatpack (VQFP)	100	10	38	32	°C/W
Plastic Quad Flat Pack (PQFP) without Heat Spreader	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	14.5	°C/W
Plastic Ball Grid Array (PBGA)	313	3	23	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W

Note: SX08 does not have a heat spreader.

Table 1-16 • Temperature and Voltage Derating Factors*

V_{CCA}	Junction Temperature						
	-55	-40	0	25	70	85	125
3.0	0.75	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.70	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.66	0.69	0.77	0.78	0.87	0.92	1.02

Note: *Normalized to worst-case commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 3.0\text{ V}$

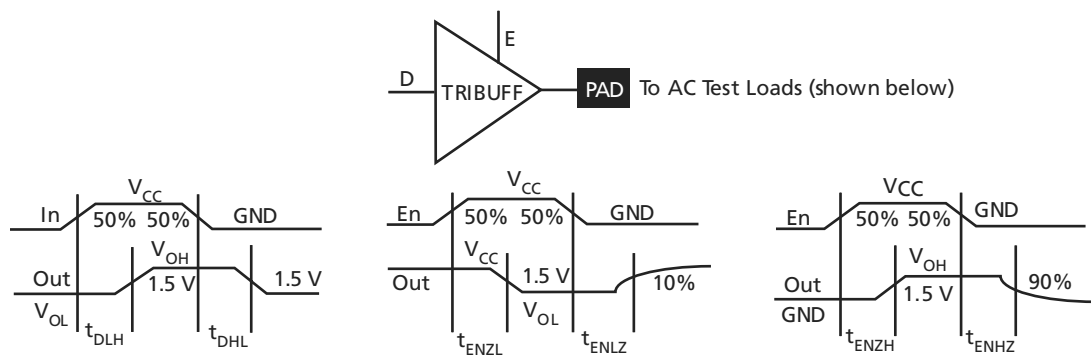


Figure 1-13 • Output Buffer Delays

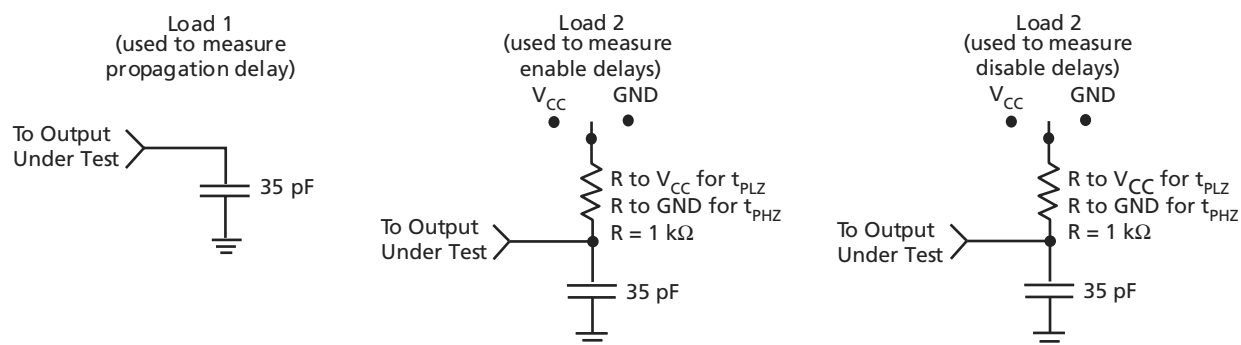


Figure 1-14 • AC Test Loads

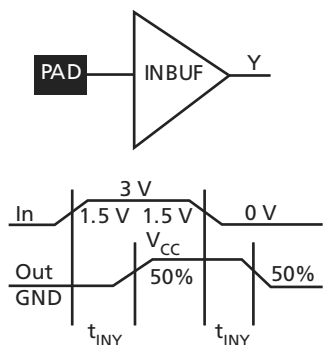


Figure 1-15 • Input Buffer Delays

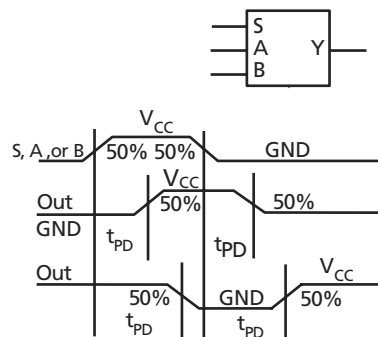


Figure 1-16 • C-Cell Delays

A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics**
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ¹										
t _{PD}	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays ²										
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{RD2}	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t _{RD3}	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t _{RD4}	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{RD8}	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t _{RD12}	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t _{RCO}	Sequential Clock-to-Q	0.8		1.1		1.2		1.4		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t _{INYH}	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t _{INYL}	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays ²										
t _{IRD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{IRD2}	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t _{IRD3}	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t _{IRD4}	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{IRD8}	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t _{IRD12}	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} , the loading is 5 pF.

208-Pin PQFP

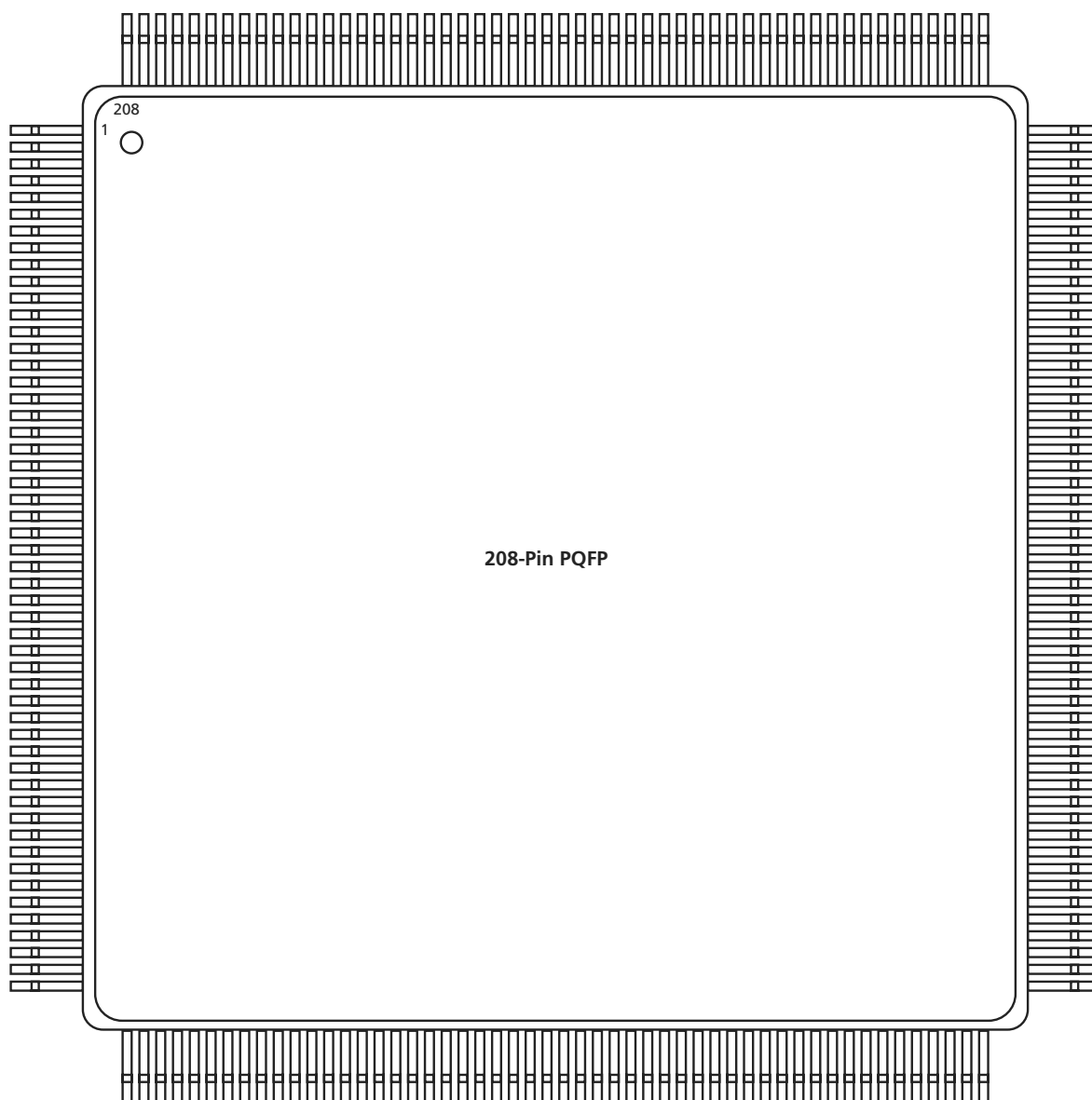


Figure 2-2 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V _{CCA}	V _{CCA}	V _{CCA}
80	V _{CCI}	V _{CCI}	V _{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V _{CCA}	V _{CCA}	V _{CCA}
90	V _{CCR}	V _{CCR}	V _{CCR}
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V _{CCI}	V _{CCI}	V _{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
109	GND	GND	GND
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V _{CCI}	V _{CCI}	V _{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	V _{CCR}	V _{CCR}	V _{CCR}
128	GND	GND	GND
129	V _{CCA}	V _{CCA}	V _{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

176-Pin TQFP

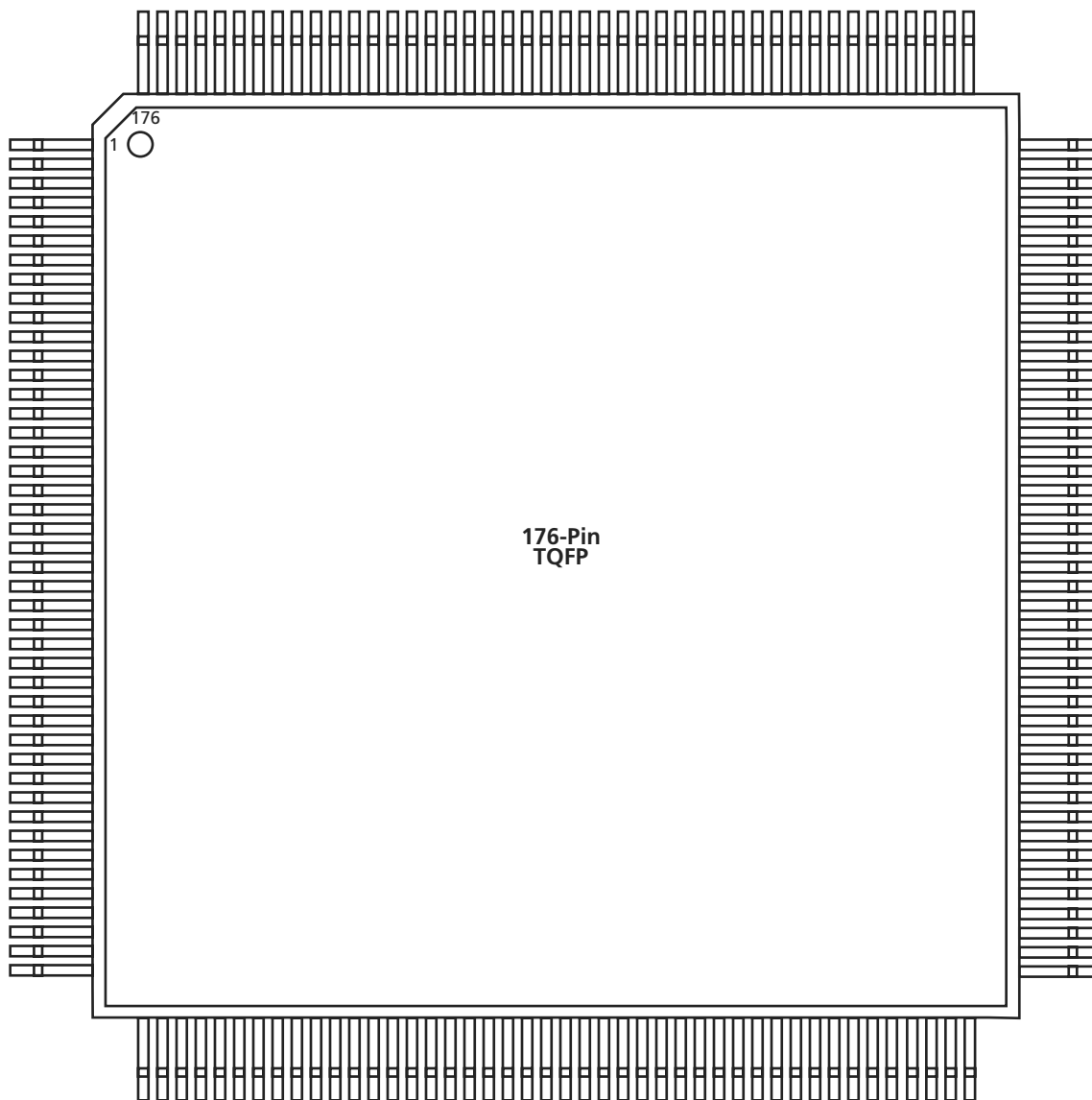


Figure 2-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V _{CCI}	V _{CCI}	V _{CCI}
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V _{CCA}	V _{CCA}	V _{CCA}
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V _{CCI}	V _{CCI}	V _{CCI}
33	V _{CCA}	V _{CCA}	V _{CCA}
34	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V _{CCI}	V _{CCI}	V _{CCI}
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V _{CCA}	V _{CCA}	V _{CCA}
67	V _{CCR}	V _{CCR}	V _{CCR}
68	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
69	HCLK	HCLK	HCLK
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	I/O	I/O	I/O
81	NC	I/O	I/O
82	V _{CCI}	V _{CCI}	V _{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	TDO, I/O	TDO, I/O	TDO, I/O
88	I/O	I/O	I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	V _{CCI}	V _{CCI}	V _{CCI}
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	GND	GND	GND
109	V _{CCA}	V _{CCA}	V _{CCA}
110	GND	GND	GND
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	I/O	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	NC	I/O	I/O
119	I/O	I/O	I/O
120	NC	I/O	I/O
121	NC	I/O	I/O
122	V _{CCA}	V _{CCA}	V _{CCA}
123	GND	GND	GND
124	V _{CCI}	V _{CCI}	V _{CCI}
125	I/O	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	NC	I/O	I/O
132	NC	I/O	I/O
133	GND	GND	GND
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O

313-Pin PBGA		313-Pin PBGA		313-Pin PBGA		313-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
A1	GND	AC5	I/O	B10	I/O	E15	I/O
A3	NC	AC7	I/O	B12	I/O	E17	I/O
A5	I/O	AC9	I/O	B14	I/O	E19	I/O
A7	I/O	AC11	I/O	B16	I/O	E21	I/O
A9	I/O	AC13	V _{CCR}	B18	I/O	E23	I/O
A11	I/O	AC15	I/O	B20	I/O	E25	I/O
A13	V _{CCR}	AC17	I/O	B22	I/O	F2	I/O
A15	I/O	AC19	I/O	B24	I/O	F4	I/O
A17	I/O	AC21	I/O	C1	TDI, I/O	F6	NC
A19	I/O	AC23	I/O	C3	I/O	F8	I/O
A21	I/O	AC25	NC	C5	NC	F10	NC
A23	NC	AD2	GND	C7	I/O	F12	I/O
A25	GND	AD4	I/O	C9	I/O	F14	I/O
AA1	I/O	AD6	V _{CCI}	C11	I/O	F16	NC
AA3	I/O	AD8	I/O	C13	V _{CCI}	F18	I/O
AA5	NC	AD10	I/O	C15	I/O	F20	I/O
AA7	I/O	AD12	PRB, I/O	C17	I/O	F22	I/O
AA9	NC	AD14	I/O	C19	V _{CCI}	F24	I/O
AA11	I/O	AD16	I/O	C21	I/O	G1	I/O
AA13	I/O	AD18	I/O	C23	I/O	G3	TMS
AA15	I/O	AD20	I/O	C25	NC	G5	I/O
AA17	I/O	AD22	NC	D2	I/O	G7	I/O
AA19	I/O	AD24	I/O	D4	NC	G9	V _{CCI}
AA21	I/O	AE1	NC	D6	I/O	G11	I/O
AA23	NC	AE3	I/O	D8	I/O	G13	CLKB
AA25	I/O	AE5	I/O	D10	I/O	G15	I/O
AB2	NC	AE7	I/O	D12	I/O	G17	I/O
AB4	NC	AE9	I/O	D14	I/O	G19	I/O
AB6	I/O	AE11	I/O	D16	I/O	G21	I/O
AB8	I/O	AE13	V _{CCA}	D18	I/O	G23	I/O
AB10	I/O	AE15	I/O	D20	I/O	G25	I/O
AB12	I/O	AE17	I/O	D22	I/O	H2	I/O
AB14	I/O	AE19	I/O	D24	NC	H4	I/O
AB16	I/O	AE21	I/O	E1	I/O	H6	I/O
AB18	V _{CCI}	AE23	TDO, I/O	E3	NC	H8	I/O
AB20	NC	AE25	GND	E5	I/O	H10	I/O
AB22	I/O	B2	TCK, I/O	E7	I/O	H12	PRA, I/O
AB24	I/O	B4	I/O	E9	I/O	H14	I/O
AC1	I/O	B6	I/O	E11	I/O	H16	I/O
AC3	I/O	B8	I/O	E13	V _{CCA}	H18	NC

313-Pin PBGA		313-Pin PBGA		313-Pin PBGA		313-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
H20	I/O	L25	I/O	R5	I/O	V10	I/O
H22	V _{CCI}	M2	I/O	R7	I/O	V12	I/O
H24	I/O	M4	I/O	R9	I/O	V14	I/O
J1	I/O	M6	I/O	R11	I/O	V16	NC
J3	I/O	M8	I/O	R13	GND	V18	I/O
J5	I/O	M10	I/O	R15	I/O	V20	I/O
J7	NC	M12	GND	R17	I/O	V22	V _{CCA}
J9	I/O	M14	GND	R19	I/O	V24	V _{CCI}
J11	I/O	M16	V _{CCI}	R21	I/O	W1	I/O
J13	CLKA	M18	I/O	R23	I/O	W3	I/O
J15	I/O	M20	I/O	R25	I/O	W5	I/O
J17	I/O	M22	I/O	T2	I/O	W7	NC
J19	I/O	M24	I/O	T4	I/O	W9	I/O
J21	GND	N1	I/O	T6	I/O	W11	I/O
J23	I/O	N3	V _{CCA}	T8	I/O	W13	V _{CCI}
J25	I/O	N5	V _{CCR}	T10	I/O	W15	I/O
K2	I/O	N7	I/O	T12	I/O	W17	I/O
K4	I/O	N9	V _{CCI}	T14	HCLK	W19	I/O
K6	I/O	N11	GND	T16	I/O	W21	I/O
K8	V _{CCI}	N13	GND	T18	I/O	W23	I/O
K10	I/O	N15	GND	T20	I/O	W25	I/O
K12	I/O	N17	I/O	T22	I/O	Y2	I/O
K14	I/O	N19	I/O	T24	I/O	Y4	I/O
K16	I/O	N21	I/O	U1	I/O	Y6	I/O
K18	I/O	N23	V _{CCR}	U3	I/O	Y8	I/O
K20	V _{CCA}	N25	V _{CCA}	U5	V _{CCI}	Y10	I/O
K22	I/O	P2	I/O	U7	I/O	Y12	I/O
K24	I/O	P4	I/O	U9	I/O	Y14	I/O
L1	I/O	P6	I/O	U11	I/O	Y16	I/O
L3	I/O	P8	I/O	U13	I/O	Y18	I/O
L5	I/O	P10	I/O	U15	I/O	Y20	NC
L7	I/O	P12	GND	U17	I/O	Y22	I/O
L9	I/O	P14	GND	U19	I/O	Y24	NC
L11	I/O	P16	I/O	U21	I/O		
L13	GND	P18	I/O	U23	I/O		
L15	I/O	P20	NC	U25	I/O		
L17	I/O	P22	I/O	V2	V _{CCA}		
L19	I/O	P24	I/O	V4	I/O		
L21	I/O	R1	I/O	V6	I/O		
L23	I/O	R3	I/O	V8	I/O		

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
A1	GND	AA13	I/O	AC2	V _{CCI}	B14	I/O
A2	GND	AA14	I/O	AC3	NC	B15	I/O
A3	V _{CCI}	AA15	I/O	AC4	I/O	B16	I/O
A4	NC	AA16	I/O	AC5	I/O	B17	I/O
A5	I/O	AA17	I/O	AC6	I/O	B18	I/O
A6	I/O	AA18	I/O	AC7	I/O	B19	I/O
A7	V _{CCI}	AA19	I/O	AC8	I/O	B20	I/O
A8	NC	AA20	TDO, I/O	AC9	V _{CCI}	B21	I/O
A9	I/O	AA21	V _{CCI}	AC10	I/O	B22	GND
A10	I/O	AA22	I/O	AC11	I/O	B23	V _{CCI}
A11	I/O	AA23	V _{CCI}	AC12	I/O	C1	NC
A12	I/O	AB1	I/O	AC13	I/O	C2	TDI, I/O
A13	CLKB	AB2	GND	AC14	I/O	C3	GND
A14	I/O	AB3	I/O	AC15	NC	C4	I/O
A15	I/O	AB4	I/O	AC16	I/O	C5	I/O
A16	I/O	AB5	I/O	AC17	I/O	C6	I/O
A17	I/O	AB6	I/O	AC18	I/O	C7	I/O
A18	I/O	AB7	I/O	AC19	I/O	C8	I/O
A19	I/O	AB8	I/O	AC20	I/O	C9	I/O
A20	I/O	AB9	I/O	AC21	NC	C10	I/O
A21	NC	AB10	I/O	AC22	V _{CCI}	C11	I/O
A22	V _{CCI}	AB11	PRB, I/O	AC23	GND	C12	I/O
A23	GND	AB12	I/O	B1	V _{CCI}	C13	I/O
AA1	V _{CCI}	AB13	HCLK	B2	GND	C14	I/O
AA2	I/O	AB14	I/O	B3	I/O	C15	I/O
AA3	GND	AB15	I/O	B4	I/O	C16	I/O
AA4	I/O	AB16	I/O	B5	I/O	C17	I/O
AA5	I/O	AB17	I/O	B6	I/O	C18	I/O
AA6	I/O	AB18	I/O	B7	I/O	C19	I/O
AA7	I/O	AB19	I/O	B8	I/O	C20	I/O
AA8	I/O	AB20	I/O	B9	I/O	C21	V _{CCI}
AA9	I/O	AB21	I/O	B10	I/O	C22	GND
AA10	I/O	AB22	GND	B11	I/O	C23	NC
AA11	I/O	AB23	I/O	B12	PRA, I/O	D1	I/O
AA12	I/O	AC1	GND	B13	CLKA	D2	I/O