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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	249
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	313-BBGA
Supplier Device Package	313-PBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a54sx32-2bg313">https://www.e-xfl.com/product-detail/microsemi/a54sx32-2bg313</a>



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# SX Family FPGAs

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## General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or “sea-of-modules”), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX’s flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

## SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

### Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

### Logic Module Design

The SX family architecture is described as a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

## Chip Architecture

The SX family chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

## Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *clusters*. There are two types of *clusters*: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (Figure 1-4). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

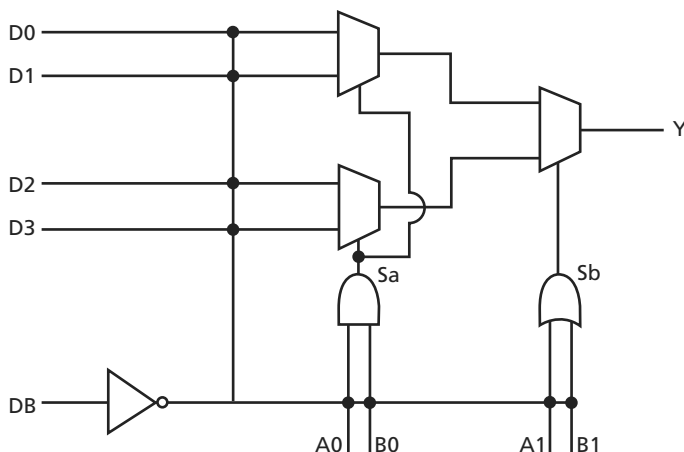


Figure 1-3 • C-Cell

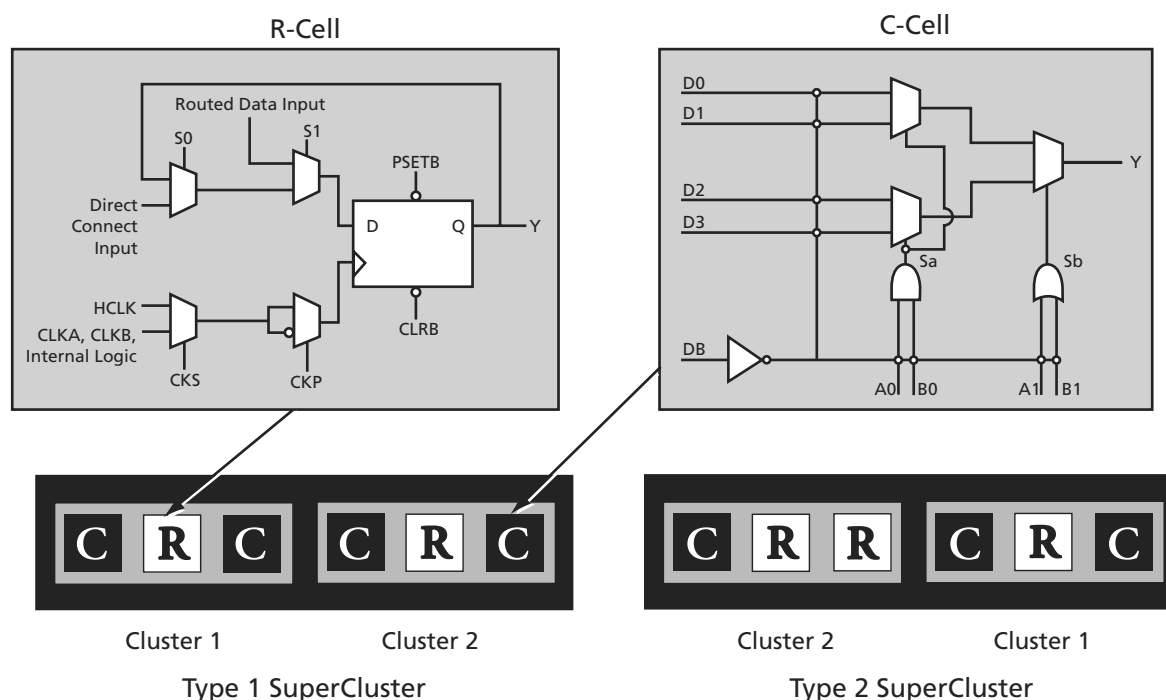


Figure 1-4 • Cluster Organization

## Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

## Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}}$$

EQ 1-5

## DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • Standby Power

I <sub>CC</sub>	V <sub>CC</sub>	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

$$P_{\text{DC}} = (I_{\text{standby}}) \times V_{\text{CCA}} + (I_{\text{standby}}) \times V_{\text{CCR}} + (I_{\text{standby}}) \times V_{\text{CCI}} + xV_{\text{OL}} \times I_{\text{OL}} + y(V_{\text{CCI}} - V_{\text{OH}}) \times V_{\text{OH}}$$

EQ 1-6

## AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-7

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 \times (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 \times (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 \times (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-8

## Definition of Terms Used in Formula

- m = Number of logic modules switching at  $f_m$
- n = Number of input buffers switching at  $f_n$
- p = Number of output buffers switching at  $f_p$
- $q_1$  = Number of clock loads on the first routed array clock
- $q_2$  = Number of clock loads on the second routed array clock
- x = Number of I/Os at logic low
- y = Number of I/Os at logic high
- $r_1$  = Fixed capacitance due to first routed array clock
- $r_2$  = Fixed capacitance due to second routed array clock
- $s_1$  = Number of clock loads on the dedicated array clock
- $C_{\text{EQM}}$  = Equivalent capacitance of logic modules in pF
- $C_{\text{EQI}}$  = Equivalent capacitance of input buffers in pF
- $C_{\text{EQO}}$  = Equivalent capacitance of output buffers in pF
- $C_{\text{EQCR}}$  = Equivalent capacitance of routed array clock in pF
- $C_{\text{EQHV}}$  = Variable capacitance of dedicated array clock
- $C_{\text{EQHF}}$  = Fixed capacitance of dedicated array clock
- $C_L$  = Output lead capacitance in pF
- $f_m$  = Average logic module switching rate in MHz
- $f_n$  = Average input buffer switching rate in MHz
- $f_p$  = Average output buffer switching rate in MHz
- $f_{q1}$  = Average first routed array clock rate in MHz
- $f_{q2}$  = Average second routed array clock rate in MHz
- $f_{s1}$  = Average dedicated array clock rate in MHz

Table 1-13 shows capacitance values for various devices.

Table 1-13 • Capacitance Values for Devices

	<b>A545X08</b>	<b>A545X16</b>	<b>A545X16P</b>	<b>A545X32</b>
$C_{EQM}$ (pF)	4.0	4.0	4.0	4.0
$C_{EQI}$ (pF)	3.4	3.4	3.4	3.4
$C_{EQO}$ (pF)	4.7	4.7	4.7	4.7
$C_{EQCR}$ (pF)	1.6	1.6	1.6	1.6
$C_{EQHV}$	0.615	0.615	0.615	0.615
$C_{EQHF}$	60	96	96	140
$r_1$ (pF)	87	138	138	171
$r_2$ (pF)	87	138	138	171

Table 1-14 • Power Consumption Guidelines

<b>Description</b>	<b>Power Consumption Guideline</b>
Logic Modules (m)	20% of modules
Inputs Switching (n)	# inputs/4
Outputs Switching (p)	# outputs/4
First Routed Array Clock Loads ( $q_1$ )	20% of register cells
Second Routed Array Clock Loads ( $q_2$ )	20% of register cells
Load Capacitance ( $C_L$ )	35 pF
Average Logic Module Switching Rate ( $f_m$ )	$f/10$
Average Input Switching Rate ( $f_n$ )	$f/5$
Average Output Switching Rate ( $f_p$ )	$f/10$
Average First Routed Array Clock Rate ( $f_{q1}$ )	$f/2$
Average Second Routed Array Clock Rate ( $f_{q2}$ )	$f/2$
Average Dedicated Array Clock Rate ( $f_{s1}$ )	$f$
Dedicated Clock Array Clock Loads ( $s_1$ )	20% of regular modules

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{\text{Total}} = P_{\text{AC}} \text{ (dynamic power)} + P_{\text{DC}} \text{ (static power)}$$

EQ 1-9

## Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

### Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A545X16P device. A pattern of 0101... was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101... caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

### AC Power Dissipation

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-10

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-11

Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.

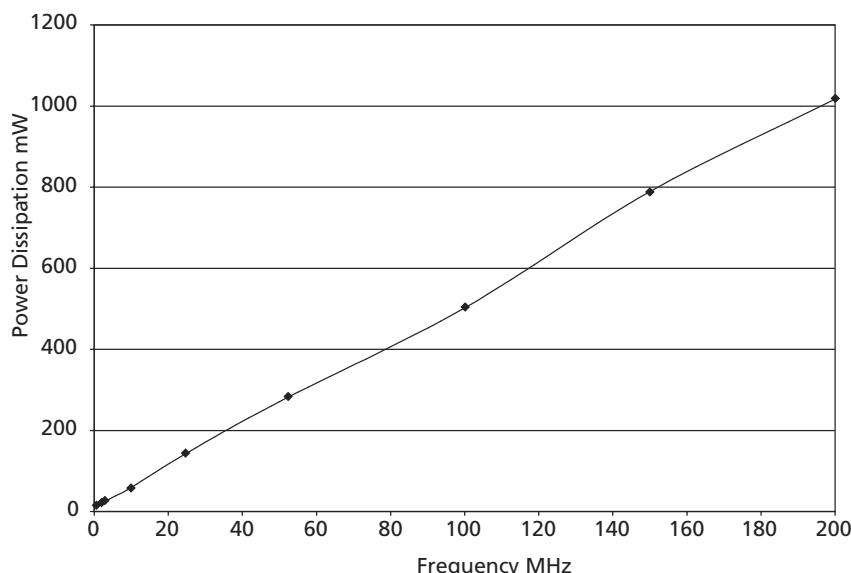


Figure 1-11 • Power Dissipation

## Junction Temperature ( $T_j$ )

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a$$

EQ 1-13

Where:

$T_a$  = Ambient Temperature

$\Delta T$  = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} \times P$$

$P$  = Power calculated from Estimating Power Consumption section

$\theta_{ja}$  = Junction to ambient of package.  $\theta_{ja}$  numbers are located in the "Package Thermal Characteristics" section.

## Package Thermal Characteristics

The device junction to case thermal characteristic is  $\theta_{jc}$ , and the junction to ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

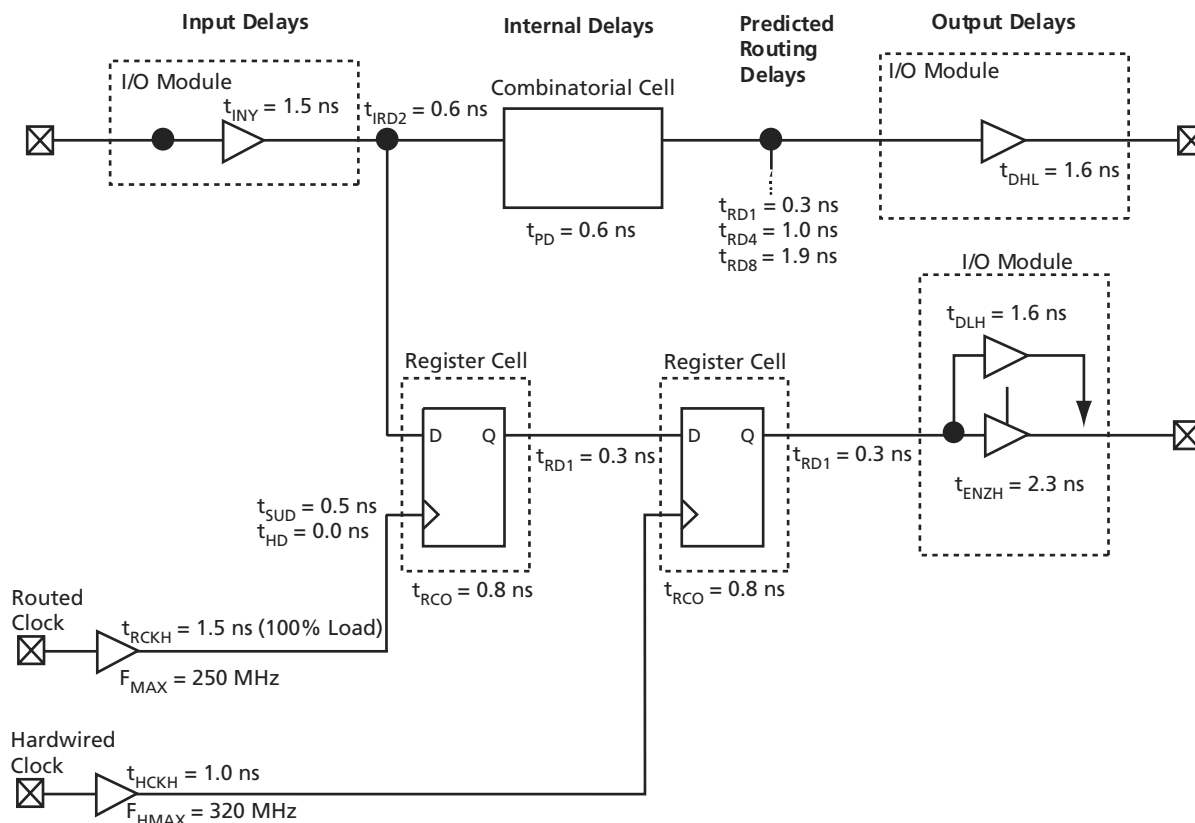
The maximum junction temperature is 150 °C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ (°C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{28^\circ\text{C/W}} = 2.86 \text{ W}$$

EQ 1-14

# SX Timing Model



**Note:** Values shown for A54SX08-3, worst-case commercial conditions.

Figure 1-12 • SX Timing Model

## Hardwired Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.0 = 1.3 \text{ ns} \end{aligned}$$

EQ 1-15

## Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.0 + 0.8 + 0.3 + 1.6 = 3.7 \text{ ns} \end{aligned}$$

EQ 1-16

## Routed Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.5 = 0.8 \text{ ns} \end{aligned}$$

EQ 1-17

## Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.52 + 0.8 + 0.3 + 1.6 = 4.2 \text{ ns} \end{aligned}$$

EQ 1-18



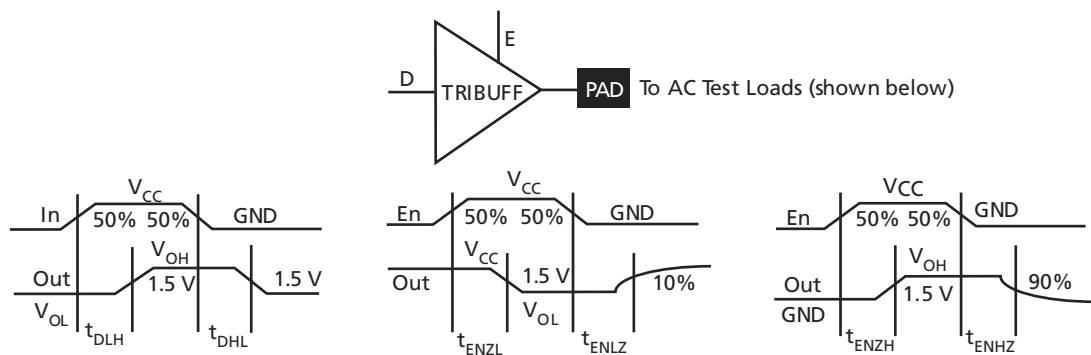


Figure 1-13 • Output Buffer Delays

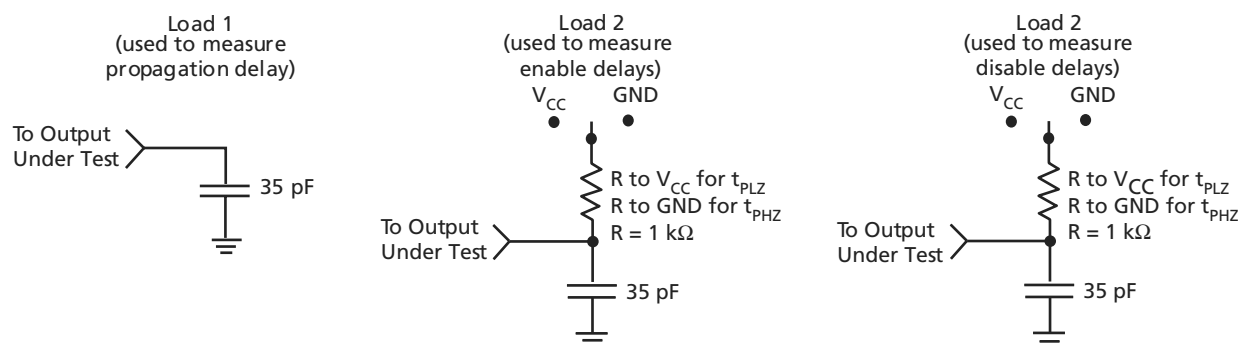


Figure 1-14 • AC Test Loads

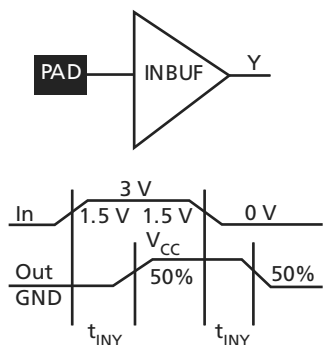


Figure 1-15 • Input Buffer Delays

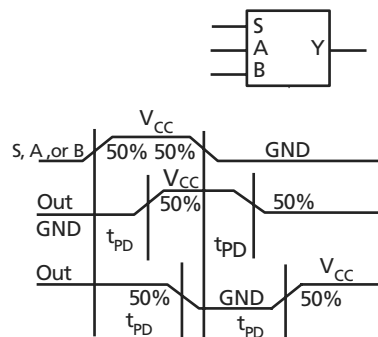


Figure 1-16 • C-Cell Delays

## A54SX16P Timing Characteristics

Table 1-19 • **A54SX16P Timing Characteristics**  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>1</sup>										
t <sub>PD</sub>	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays <sup>2</sup>										
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t <sub>RCO</sub>	Sequential Clock-to-Q	0.9		1.1		1.3		1.4		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t <sub>INYH</sub>	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t <sub>INYL</sub>	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays <sup>2</sup>										
t <sub>IRD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>IRD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

**Note:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 10 pF loading.

## A54SX32 Timing Characteristics

Table 1-20 • A54SX32 Timing Characteristics  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>1</sup>										
t <sub>PD</sub>	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays <sup>2</sup>										
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns
R-Cell Timing										
t <sub>RCO</sub>	Sequential Clock-to-Q	0.8		1.1		1.3		1.4		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t <sub>INYH</sub>	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t <sub>INYL</sub>	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays <sup>2</sup>										
t <sub>IRD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t <sub>IRD12</sub>	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns

### Note:

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except  $t_{ENZL}$  and  $t_{ENZH}$ . For  $t_{ENZL}$  and  $t_{ENZH}$  the loading is 5 pF.

# Package Pin Assignments

## 84-Pin PLCC

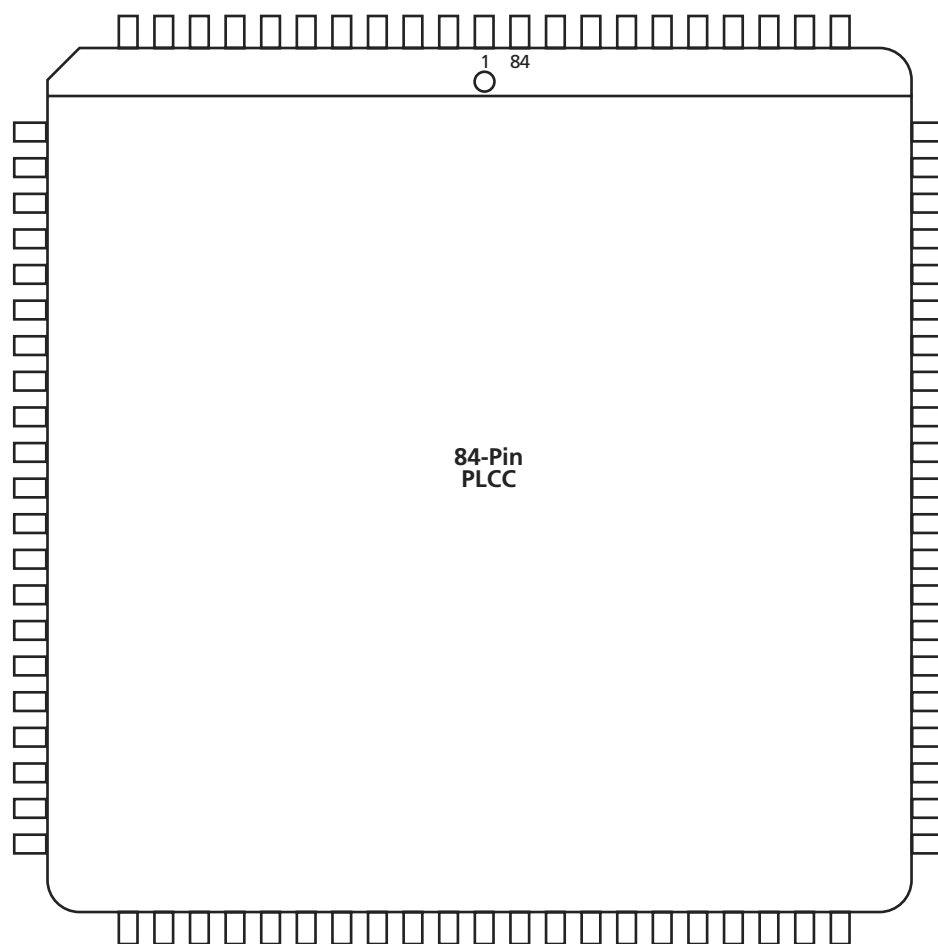


Figure 2-1 • 84-Pin PLCC (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

84-Pin PLCC	
Pin Number	A54SX08 Function
1	V <sub>CCR</sub>
2	GND
3	V <sub>CCA</sub>
4	PRA, I/O
5	I/O
6	I/O
7	V <sub>CCI</sub>
8	I/O
9	I/O
10	I/O
11	TCK, I/O
12	TDI, I/O
13	I/O
14	I/O
15	I/O
16	TMS
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V <sub>CCI</sub>
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O

84-Pin PLCC	
Pin Number	A54SX08 Function
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V <sub>CCA</sub>
42	GND
43	V <sub>CCR</sub>
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V <sub>CCA</sub>
60	V <sub>CCI</sub>
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V <sub>CCA</sub>
69	GND
70	I/O

84-Pin PLCC	
Pin Number	A54SX08 Function
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	CLKA
84	CLKB

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
145	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
146	GND	GND	GND
147	I/O	I/O	I/O
148	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	NC	I/O	I/O
156	NC	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	NC	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	NC	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	NC	I/O	I/O
177	I/O	I/O	I/O
178	I/O	I/O	I/O
179	I/O	I/O	I/O
180	CLKA	CLKA	CLKA

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
181	CLKB	CLKB	CLKB
182	V <sub>CCR</sub>	V <sub>CCR</sub>	V <sub>CCR</sub>
183	GND	GND	GND
184	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
185	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	NC	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	NC	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	NC	I/O	I/O
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	NC	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
202	NC	I/O	I/O
203	NC	I/O	I/O
204	I/O	I/O	I/O
205	NC	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O

**Note:** \* Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
33	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
34	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
67	V <sub>CCR</sub>	V <sub>CCR</sub>	V <sub>CCR</sub>
68	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
69	HCLK	HCLK	HCLK
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	I/O	I/O	I/O
81	NC	I/O	I/O
82	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	TDO, I/O	TDO, I/O	TDO, I/O
88	I/O	I/O	I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
99	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	GND	GND	GND
109	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
110	GND	GND	GND
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	I/O	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	NC	I/O	I/O
119	I/O	I/O	I/O
120	NC	I/O	I/O
121	NC	I/O	I/O
122	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
123	GND	GND	GND
124	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
125	I/O	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	NC	I/O	I/O
132	NC	I/O	I/O
133	GND	GND	GND
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O



## 313-Pin PBGA

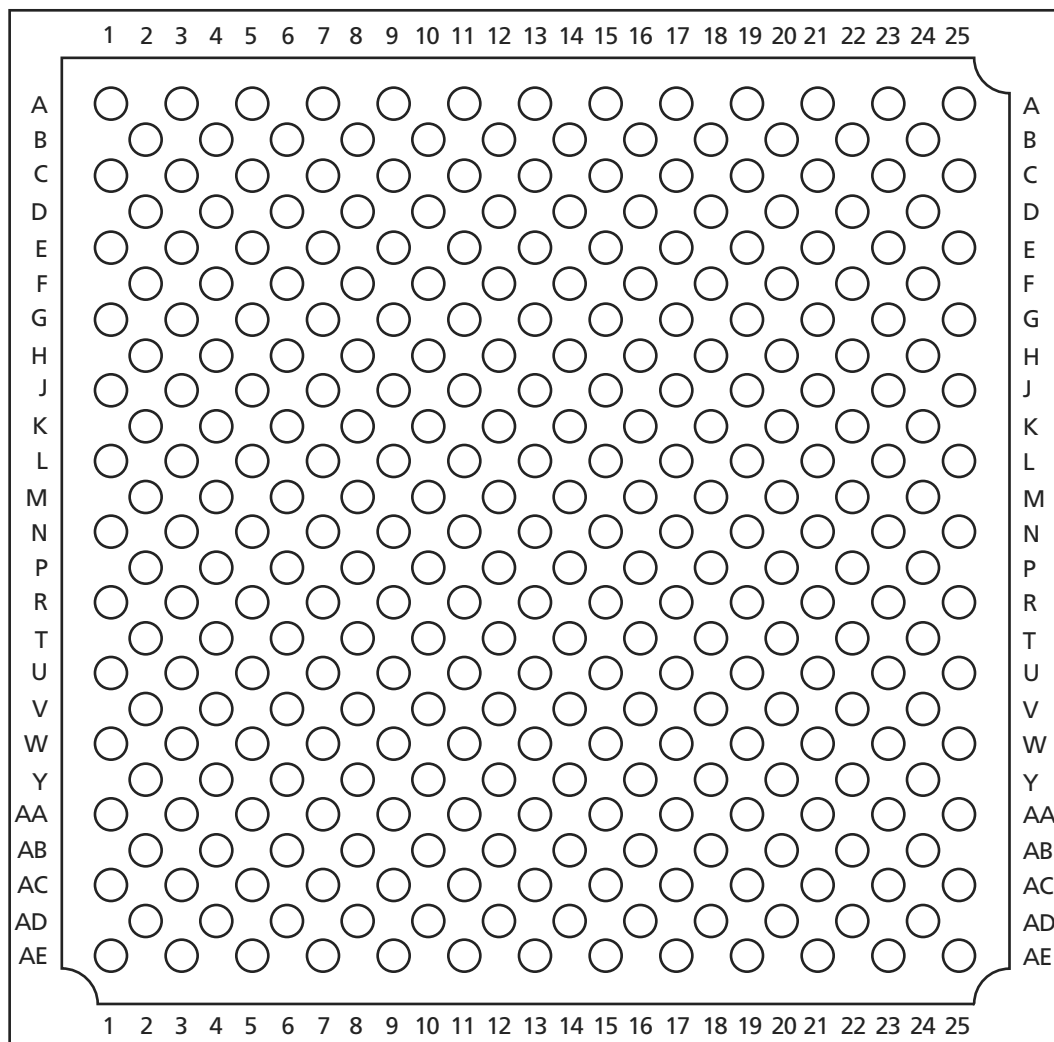


Figure 2-6 • 313-Pin PBGA (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function
D3	I/O	F22	I/O	K20	I/O	N11	GND
D4	TCK, I/O	F23	I/O	K21	I/O	N12	GND
D5	I/O	G1	I/O	K22	I/O	N13	GND
D6	I/O	G2	I/O	K23	I/O	N14	GND
D7	I/O	G3	I/O	L1	I/O	N20	NC
D8	I/O	G4	I/O	L2	I/O	N21	I/O
D9	I/O	G20	I/O	L3	I/O	N22	I/O
D10	I/O	G21	I/O	L4	V <sub>CCR</sub>	N23	I/O
D11	V <sub>CCA</sub>	G22	I/O	L10	GND	P1	I/O
D12	V <sub>CCR</sub>	G23	GND	L11	GND	P2	I/O
D13	I/O	H1	I/O	L12	GND	P3	I/O
D14	I/O	H2	I/O	L13	GND	P4	I/O
D15	I/O	H3	I/O	L14	GND	P10	GND
D16	I/O	H4	I/O	L20	V <sub>CCR</sub>	P11	GND
D17	I/O	H20	V <sub>CCA</sub>	L21	I/O	P12	GND
D18	I/O	H21	I/O	L22	I/O	P13	GND
D19	I/O	H22	I/O	L23	NC	P14	GND
D20	I/O	H23	I/O	M1	I/O	P20	I/O
D21	I/O	J1	NC	M2	I/O	P21	I/O
D22	I/O	J2	I/O	M3	I/O	P22	I/O
D23	I/O	J3	I/O	M4	V <sub>CCA</sub>	P23	I/O
E1	V <sub>CCI</sub>	J4	I/O	M10	GND	R1	I/O
E2	I/O	J20	I/O	M11	GND	R2	I/O
E3	I/O	J21	I/O	M12	GND	R3	I/O
E4	I/O	J22	I/O	M13	GND	R4	I/O
E20	I/O	J23	I/O	M14	GND	R20	I/O
E21	I/O	K1	I/O	M20	V <sub>CCA</sub>	R21	I/O
E22	I/O	K2	I/O	M21	I/O	R22	I/O
E23	I/O	K3	I/O	M22	I/O	R23	I/O
F1	I/O	K4	I/O	M23	V <sub>CCI</sub>	T1	I/O
F2	TMS	K10	GND	N1	I/O	T2	I/O
F3	I/O	K11	GND	N2	I/O	T3	I/O
F4	I/O	K12	GND	N3	I/O	T4	I/O
F20	I/O	K13	GND	N4	I/O	T20	I/O
F21	I/O	K14	GND	N10	GND	T21	I/O

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	A54SX08 Function	Pin Number	A54SX08 Function	Pin Number	A54SX08 Function	Pin Number	A54SX08 Function
A1	I/O	D1	I/O	G1	I/O	K1	I/O
A2	I/O	D2	V <sub>CCI</sub>	G2	GND	K2	I/O
A3	I/O	D3	TDI, I/O	G3	I/O	K3	I/O
A4	I/O	D4	I/O	G4	I/O	K4	I/O
A5	V <sub>CCA</sub>	D5	I/O	G5	GND	K5	I/O
A6	GND	D6	I/O	G6	GND	K6	I/O
A7	CLKA	D7	I/O	G7	GND	K7	GND
A8	I/O	D8	I/O	G8	V <sub>CCI</sub>	K8	I/O
A9	I/O	D9	I/O	G9	I/O	K9	I/O
A10	I/O	D10	I/O	G10	I/O	K10	GND
A11	I/O	D11	I/O	G11	I/O	K11	I/O
A12	I/O	D12	I/O	G12	I/O	K12	I/O
B1	I/O	E1	I/O	H1	I/O	L1	GND
B2	GND	E2	I/O	H2	I/O	L2	I/O
B3	I/O	E3	I/O	H3	I/O	L3	I/O
B4	I/O	E4	I/O	H4	I/O	L4	I/O
B5	I/O	E5	TMS	H5	V <sub>CCA</sub>	L5	I/O
B6	I/O	E6	V <sub>CCI</sub>	H6	V <sub>CCA</sub>	L6	I/O
B7	CLKB	E7	V <sub>CCI</sub>	H7	V <sub>CCI</sub>	L7	HCLK
B8	I/O	E8	V <sub>CCI</sub>	H8	V <sub>CCI</sub>	L8	I/O
B9	I/O	E9	V <sub>CCA</sub>	H9	V <sub>CCA</sub>	L9	I/O
B10	I/O	E10	I/O	H10	I/O	L10	I/O
B11	GND	E11	GND	H11	I/O	L11	I/O
B12	I/O	E12	I/O	H12	V <sub>CCR</sub>	L12	I/O
C1	I/O	F1	I/O	J1	I/O	M1	I/O
C2	I/O	F2	I/O	J2	I/O	M2	I/O
C3	TCK, I/O	F3	V <sub>CCR</sub>	J3	I/O	M3	I/O
C4	I/O	F4	I/O	J4	I/O	M4	I/O
C5	I/O	F5	GND	J5	I/O	M5	I/O
C6	PRA, I/O	F6	GND	J6	PRB, I/O	M6	I/O
C7	I/O	F7	GND	J7	I/O	M7	V <sub>CCA</sub>
C8	I/O	F8	V <sub>CCI</sub>	J8	I/O	M8	I/O
C9	I/O	F9	I/O	J9	I/O	M9	I/O
C10	I/O	F10	GND	J10	I/O	M10	I/O
C11	I/O	F11	I/O	J11	I/O	M11	TD0, I/O
C12	I/O	F12	I/O	J12	V <sub>CCA</sub>	M12	I/O

# Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v3.2)	Page
v3.1 (June 2003)	The "Ordering Information" was updated to include RoHS information.	1-ii
	The Product Plan was removed since all products have been released.	N/A
	Information concerning the TRST pin in the "Probe Circuit Control Pins" section was removed.	1-6
	The "Dedicated Test Mode" section is new.	1-6
	The "Programming" section is new.	1-7
	A note was added to the "Power-Up Sequencing" table.	1-15
	A note was added to the "Power-Down Sequencing" table. The 3.3 V comments were updated for the following devices: A545X08, A545X16, A545X32.	1-15
	U11 and U13 were added to the "313-Pin PBGA" table.	2-17
v3.0.1	Storage temperature in Table 1-3 was updated.	1-7
	Table 1-1 was updated.	1-5

## Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

### Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

### Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

### Unmarked (production)

This datasheet version contains information that is considered to be final.

### Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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