# Microchip Technology - A54SX32-BGG329I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 2880 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 249 |
| Number of Gates | 48000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 329-BBGA |
| Supplier Device Package | 329-PBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-bgg329i |

# Ordering Information

A54SX16 – P 2 PQ G 208

Application (Temperature Range)
Blank = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
PP = Pre-production

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
BG = Ball Grid Array
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flat Pack
TQ = Thin (1.4 mm) Quad Flat Pack
VQ = Very Thin (1.0 mm) Quad Flat Pack
FG = Fine Pitch Ball Grid Array (1.0 mm)

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% Faster than Standard
–2 = Approximately 25% Faster than Standard
–3 = Approximately 35% Faster than Standard

Blank = Not PCI Compliant
P = PCI Compliant

Part Number
A54SX08 = 12,000 System Gates
A54SX16 = 24,000 System Gates
A54SX16P = 24,000 System Gates
A54SX32 = 48,000 System Gates

# Plastic Device Resources

| Device | User I/Os (including clock buffers) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **PLCC 84-Pin** | **VQFP 100-Pin** | **PQFP 208-Pin** | **TQFP 144-Pin** | **TQFP 176-Pin** | **PBGA 313-Pin** | **PBGA 329-Pin** | **FBGA 144-Pin** |
| A54SX08 | 69 | 81 | 130 | 113 | 128 | – | – | 111 |
| A54SX16 | – | 81 | 175 | – | 147 | – | – | – |
| A54SX16P | – | 81 | 175 | 113 | 147 | – | – | – |
| A54SX32 | – | – | 174 | 113 | 147 | 249 | 249 | – |

**Note:** *Package Definitions (Consult your local Actel sales representative for product availability):*
*PLCC = Plastic Leaded Chip Carrier*
*PQFP = Plastic Quad Flat Pack*
*TQFP = Thin Quad Flat Pack*
*VQFP = Very Thin Quad Flat Pack*
*PBGA = Plastic Ball Grid Array*
*FBGA = Fine Pitch (1.0 mm) Ball Grid Array*

# SX Family FPGAs

## General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX's flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

## SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

### Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

### Logic Module Design

The SX family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

*Table 1-4* • **Recommended Operating Conditions**

| **Parameter** | **Commercial** | **Industrial** | **Military** | **Units** |
|---|---|---|---|---|
| Temperature Range* | 0 to + 70 | –40 to + 85 | –55 to +125 | °C |
| 3.3 V Power Supply Tolerance | ±10 | ±10 | ±10 | %$V_{CC}$ |
| 5.0 V Power Supply Tolerance | ±5 | ±10 | ±10 | %$V_{CC}$ |

***Note:*** **Ambient temperature ($T_A$) is used for commercial and industrial; case temperature ($T_C$) is used for military.*

*Table 1-5* • **Electrical Specifications**

| | | **Commercial** | | **Industrial** | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $V_{OH}$ | ($I_{OH}$ = –20 µA) (CMOS)<br>($I_{OH}$ = –8 mA) (TTL)<br>($I_{OH}$ = –6 mA) (TTL) | ($V_{CCI}$ – 0.1)<br>2.4 | $V_{CCI}$<br>$V_{CCI}$ | ($V_{CCI}$ – 0.1)<br><br>2.4 | $V_{CCI}$<br><br>$V_{CCI}$ | V |
| $V_{OL}$ | ($I_{OL}$= 20 µA) (CMOS)<br>($I_{OL}$ = 12 mA) (TTL)<br>($I_{OL}$ = 8 mA) (TTL) | | 0.10<br>0.50 | | <br><br>0.50 | V |
| $V_{IL}$ | | | 0.8 | | 0.8 | V |
| $V_{IH}$ | | 2.0 | | 2.0 | | V |
| $t_R$, $t_F$ | Input Transition Time $t_R$, $t_F$ | | 50 | | 50 | ns |
| $C_{IO}$ | $C_{IO}$ I/O Capacitance | | 10 | | 10 | pF |
| $I_{CC}$ | Standby Current, $I_{CC}$ | | 4.0 | | 4.0 | mA |
| $I_{CC(D)}$ | $I_{CC(D)}$ $I_{Dynamic}$ $V_{CC}$ Supply Current | See "Evaluating Power in SX Devices" on page 1-16. | | | | |

# PCI Compliance for the SX Family

The SX family supports 3.3 V and 5.0 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

*Table 1-6* • **A54SX16P DC Specifications (5.0 V PCI Operation)**

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply Voltage for Array | | 3.0 | 3.6 | V |
| $V_{CCR}$ | Supply Voltage required for Internal Biasing | | 4.75 | 5.25 | V |
| $V_{CCI}$ | Supply Voltage for I/Os | | 4.75 | 5.25 | V |
| $V_{IH}$ | Input High Voltage[1] | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input Low Voltage[1] | | –0.5 | 0.8 | V |
| $I_{IH}$ | Input High Leakage Current | $V_{IN}$ = 2.7 | | 70 | µA |
| $I_{IL}$ | Input Low Leakage Current | $V_{IN}$ = 0.5 | | –70 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = –2 mA | 2.4 | | V |
| $V_{OL}$ | Output Low Voltage[2] | $I_{OUT}$ = 3 mA, 6 mA | | 0.55 | V |
| $C_{IN}$ | Input Pin Capacitance[3] | | | 10 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 5 | 12 | pF |
| $C_{IDSEL}$ | IDSEL Pin Capacitance[4] | | | 8 | pF |

***Notes:***

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used, AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*
4. *Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].*

# Power-Up Sequencing

*Table 1-10* • **Power-Up Sequencing**

| $V_{CCA}$ | $V_{CCR}$ | $V_{CCI}$ | Power-Up Sequence | Comments |
|---|---|---|---|---|
| **A54SX08, A54SX16, A54SX32** | | | | |
| 3.3 V | 5.0 V | 3.3 V | 5.0 V First<br>3.3 V Second | No possible damage to device |
| | | | 3.3 V First<br>5.0 V Second | Possible damage to device |
| **A54SX16P** | | | | |
| 3.3 V | 3.3 V | 3.3 V | 3.3 V Only | No possible damage to device |
| 3.3 V | 5.0 V | 3.3 V | 5.0 V First<br>3.3 V Second | No possible damage to device |
| | | | 3.3 V First<br>5.0 V Second | Possible damage to device |
| 3.3 V | 5.0 V | 5.0 V | 5.0 V First<br>3.3 V Second | No possible damage to device |
| | | | 3.3 V First<br>5.0 V Second | No possible damage to device |

***Note:*** *No inputs should be driven (high or low) before completion of power-up.*

# Power-Down Sequencing

*Table 1-11* • **Power-Down Sequencing**

| $V_{CCA}$ | $V_{CCR}$ | $V_{CCI}$ | Power-Down Sequence | Comments |
|---|---|---|---|---|
| **A54SX08, A54SX16, A54SX32** | | | | |
| 3.3 V | 5.0 V | 3.3 V | 5.0 V First<br>3.3 V Second | Possible damage to device |
| | | | 3.3 V First<br>5.0 V Second | No possible damage to device |
| **A54SX16P** | | | | |
| 3.3 V | 3.3 V | 3.3 V | 3.3 V Only | No possible damage to device |
| 3.3 V | 5.0 V | 3.3 V | 5.0 V First<br>3.3 V Second | Possible damage to device |
| | | | 3.3 V First<br>5.0 V Second | No possible damage to device |
| 3.3 V | 5.0 V | 5.0 V | 5.0 V First<br>3.3 V Second | No possible damage to device |
| | | | 3.3 V First<br>5.0 V Second | No possible damage to device |

***Note:*** *No inputs should be driven (high or low) after the beginning of the power-down sequence.*

# Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device’s maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

## Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{Total} = P_{DC} + P_{AC}$$

*EQ 1-5*

## DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

*Table 1-12* • **Standby Power**

| $I_{CC}$ | $V_{CC}$ | Power |
|---|---|---|
| 4 mA | 3.6 V | 14.4 mW |

The DC power dissipation is defined in EQ 1-6.

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + xV_{OL} \times I_{OL} + y(V_{CCI} - V_{OH}) \times V_{OH}$$

*EQ 1-6*

## AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

*EQ 1-7*

$$\begin{aligned}P_{AC} = V_{CCA}^2 \times [&(m \times C_{EQM} \times f_m)_{Module} + \\ &(n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + \\ &(0.5 \times (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + \\ &(0.5 \times (q2 \times CEQCR \times f_{q2}) + (r2 \times f_{q2}))RCLKB + \\ &(0.5 \times (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]\end{aligned}$$

*EQ 1-8*

### Definition of Terms Used in Formula

$m$ = Number of logic modules switching at $f_m$
$n$ = Number of input buffers switching at $f_n$
$p$ = Number of output buffers switching at $f_p$
$q_1$ = Number of clock loads on the first routed array clock
$q_2$ = Number of clock loads on the second routed array clock
$x$ = Number of I/Os at logic low
$y$ = Number of I/Os at logic high
$r_1$ = Fixed capacitance due to first routed array clock
$r_2$ = Fixed capacitance due to second routed array clock
$s_1$ = Number of clock loads on the dedicated array clock
$C_{EQM}$ = Equivalent capacitance of logic modules in pF
$C_{EQI}$ = Equivalent capacitance of input buffers in pF
$C_{EQO}$ = Equivalent capacitance of output buffers in pF
$C_{EQCR}$ = Equivalent capacitance of routed array clock in pF
$C_{EQHV}$ = Variable capacitance of dedicated array clock
$C_{EQHF}$ = Fixed capacitance of dedicated array clock
$C_L$ = Output lead capacitance in pF
$f_m$ = Average logic module switching rate in MHz
$f_n$ = Average input buffer switching rate in MHz
$f_p$ = Average output buffer switching rate in MHz
$f_{q1}$ = Average first routed array clock rate in MHz
$f_{q2}$ = Average second routed array clock rate in MHz
$f_{s1}$ = Average dedicated array clock rate in MHz

Table 1-13 shows capacitance values for various devices.

*Table 1-13* • **Capacitance Values for Devices**

| | A54SX08 | A54SX16 | A54SX16P | A54SX32 |
|---|---|---|---|---|
| $C_{EQM}$ (pF) | 4.0 | 4.0 | 4.0 | 4.0 |
| $C_{EQI}$ (pF) | 3.4 | 3.4 | 3.4 | 3.4 |
| $C_{EQO}$ (pF) | 4.7 | 4.7 | 4.7 | 4.7 |
| $C_{EQCR}$ (pF) | 1.6 | 1.6 | 1.6 | 1.6 |
| $C_{EQHV}$ | 0.615 | 0.615 | 0.615 | 0.615 |
| $C_{EQHF}$ | 60 | 96 | 96 | 140 |
| $r_1$ (pF) | 87 | 138 | 138 | 171 |
| $r_2$ (pF) | 87 | 138 | 138 | 171 |

## Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

## Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A54SX16P device. A pattern of 0101… was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101… caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

*Table 1-14* • **Power Consumption Guidelines**

| Description | Power Consumption Guideline |
|---|---|
| Logic Modules (m) | 20% of modules |
| Inputs Switching (n) | # inputs/4 |
| Outputs Switching (p) | # outputs/4 |
| First Routed Array Clock Loads ($q_1$) | 20% of register cells |
| Second Routed Array Clock Loads ($q_2$) | 20% of register cells |
| Load Capacitance ($C_L$) | 35 pF |
| Average Logic Module Switching Rate ($f_m$) | f/10 |
| Average Input Switching Rate ($f_n$) | f/5 |
| Average Output Switching Rate ($f_p$) | f/10 |
| Average First Routed Array Clock Rate ($f_{q1}$) | f/2 |
| Average Second Routed Array Clock Rate ($f_{q2}$) | f/2 |
| Average Dedicated Array Clock Rate ($f_{s1}$) | f |
| Dedicated Clock Array Clock Loads ($s_1$) | 20% of regular modules |

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{Total} = P_{AC} \text{ (dynamic power)} + P_{DC} \text{ (static power)} \qquad \text{EQ 1-9}$$

## AC Power Dissipation

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer} \qquad \text{EQ 1-10}$$

$$\begin{aligned} P_{AC} = {} & V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + \\ & (n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + \\ & (0.5\ (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + \\ & (0.5\ (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2}))_{RCLKB} + \\ & (0.5\ (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}] \end{aligned} \qquad \text{EQ 1-11}$$

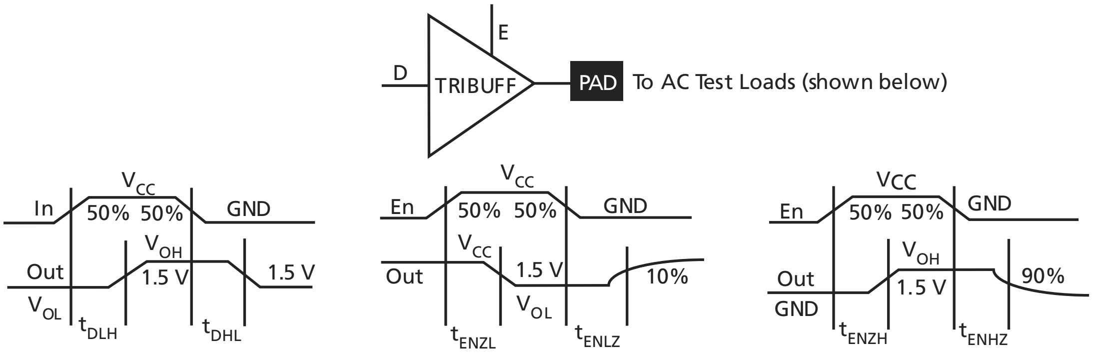

*Figure 1-13* • **Output Buffer Delays**

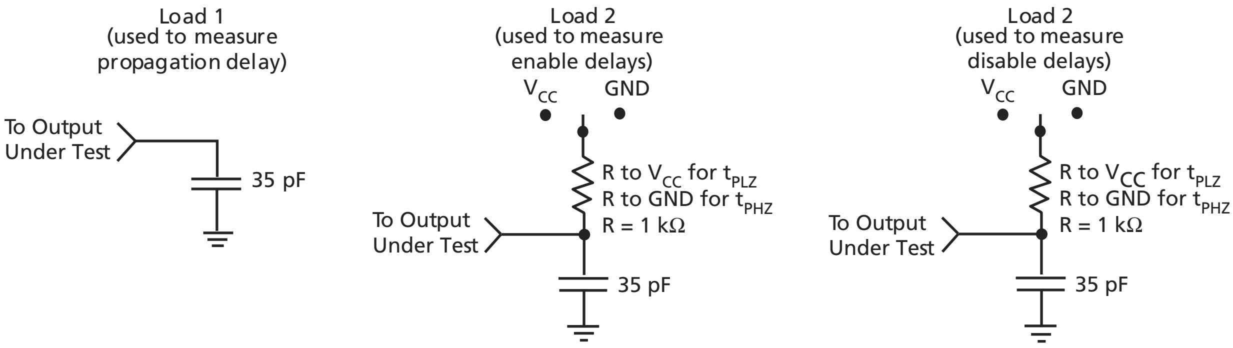

*Figure 1-14* • **AC Test Loads**

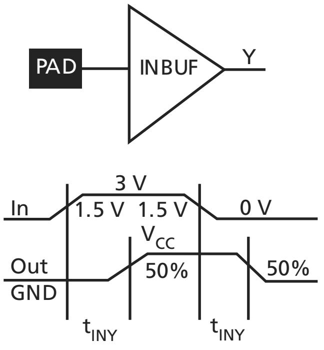

*Figure 1-15* • **Input Buffer Delays**

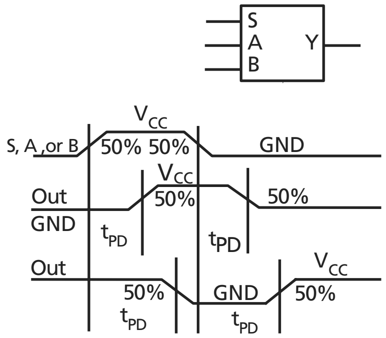

*Figure 1-16* • **C-Cell Delays**

Table 1-19 • **A54SX16P Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCR}$ = 4.75 V, $V_{CCA}$,$V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| | | '–3' Speed | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **TTL/PCI Output Module Timing** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 1.5 | | 1.7 | | 2.0 | | 2.3 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 1.9 | | 2.2 | | 2.4 | | 2.9 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.3 | | 2.6 | | 3.0 | | 3.5 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 1.5 | | 1.7 | | 1.9 | | 2.3 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.7 | | 3.1 | | 3.5 | | 4.1 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | ns |
| **PCI Output Module Timing**[3] | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 1.8 | | 2.0 | | 2.3 | | 2.7 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 1.7 | | 2.0 | | 2.2 | | 2.6 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 0.8 | | 1.0 | | 1.1 | | 1.3 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 1.2 | | 1.2 | | 1.5 | | 1.8 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 1.0 | | 1.1 | | 1.3 | | 1.5 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 1.1 | | 1.3 | | 1.5 | | 1.7 | ns |
| **TTL Output Module Timing** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 2.1 | | 2.5 | | 2.8 | | 3.3 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 2.0 | | 2.3 | | 2.6 | | 3.1 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.5 | | 2.9 | | 3.2 | | 3.8 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.0 | | 3.5 | | 3.9 | | 4.6 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.3 | | 2.7 | | 3.1 | | 3.6 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | ns |

***Note:***

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 10 pF loading.*

## Pin Description

**CLKA/B** **Clock A and B**

These pins are 3.3 V / 5.0 V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as bidirectional.)

**GND** **Ground**

LOW supply voltage.

**HCLK** **Dedicated (hardwired) Array Clock**

This pin is the 3.3 V / 5.0 V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

**I/O** **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3 V PCI or 5.0 V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

**NC** **No Connection**

This pin is not connected to circuitry within the device.

**PRA, I/O** **Probe A**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality.

**PRB, I/O** **Probe B**

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality.

**TCK** **Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDI** **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDO** **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the “logic reset” state.

**TMS** **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-2 on page 1-6). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

**$V_{CCI}$** **Supply Voltage**

Supply voltage for I/Os. See Table 1-1 on page 1-5.

**$V_{CCA}$** **Supply Voltage**

Supply voltage for Array. See Table 1-1 on page 1-5.

**$V_{CCR}$** **Supply Voltage**

Supply voltage for input tolerance (required for internal biasing). See Table 1-1 on page 1-5.

# Package Pin Assignments

## 84-Pin PLCC

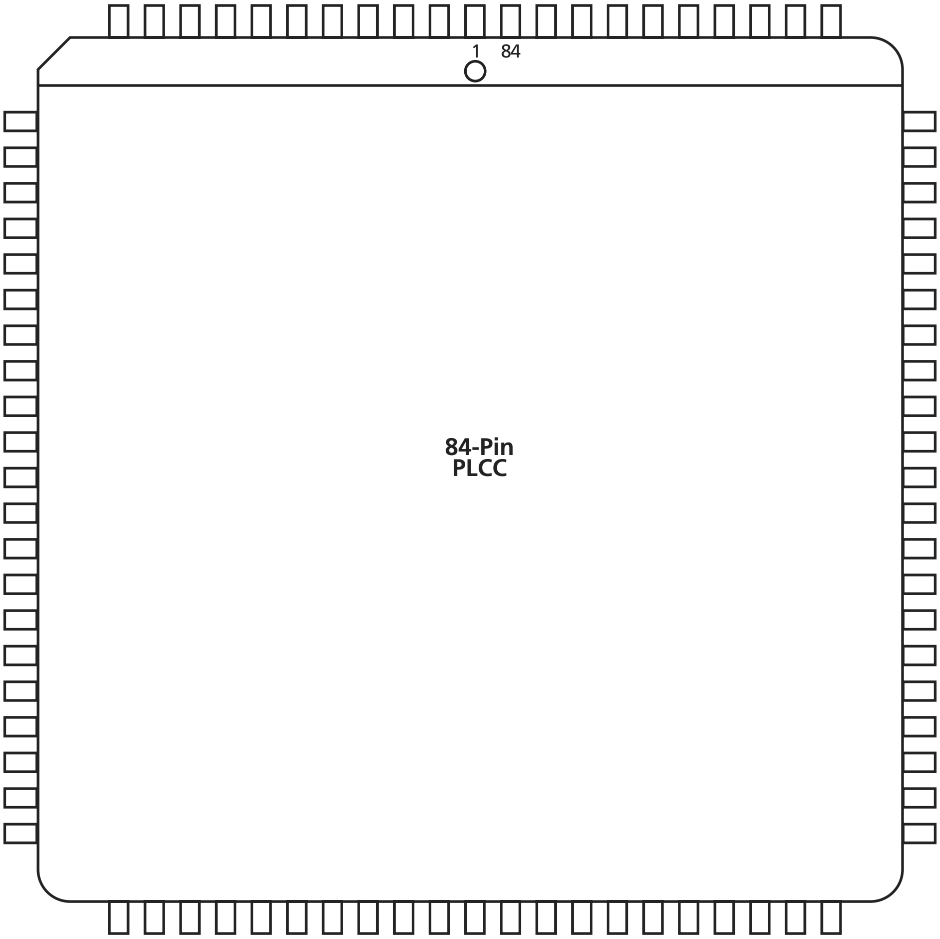

*Figure 2-1* • **84-Pin PLCC (Top View)**

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 84-Pin PLCC | |
|---|---|
| Pin Number | A54SX08 Function |
| 1 | $V_{CCR}$ |
| 2 | GND |
| 3 | $V_{CCA}$ |
| 4 | PRA, I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | $V_{CCI}$ |
| 8 | I/O |
| 9 | I/O |
| 10 | I/O |
| 11 | TCK, I/O |
| 12 | TDI, I/O |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | TMS |
| 17 | I/O |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | I/O |
| 22 | I/O |
| 23 | I/O |
| 24 | I/O |
| 25 | I/O |
| 26 | I/O |
| 27 | GND |
| 28 | $V_{CCI}$ |
| 29 | I/O |
| 30 | I/O |
| 31 | I/O |
| 32 | I/O |
| 33 | I/O |
| 34 | I/O |
| 35 | I/O |
| 36 | I/O |
| 37 | I/O |
| 38 | I/O |
| 39 | I/O |
| 40 | PRB, I/O |
| 41 | $V_{CCA}$ |
| 42 | GND |
| 43 | $V_{CCR}$ |
| 44 | I/O |
| 45 | HCLK |
| 46 | I/O |
| 47 | I/O |
| 48 | I/O |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | TDO, I/O |
| 53 | I/O |
| 54 | I/O |
| 55 | I/O |
| 56 | I/O |
| 57 | I/O |
| 58 | I/O |
| 59 | $V_{CCA}$ |
| 60 | $V_{CCI}$ |
| 61 | GND |
| 62 | I/O |
| 63 | I/O |
| 64 | I/O |
| 65 | I/O |
| 66 | I/O |
| 67 | I/O |
| 68 | $V_{CCA}$ |
| 69 | GND |
| 70 | I/O |
| 71 | I/O |
| 72 | I/O |
| 73 | I/O |
| 74 | I/O |
| 75 | I/O |
| 76 | I/O |
| 77 | I/O |
| 78 | I/O |
| 79 | I/O |
| 80 | I/O |
| 81 | I/O |
| 82 | I/O |
| 83 | CLKA |
| 84 | CLKB |

| 208-Pin PQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 145 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 146 | GND | GND | GND |
| 147 | I/O | I/O | I/O |
| 148 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 149 | I/O | I/O | I/O |
| 150 | I/O | I/O | I/O |
| 151 | I/O | I/O | I/O |
| 152 | I/O | I/O | I/O |
| 153 | I/O | I/O | I/O |
| 154 | I/O | I/O | I/O |
| 155 | NC | I/O | I/O |
| 156 | NC | I/O | I/O |
| 157 | GND | GND | GND |
| 158 | I/O | I/O | I/O |
| 159 | I/O | I/O | I/O |
| 160 | I/O | I/O | I/O |
| 161 | I/O | I/O | I/O |
| 162 | I/O | I/O | I/O |
| 163 | I/O | I/O | I/O |
| 164 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 165 | I/O | I/O | I/O |
| 166 | I/O | I/O | I/O |
| 167 | NC | I/O | I/O |
| 168 | I/O | I/O | I/O |
| 169 | I/O | I/O | I/O |
| 170 | NC | I/O | I/O |
| 171 | I/O | I/O | I/O |
| 172 | I/O | I/O | I/O |
| 173 | NC | I/O | I/O |
| 174 | I/O | I/O | I/O |
| 175 | I/O | I/O | I/O |
| 176 | NC | I/O | I/O |
| 177 | I/O | I/O | I/O |
| 178 | I/O | I/O | I/O |
| 179 | I/O | I/O | I/O |
| 180 | CLKA | CLKA | CLKA |

| 208-Pin PQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 181 | CLKB | CLKB | CLKB |
| 182 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 183 | GND | GND | GND |
| 184 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 185 | GND | GND | GND |
| 186 | PRA, I/O | PRA, I/O | PRA, I/O |
| 187 | I/O | I/O | I/O |
| 188 | I/O | I/O | I/O |
| 189 | NC | I/O | I/O |
| 190 | I/O | I/O | I/O |
| 191 | I/O | I/O | I/O |
| 192 | NC | I/O | I/O |
| 193 | I/O | I/O | I/O |
| 194 | I/O | I/O | I/O |
| 195 | NC | I/O | I/O |
| 196 | I/O | I/O | I/O |
| 197 | I/O | I/O | I/O |
| 198 | NC | I/O | I/O |
| 199 | I/O | I/O | I/O |
| 200 | I/O | I/O | I/O |
| 201 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 202 | NC | I/O | I/O |
| 203 | NC | I/O | I/O |
| 204 | I/O | I/O | I/O |
| 205 | NC | I/O | I/O |
| 206 | I/O | I/O | I/O |
| 207 | I/O | I/O | I/O |
| 208 | TCK, I/O | TCK, I/O | TCK, I/O |

***Note:*** ** Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | TMS | TMS | TMS |
| 10 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 11 | GND | GND | GND |
| 12 | I/O | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 20 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 21 | I/O | I/O | I/O |
| 22 | I/O | I/O | I/O |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | GND | GND | GND |
| 29 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 30 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | I/O | I/O | I/O |
| 36 | GND | GND | GND |

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 37 | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | I/O | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | PRB, I/O | PRB, I/O | PRB, I/O |
| 55 | I/O | I/O | I/O |
| 56 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 57 | GND | GND | GND |
| 58 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 59 | I/O | I/O | I/O |
| 60 | HCLK | HCLK | HCLK |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 69 | I/O | I/O | I/O |
| 70 | I/O | I/O | I/O |
| 71 | TDO, I/O | TDO, I/O | TDO, I/O |
| 72 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 73 | GND | GND | GND |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 80 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 81 | GND | GND | GND |
| 82 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | I/O |
| 89 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 90 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 99 | GND | GND | GND |
| 100 | I/O | I/O | I/O |
| 101 | GND | GND | GND |
| 102 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 103 | I/O | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 109 | GND | GND | GND |
| 110 | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | I/O | I/O | I/O |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | CLKA | CLKA | CLKA |
| 126 | CLKB | CLKB | CLKB |
| 127 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 128 | GND | GND | GND |
| 129 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 130 | I/O | I/O | I/O |
| 131 | PRA, I/O | PRA, I/O | PRA, I/O |
| 132 | I/O | I/O | I/O |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | TCK, I/O | TCK, I/O | TCK, I/O |

| 176-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | NC | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | I/O | I/O | I/O |
| 10 | TMS | TMS | TMS |
| 11 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 12 | NC | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | I/O | I/O | I/O |
| 20 | I/O | I/O | I/O |
| 21 | GND | GND | GND |
| 22 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 23 | GND | GND | GND |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | I/O | I/O | I/O |
| 29 | I/O | I/O | I/O |
| 30 | I/O | I/O | I/O |
| 31 | I/O | I/O | I/O |
| 32 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 33 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 34 | I/O | I/O | I/O |

| 176-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 35 | I/O | I/O | I/O |
| 36 | I/O | I/O | I/O |
| 37 | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | NC | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | NC | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | GND | GND | GND |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 53 | I/O | I/O | I/O |
| 54 | NC | I/O | I/O |
| 55 | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O |
| 57 | NC | I/O | I/O |
| 58 | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O |
| 60 | I/O | I/O | I/O |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | PRB, I/O | PRB, I/O | PRB, I/O |
| 65 | GND | GND | GND |
| 66 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 67 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 68 | I/O | I/O | I/O |

# 313-Pin PBGA

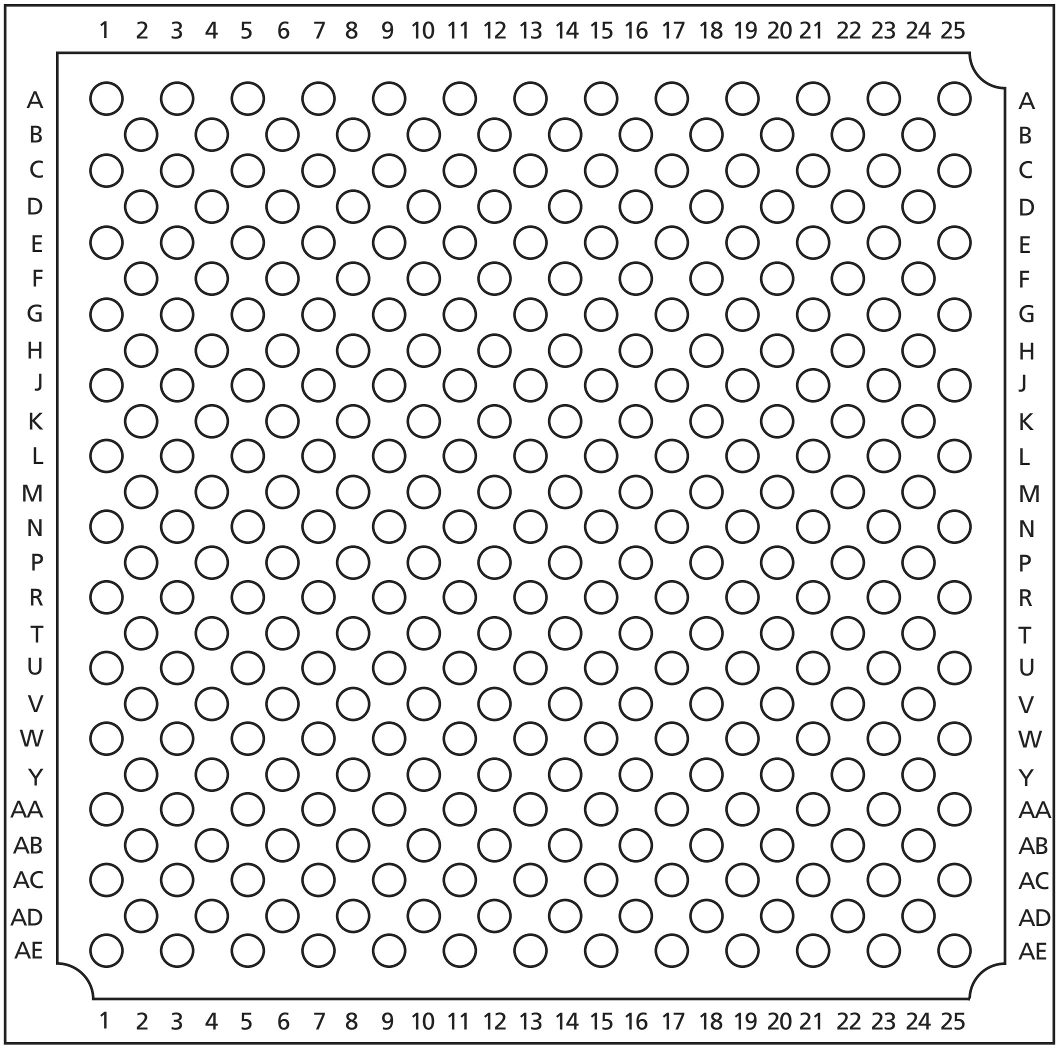

*Figure 2-6* • **313-Pin PBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

# 329-Pin PBGA

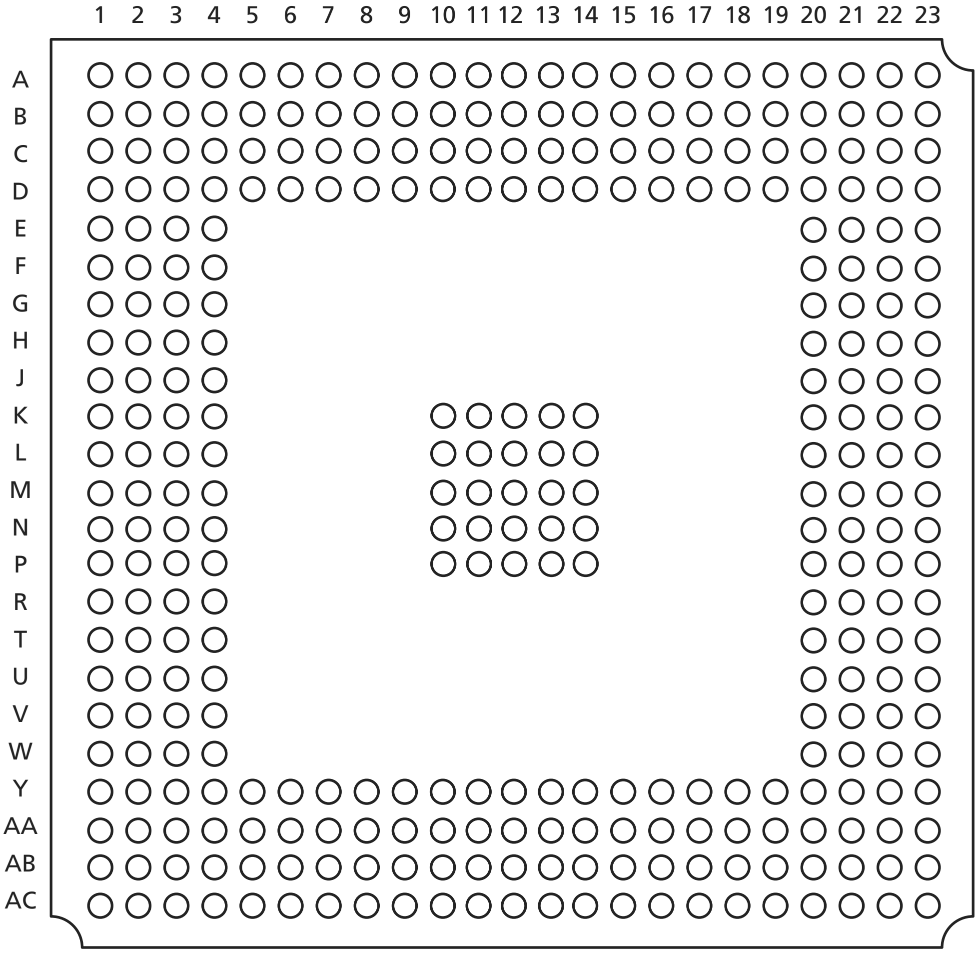

*Figure 2-7* • **329-Pin PBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32 Function** |
| T22 | I/O |
| T23 | I/O |
| U1 | I/O |
| U2 | I/O |
| U3 | $V_{CCA}$ |
| U4 | I/O |
| U20 | I/O |
| U21 | $V_{CCA}$ |
| U22 | I/O |
| U23 | I/O |
| V1 | $V_{CCI}$ |
| V2 | I/O |
| V3 | I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32 Function** |
| V4 | I/O |
| V20 | I/O |
| V21 | I/O |
| V22 | I/O |
| V23 | I/O |
| W1 | I/O |
| W2 | I/O |
| W3 | I/O |
| W4 | I/O |
| W20 | I/O |
| W21 | I/O |
| W22 | I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32 Function** |
| W23 | NC |
| Y1 | NC |
| Y2 | I/O |
| Y3 | I/O |
| Y4 | GND |
| Y5 | I/O |
| Y6 | I/O |
| Y7 | I/O |
| Y8 | I/O |
| Y9 | I/O |
| Y10 | I/O |
| Y11 | I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32 Function** |
| Y12 | $V_{CCA}$ |
| Y13 | $V_{CCR}$ |
| Y14 | I/O |
| Y15 | I/O |
| Y16 | I/O |
| Y17 | I/O |
| Y18 | I/O |
| Y19 | I/O |
| Y20 | GND |
| Y21 | I/O |
| Y22 | I/O |
| Y23 | I/O |

| 144-Pin FBGA | |
|---|---|
| Pin Number | A54SX08 Function |
| A1 | I/O |
| A2 | I/O |
| A3 | I/O |
| A4 | I/O |
| A5 | $V_{CCA}$ |
| A6 | GND |
| A7 | CLKA |
| A8 | I/O |
| A9 | I/O |
| A10 | I/O |
| A11 | I/O |
| A12 | I/O |
| B1 | I/O |
| B2 | GND |
| B3 | I/O |
| B4 | I/O |
| B5 | I/O |
| B6 | I/O |
| B7 | CLKB |
| B8 | I/O |
| B9 | I/O |
| B10 | I/O |
| B11 | GND |
| B12 | I/O |
| C1 | I/O |
| C2 | I/O |
| C3 | TCK, I/O |
| C4 | I/O |
| C5 | I/O |
| C6 | PRA, I/O |
| C7 | I/O |
| C8 | I/O |
| C9 | I/O |
| C10 | I/O |
| C11 | I/O |
| C12 | I/O |

| 144-Pin FBGA | |
|---|---|
| Pin Number | A54SX08 Function |
| D1 | I/O |
| D2 | $V_{CCI}$ |
| D3 | TDI, I/O |
| D4 | I/O |
| D5 | I/O |
| D6 | I/O |
| D7 | I/O |
| D8 | I/O |
| D9 | I/O |
| D10 | I/O |
| D11 | I/O |
| D12 | I/O |
| E1 | I/O |
| E2 | I/O |
| E3 | I/O |
| E4 | I/O |
| E5 | TMS |
| E6 | $V_{CCI}$ |
| E7 | $V_{CCI}$ |
| E8 | $V_{CCI}$ |
| E9 | $V_{CCA}$ |
| E10 | I/O |
| E11 | GND |
| E12 | I/O |
| F1 | I/O |
| F2 | I/O |
| F3 | $V_{CCR}$ |
| F4 | I/O |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | $V_{CCI}$ |
| F9 | I/O |
| F10 | GND |
| F11 | I/O |
| F12 | I/O |

| 144-Pin FBGA | |
|---|---|
| Pin Number | A54SX08 Function |
| G1 | I/O |
| G2 | GND |
| G3 | I/O |
| G4 | I/O |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | $V_{CCI}$ |
| G9 | I/O |
| G10 | I/O |
| G11 | I/O |
| G12 | I/O |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| H5 | $V_{CCA}$ |
| H6 | $V_{CCA}$ |
| H7 | $V_{CCI}$ |
| H8 | $V_{CCI}$ |
| H9 | $V_{CCA}$ |
| H10 | I/O |
| H11 | I/O |
| H12 | $V_{CCR}$ |
| J1 | I/O |
| J2 | I/O |
| J3 | I/O |
| J4 | I/O |
| J5 | I/O |
| J6 | PRB, I/O |
| J7 | I/O |
| J8 | I/O |
| J9 | I/O |
| J10 | I/O |
| J11 | I/O |
| J12 | $V_{CCA}$ |

| 144-Pin FBGA | |
|---|---|
| Pin Number | A54SX08 Function |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | I/O |
| K5 | I/O |
| K6 | I/O |
| K7 | GND |
| K8 | I/O |
| K9 | I/O |
| K10 | GND |
| K11 | I/O |
| K12 | I/O |
| L1 | GND |
| L2 | I/O |
| L3 | I/O |
| L4 | I/O |
| L5 | I/O |
| L6 | I/O |
| L7 | HCLK |
| L8 | I/O |
| L9 | I/O |
| L10 | I/O |
| L11 | I/O |
| L12 | I/O |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | I/O |
| M5 | I/O |
| M6 | I/O |
| M7 | $V_{CCA}$ |
| M8 | I/O |
| M9 | I/O |
| M10 | I/O |
| M11 | TDO, I/O |
| M12 | I/O |