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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

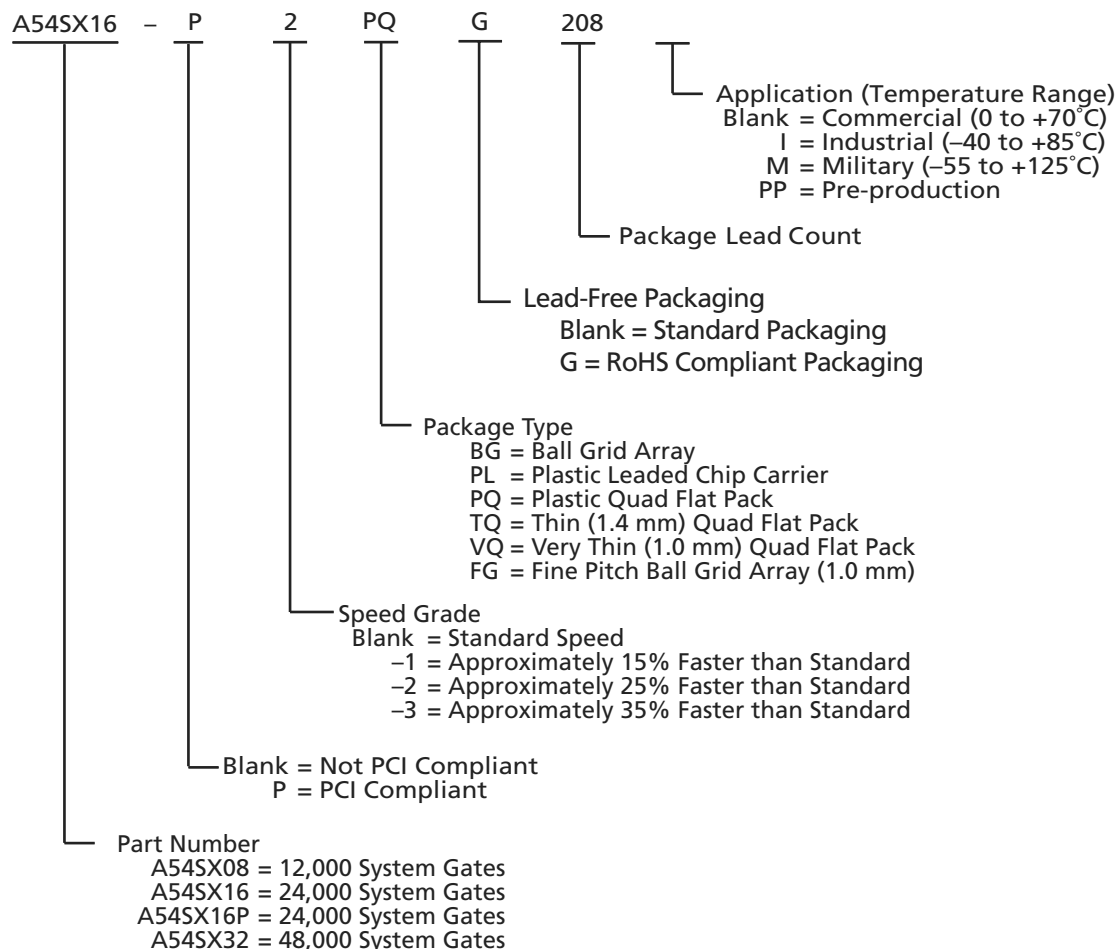
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	174
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	208-BFCQFP with Tie Bar
Supplier Device Package	208-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-cq208b

Ordering Information



Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PLCC 84-Pin	VQFP 100-Pin	PQFP 208-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 313-Pin	PBGA 329-Pin	FBGA 144-Pin
A54SX08	69	81	130	113	128	–	–	111
A54SX16	–	81	175	–	147	–	–	–
A54SX16P	–	81	175	113	147	–	–	–
A54SX32	–	–	174	113	147	249	249	–

Note: Package Definitions (Consult your local Actel sales representative for product availability):

PLCC = Plastic Leaded Chip Carrier

PQFP = Plastic Quad Flat Pack

TQFP = Thin Quad Flat Pack

VQFP = Very Thin Quad Flat Pack

PBGA = Plastic Ball Grid Array

FBGA = Fine Pitch (1.0 mm) Ball Grid Array

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional

flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.

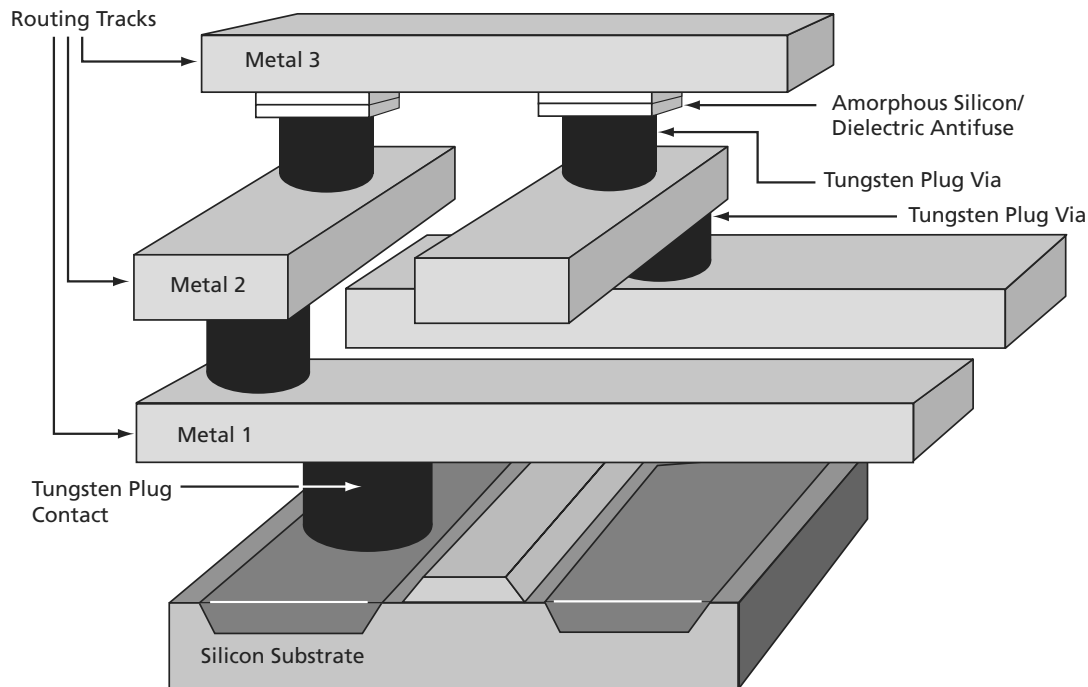


Figure 1-1 • SX Family Interconnect Elements

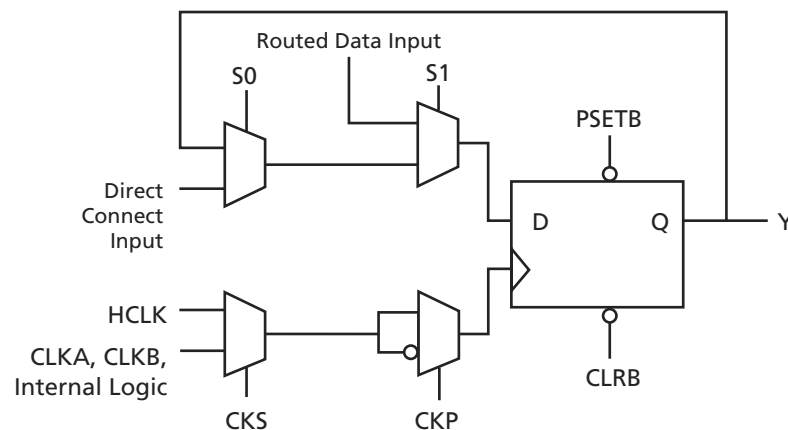


Figure 1-2 • R-Cell

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility

enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

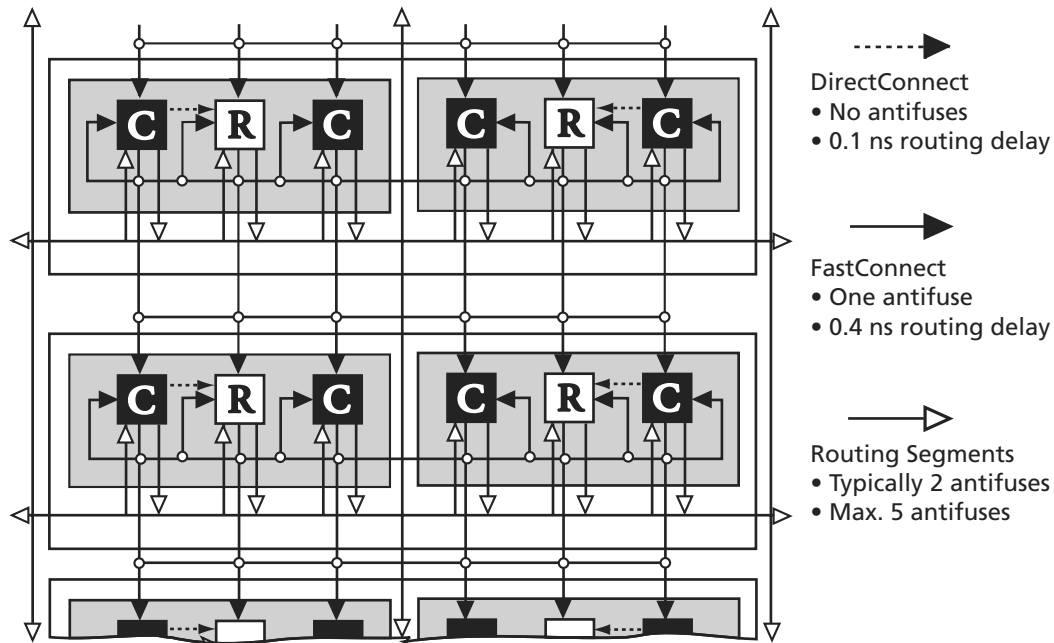


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

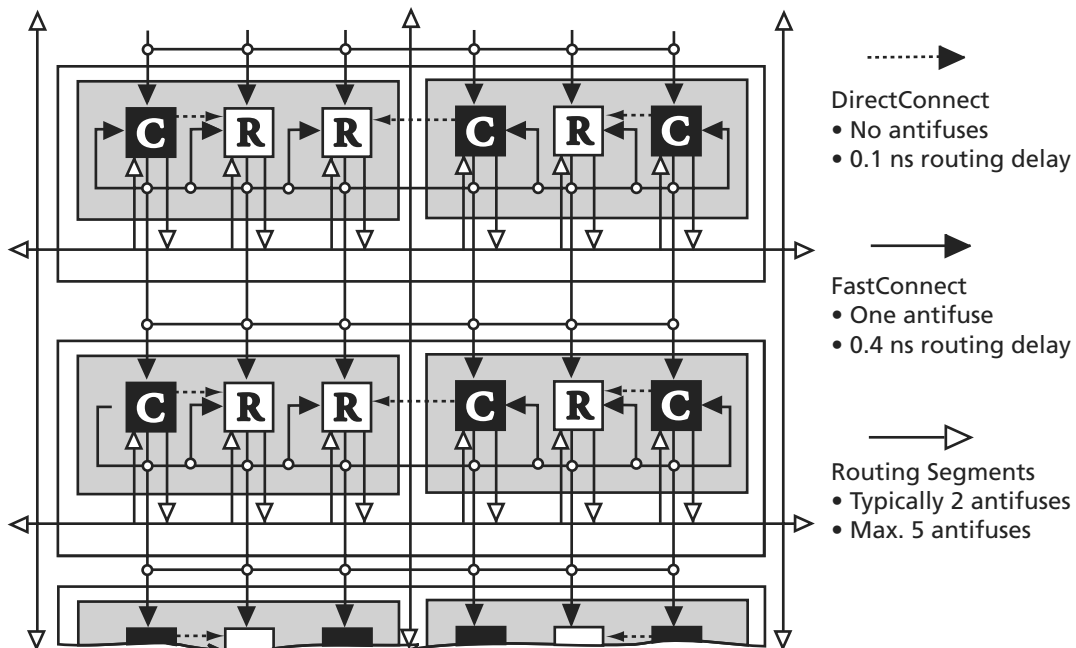


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

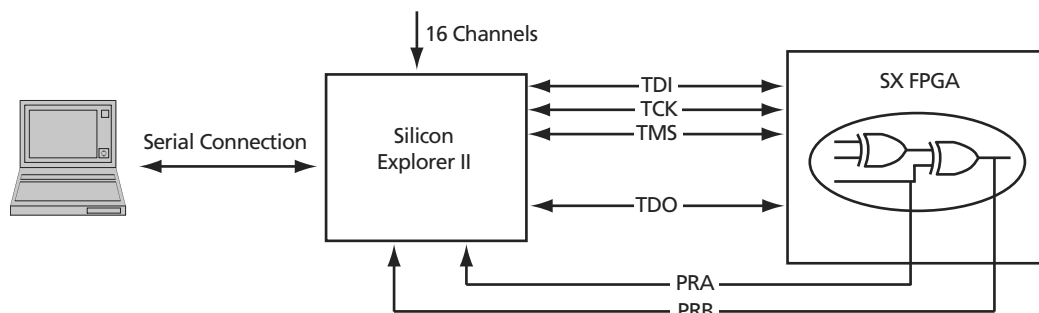


Figure 1-8 • Probe Setup

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II are compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an SX device using Silicon Sculptor II are as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming SX devices, refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

3.3 V / 5 V Operating Conditions

Table 1-3 • Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
V_{CCR}^2	DC Supply Voltage ³	-0.3 to + 6.0	V
V_{CCA}^2	DC Supply Voltage	-0.3 to + 4.0	V
V_{CCI}^2	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	-0.3 to + 4.0	V
V_{CCI}^2	DC Supply Voltage (A54SX16P)	-0.3 to + 6.0	V
V_I	Input Voltage	-0.5 to + 5.5	V
V_O	Output Voltage	-0.5 to + 3.6	V
I_{IO}	I/O Source Sink Current ³	-30 to + 5.0	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.
2. V_{CCR} in the A54SX16P must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.
3. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than $V_{CC} + 0.5$ V or less than $GND - 0.5$ V, the internal protection diodes will forward-bias and can draw excessive current.

A54SX16P DC Specifications (3.3 V PCI Operation)

Table 1-8 • A54SX16P DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		3.0	3.6	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CC}$	V
I_{IPU}	Input Pull-up Voltage ¹		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current ²	$0 < V_{IN} < V_{CC}$		± 10	μA
V_{OH}	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OUT} = 1500 \mu A$		$0.1V_{CC}$	V
C_{IN}	Input Pin Capacitance ³			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance ⁴			8	pF

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

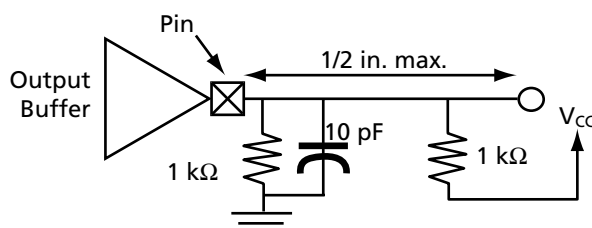
A54SX16P AC Specifications (3.3 V PCI Operation)

Table 1-9 • A54SX16P AC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CC}^1$			mA
		$0.3V_{CC} \leq V_{OUT} < 0.9V_{CC}^1$	$-12V_{CC}$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}^{1,2}$	$-17.1 + (V_{CC} - V_{OUT})$	EQ 1-3 on page 1-14	
	(Test Point)	$V_{OUT} = 0.7V_{CC}^2$		$-32V_{CC}$	mA
$I_{OL(AC)}$	Switching Current High	$V_{CC} > V_{OUT} \geq 0.6V_{CC}^1$			mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}^1$	$16V_{CC}$		mA
		$0.18V_{CC} > V_{OUT} > 0^{1,2}$	$26.7V_{OUT}$	EQ 1-4 on page 1-14	mA
	(Test Point)	$V_{OUT} = 0.18V_{CC}^2$		$38V_{CC}$	
I_{CL}	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$-3 < V_{IN} \leq -1$	$25 + (V_{IN} - V_{OUT} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate ³	0.2V _{CC} to 0.6V _{CC} load	1	4	V/ns
$slew_F$	Output Fall Slew Rate ³	0.6V _{CC} to 0.2V _{CC} load	1	4	V/ns

Notes:

1. Refer to the V/I curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.



Power-Up Sequencing

Table 1-10 • Power-Up Sequencing

V _{CCA}	V _{CCR}	V _{CCI}	Power-Up Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Note: No inputs should be driven (high or low) before completion of power-up.

Power-Down Sequencing

Table 1-11 • Power-Down Sequencing

V _{CCA}	V _{CCR}	V _{CCI}	Power-Down Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Note: No inputs should be driven (high or low) after the beginning of the power-down sequence.

Table 1-13 shows capacitance values for various devices.

Table 1-13 • Capacitance Values for Devices

	A545X08	A545X16	A545X16P	A545X32
C_{EQM} (pF)	4.0	4.0	4.0	4.0
C_{EQI} (pF)	3.4	3.4	3.4	3.4
C_{EQO} (pF)	4.7	4.7	4.7	4.7
C_{EQCR} (pF)	1.6	1.6	1.6	1.6
C_{EQHV}	0.615	0.615	0.615	0.615
C_{EQHF}	60	96	96	140
r_1 (pF)	87	138	138	171
r_2 (pF)	87	138	138	171

Table 1-14 • Power Consumption Guidelines

Description	Power Consumption Guideline
Logic Modules (m)	20% of modules
Inputs Switching (n)	# inputs/4
Outputs Switching (p)	# outputs/4
First Routed Array Clock Loads (q_1)	20% of register cells
Second Routed Array Clock Loads (q_2)	20% of register cells
Load Capacitance (C_L)	35 pF
Average Logic Module Switching Rate (f_m)	$f/10$
Average Input Switching Rate (f_n)	$f/5$
Average Output Switching Rate (f_p)	$f/10$
Average First Routed Array Clock Rate (f_{q1})	$f/2$
Average Second Routed Array Clock Rate (f_{q2})	$f/2$
Average Dedicated Array Clock Rate (f_{s1})	f
Dedicated Clock Array Clock Loads (s_1)	20% of regular modules

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{\text{Total}} = P_{\text{AC}} (\text{dynamic power}) + P_{\text{DC}} (\text{static power})$$

EQ 1-9

Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A545X16P device. A pattern of 0101... was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101... caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

AC Power Dissipation

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-10

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-11

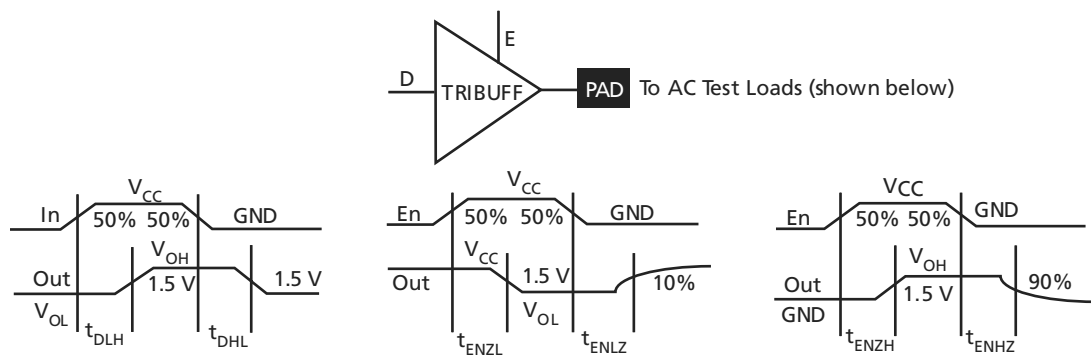


Figure 1-13 • Output Buffer Delays

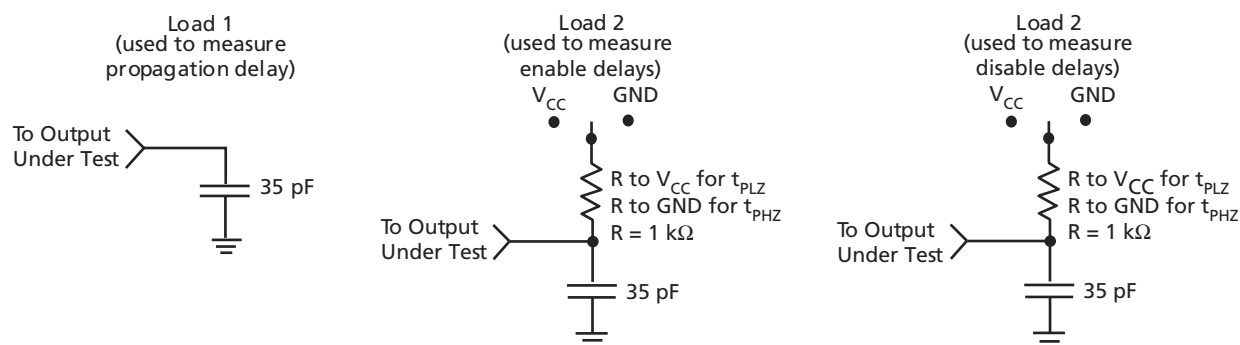


Figure 1-14 • AC Test Loads

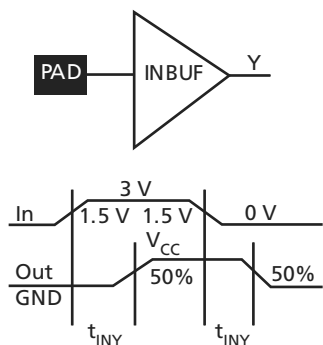


Figure 1-15 • Input Buffer Delays

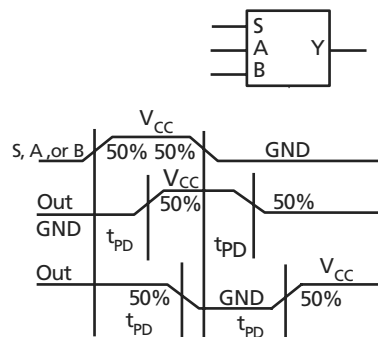


Figure 1-16 • C-Cell Delays

Table 1-17 • A54SX08 Timing Characteristics (Continued)

(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t _{HCKH}	Input LOW to HIGH (pad to R-Cell input)	1.0		1.1		1.3		1.5		ns
t _{HCKL}	Input HIGH to LOW (pad to R-Cell input)	1.0		1.2		1.4		1.6		ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew	0.1		0.2		0.2		0.2		ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t _{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)	1.3		1.5		1.7		2.0		ns
t _{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell Input)	1.4		1.6		1.8		2.1		ns
t _{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)	1.4		1.7		1.9		2.2		ns
t _{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)	1.5		1.7		2.0		2.3		ns
t _{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)	1.5		1.7		1.9		2.2		ns
t _{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)	1.5		1.8		2.0		2.3		ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (light load)	0.1		0.2		0.2		0.2		ns
t _{RCKSW}	Maximum Skew (50% load)	0.3		0.3		0.4		0.4		ns
t _{RCKSW}	Maximum Skew (100% load)	0.3		0.3		0.4		0.4		ns
TTL Output Module Timing ¹										
t _{DLH}	Data-to-Pad LOW to HIGH	1.6		1.9		2.1		2.5		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.6		1.9		2.1		2.5		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.8		3.2		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3		2.7		3.1		3.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	1.4		1.7		1.9		2.2		ns

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	NC	I/O	I/O
5	I/O	I/O	I/O
6	NC	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	I/O	I/O	I/O
11	TMS	TMS	TMS
12	V _{CCI}	V _{CCI}	V _{CCI}
13	I/O	I/O	I/O
14	NC	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	NC	I/O	I/O
24	I/O	I/O	I/O
25	V _{CCR}	V _{CCR}	V _{CCR}
26	GND	GND	GND
27	V _{CCA}	V _{CCA}	V _{CCA}
28	GND	GND	GND
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	NC	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	I/O	I/O
36	I/O	I/O	I/O

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	NC	I/O	I/O
40	V _{CCI}	V _{CCI}	V _{CCI}
41	V _{CCA}	V _{CCA}	V _{CCA}
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	NC	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	I/O	I/O	I/O
52	GND	GND	GND
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	V _{CCI}	V _{CCI}	V _{CCI}
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65*	I/O	I/O	NC*
66	I/O	I/O	I/O
67	NC	I/O	I/O
68	I/O	I/O	I/O
69	I/O	I/O	I/O
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
73	NC	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND
78	V _{CCA}	V _{CCA}	V _{CCA}
79	GND	GND	GND
80	V _{CCR}	V _{CCR}	V _{CCR}
81	I/O	I/O	I/O
82	HCLK	HCLK	HCLK
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	NC	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	NC	I/O	I/O
89	I/O	I/O	I/O
90	I/O	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	NC	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	NC	I/O	I/O
98	V _{CCI}	V _{CCI}	V _{CCI}
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	I/O	I/O
107	I/O	I/O	I/O
108	NC	I/O	I/O

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	V _{CCA}	V _{CCA}	V _{CCA}
115	V _{CCI}	V _{CCI}	V _{CCI}
116	NC	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	NC	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	NC	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	NC	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	GND	GND	GND
130	V _{CCA}	V _{CCA}	V _{CCA}
131	GND	GND	GND
132	V _{CCR}	V _{CCR}	V _{CCR}
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	I/O	I/O	I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V _{CCA}	V _{CCA}	V _{CCA}
80	V _{CCI}	V _{CCI}	V _{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V _{CCA}	V _{CCA}	V _{CCA}
90	V _{CCR}	V _{CCR}	V _{CCR}
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V _{CCI}	V _{CCI}	V _{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
109	GND	GND	GND
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V _{CCI}	V _{CCI}	V _{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	V _{CCR}	V _{CCR}	V _{CCR}
128	GND	GND	GND
129	V _{CCA}	V _{CCA}	V _{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

100-Pin VQFP

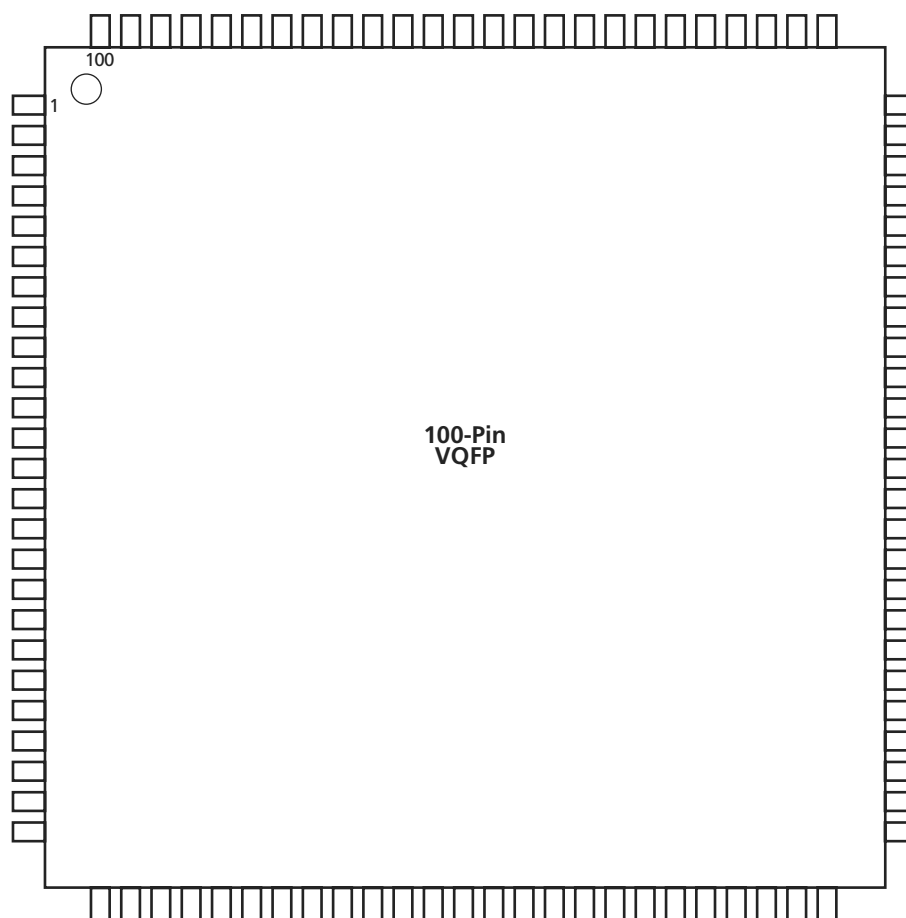


Figure 2-5 • 100-Pin VQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

313-Pin PBGA

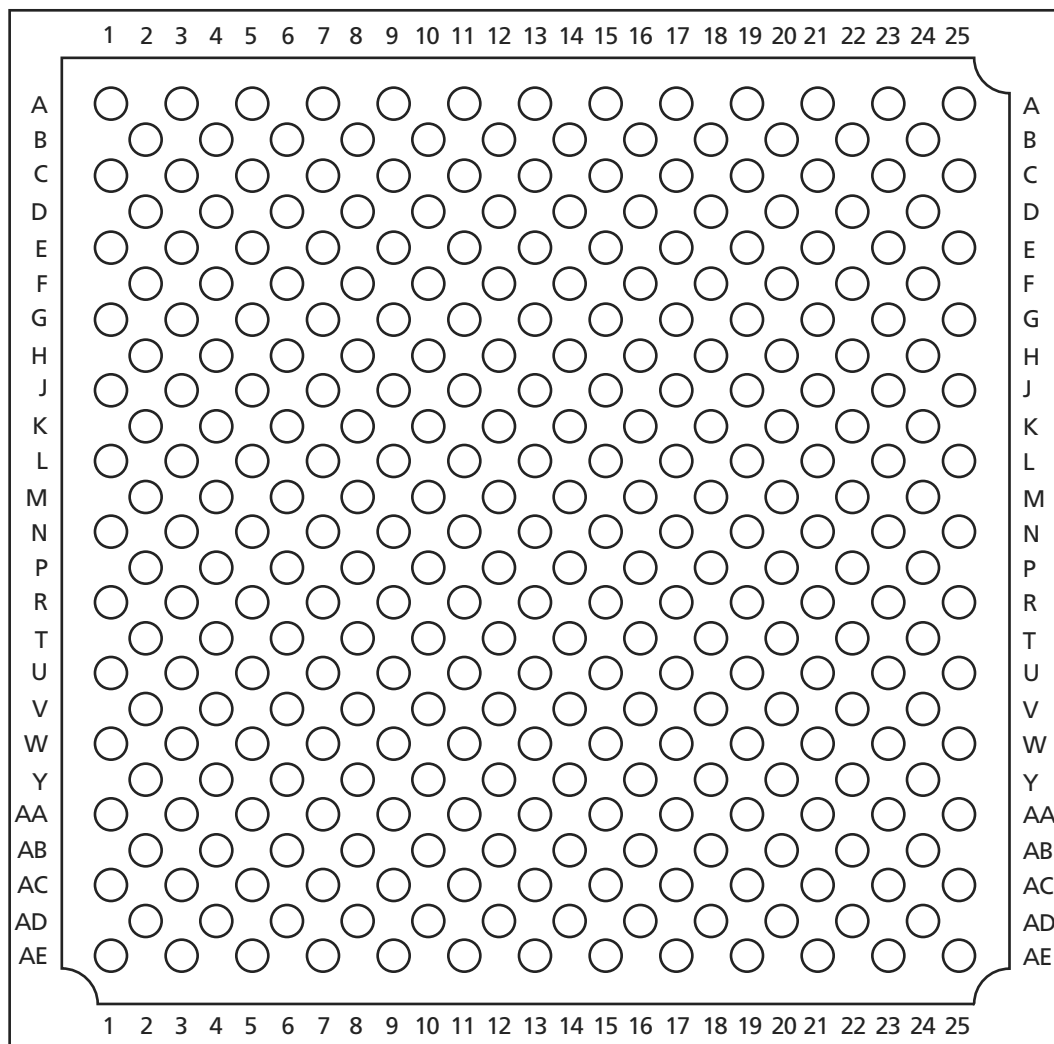


Figure 2-6 • 313-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

313-Pin PBGA		313-Pin PBGA		313-Pin PBGA		313-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
H20	I/O	L25	I/O	R5	I/O	V10	I/O
H22	V _{CCI}	M2	I/O	R7	I/O	V12	I/O
H24	I/O	M4	I/O	R9	I/O	V14	I/O
J1	I/O	M6	I/O	R11	I/O	V16	NC
J3	I/O	M8	I/O	R13	GND	V18	I/O
J5	I/O	M10	I/O	R15	I/O	V20	I/O
J7	NC	M12	GND	R17	I/O	V22	V _{CCA}
J9	I/O	M14	GND	R19	I/O	V24	V _{CCI}
J11	I/O	M16	V _{CCI}	R21	I/O	W1	I/O
J13	CLKA	M18	I/O	R23	I/O	W3	I/O
J15	I/O	M20	I/O	R25	I/O	W5	I/O
J17	I/O	M22	I/O	T2	I/O	W7	NC
J19	I/O	M24	I/O	T4	I/O	W9	I/O
J21	GND	N1	I/O	T6	I/O	W11	I/O
J23	I/O	N3	V _{CCA}	T8	I/O	W13	V _{CCI}
J25	I/O	N5	V _{CCR}	T10	I/O	W15	I/O
K2	I/O	N7	I/O	T12	I/O	W17	I/O
K4	I/O	N9	V _{CCI}	T14	HCLK	W19	I/O
K6	I/O	N11	GND	T16	I/O	W21	I/O
K8	V _{CCI}	N13	GND	T18	I/O	W23	I/O
K10	I/O	N15	GND	T20	I/O	W25	I/O
K12	I/O	N17	I/O	T22	I/O	Y2	I/O
K14	I/O	N19	I/O	T24	I/O	Y4	I/O
K16	I/O	N21	I/O	U1	I/O	Y6	I/O
K18	I/O	N23	V _{CCR}	U3	I/O	Y8	I/O
K20	V _{CCA}	N25	V _{CCA}	U5	V _{CCI}	Y10	I/O
K22	I/O	P2	I/O	U7	I/O	Y12	I/O
K24	I/O	P4	I/O	U9	I/O	Y14	I/O
L1	I/O	P6	I/O	U11	I/O	Y16	I/O
L3	I/O	P8	I/O	U13	I/O	Y18	I/O
L5	I/O	P10	I/O	U15	I/O	Y20	NC
L7	I/O	P12	GND	U17	I/O	Y22	I/O
L9	I/O	P14	GND	U19	I/O	Y24	NC
L11	I/O	P16	I/O	U21	I/O		
L13	GND	P18	I/O	U23	I/O		
L15	I/O	P20	NC	U25	I/O		
L17	I/O	P22	I/O	V2	V _{CCA}		
L19	I/O	P24	I/O	V4	I/O		
L21	I/O	R1	I/O	V6	I/O		
L23	I/O	R3	I/O	V8	I/O		

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
A1	GND	AA13	I/O	AC2	V _{CCI}	B14	I/O
A2	GND	AA14	I/O	AC3	NC	B15	I/O
A3	V _{CCI}	AA15	I/O	AC4	I/O	B16	I/O
A4	NC	AA16	I/O	AC5	I/O	B17	I/O
A5	I/O	AA17	I/O	AC6	I/O	B18	I/O
A6	I/O	AA18	I/O	AC7	I/O	B19	I/O
A7	V _{CCI}	AA19	I/O	AC8	I/O	B20	I/O
A8	NC	AA20	TDO, I/O	AC9	V _{CCI}	B21	I/O
A9	I/O	AA21	V _{CCI}	AC10	I/O	B22	GND
A10	I/O	AA22	I/O	AC11	I/O	B23	V _{CCI}
A11	I/O	AA23	V _{CCI}	AC12	I/O	C1	NC
A12	I/O	AB1	I/O	AC13	I/O	C2	TDI, I/O
A13	CLKB	AB2	GND	AC14	I/O	C3	GND
A14	I/O	AB3	I/O	AC15	NC	C4	I/O
A15	I/O	AB4	I/O	AC16	I/O	C5	I/O
A16	I/O	AB5	I/O	AC17	I/O	C6	I/O
A17	I/O	AB6	I/O	AC18	I/O	C7	I/O
A18	I/O	AB7	I/O	AC19	I/O	C8	I/O
A19	I/O	AB8	I/O	AC20	I/O	C9	I/O
A20	I/O	AB9	I/O	AC21	NC	C10	I/O
A21	NC	AB10	I/O	AC22	V _{CCI}	C11	I/O
A22	V _{CCI}	AB11	PRB, I/O	AC23	GND	C12	I/O
A23	GND	AB12	I/O	B1	V _{CCI}	C13	I/O
AA1	V _{CCI}	AB13	HCLK	B2	GND	C14	I/O
AA2	I/O	AB14	I/O	B3	I/O	C15	I/O
AA3	GND	AB15	I/O	B4	I/O	C16	I/O
AA4	I/O	AB16	I/O	B5	I/O	C17	I/O
AA5	I/O	AB17	I/O	B6	I/O	C18	I/O
AA6	I/O	AB18	I/O	B7	I/O	C19	I/O
AA7	I/O	AB19	I/O	B8	I/O	C20	I/O
AA8	I/O	AB20	I/O	B9	I/O	C21	V _{CCI}
AA9	I/O	AB21	I/O	B10	I/O	C22	GND
AA10	I/O	AB22	GND	B11	I/O	C23	NC
AA11	I/O	AB23	I/O	B12	PRA, I/O	D1	I/O
AA12	I/O	AC1	GND	B13	CLKA	D2	I/O

329-Pin PBGA	
Pin Number	A54SX32 Function
T22	I/O
T23	I/O
U1	I/O
U2	I/O
U3	V _{CCA}
U4	I/O
U20	I/O
U21	V _{CCA}
U22	I/O
U23	I/O
V1	V _{CCI}
V2	I/O
V3	I/O

329-Pin PBGA	
Pin Number	A54SX32 Function
V4	I/O
V20	I/O
V21	I/O
V22	I/O
V23	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W20	I/O
W21	I/O
W22	I/O

329-Pin PBGA	
Pin Number	A54SX32 Function
W23	NC
Y1	NC
Y2	I/O
Y3	I/O
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O

329-Pin PBGA	
Pin Number	A54SX32 Function
Y12	V _{CCA}
Y13	V _{CCR}
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O