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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	203
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BFCQFP Exposed Pad and Tie Bar
Supplier Device Package	256-CQFP (75x75)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a54sx32-cq256">https://www.e-xfl.com/product-detail/microsemi/a54sx32-cq256</a>

## Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

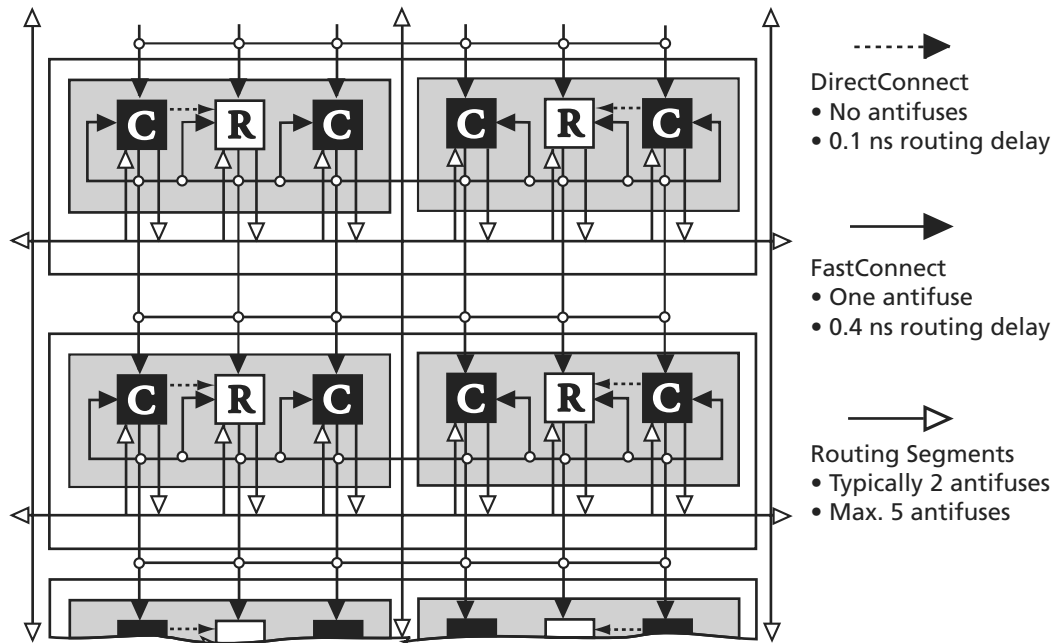


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

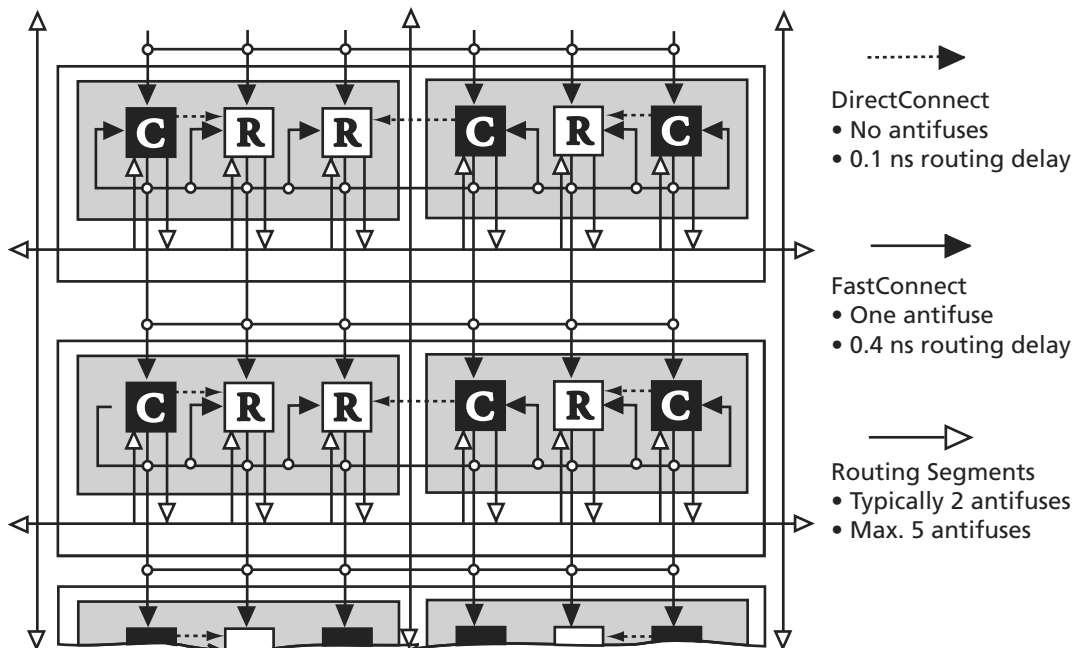


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

The Actel high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hardwired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

## Other Architectural Features

### Technology

The Actel SX family is implemented on a high-voltage twin-well CMOS process using 0.35  $\mu$  design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25  $\Omega$  with a capacitance of 1.0 fF for low signal impedance.

## Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

## I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin.

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

## Power Requirements

The SX family supports 3.3 V operation and is designed to tolerate 5.0 V inputs. (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest power architecture on the market.

Table 1-1 • Supply Voltages

Device	V <sub>CCA</sub>	V <sub>CCI</sub>	V <sub>CCR</sub>	Maximum Input Tolerance	Maximum Output Drive
A54SX08 A54SX16 A54SX32	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
A54SX16-P*	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V

**Note:** \*A54SX16-P has three different entries because it is capable of both a 3.3 V and a 5.0 V drive.

**Table 1-4 • Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to + 70	–40 to + 85	–55 to +125	°C
3.3 V Power Supply Tolerance	±10	±10	±10	%V <sub>CC</sub>
5.0 V Power Supply Tolerance	±5	±10	±10	%V <sub>CC</sub>

**Note:** \*Ambient temperature ( $T_A$ ) is used for commercial and industrial; case temperature ( $T_C$ ) is used for military.

**Table 1-5 • Electrical Specifications**

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V <sub>OH</sub>	(I <sub>OH</sub> = –20 $\mu$ A) (CMOS) (I <sub>OH</sub> = –8 mA) (TTL) (I <sub>OH</sub> = –6 mA) (TTL)	(V <sub>CCI</sub> – 0.1) 2.4	V <sub>CCI</sub> V <sub>CCI</sub>	(V <sub>CCI</sub> – 0.1) 2.4	V <sub>CCI</sub> V <sub>CCI</sub>	V
V <sub>OL</sub>	(I <sub>OL</sub> = 20 $\mu$ A) (CMOS) (I <sub>OL</sub> = 12 mA) (TTL) (I <sub>OL</sub> = 8 mA) (TTL)		0.10 0.50		0.50	V
V <sub>IL</sub>			0.8		0.8	V
V <sub>IH</sub>		2.0		2.0		V
t <sub>R</sub> , t <sub>F</sub>	Input Transition Time t <sub>R</sub> , t <sub>F</sub>		50		50	ns
C <sub>IO</sub>	C <sub>IO</sub> I/O Capacitance		10		10	pF
I <sub>CC</sub>	Standby Current, I <sub>CC</sub>		4.0		4.0	mA
I <sub>CC(D)</sub>	I <sub>CC(D)</sub> I <sub>Dynamic</sub> V <sub>CC</sub> Supply Current	See "Evaluating Power in SX Devices" on page 1-16.				

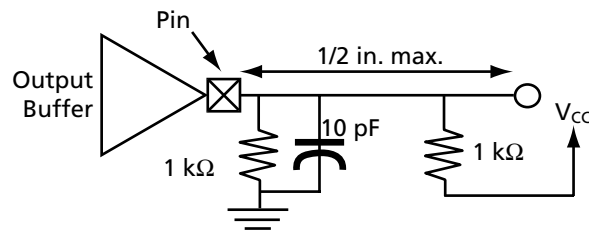
## A54SX16P AC Specifications for (PCI Operation)

Table 1-7 • A54SX16P AC Specifications for (PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4^1$	-44		mA
		$1.4 \leq V_{OUT} < 2.4^1, 2$	$-44 + (V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}^{1, 3}$		EQ 1-1 on page 1-11	
	(Test Point)	$V_{OUT} = 3.1^3$		-142	mA
$I_{OL(AC)}$	Switching Current High	$V_{OUT} \geq 2.2^1$	95		mA
		$2.2 > V_{OUT} > 0.55^1$	$V_{OUT}/0.023$		
		$0.71 > V_{OUT} > 0^{1, 3}$		EQ 1-2 on page 1-11	mA
	(Test Point)	$V_{OUT} = 0.71^3$		206	mA
$I_{CL}$	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load <sup>4</sup>	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load <sup>4</sup>	1	5	V/ns

### Notes:

1. Refer to the *V<sub>I</sub>* curves in Figure 1-9 on page 1-11. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half-size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maxima (A and B) are provided with the respective diagrams in Figure 1-9 on page 1-11. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.



## Power-Up Sequencing

Table 1-10 • Power-Up Sequencing

V <sub>CCA</sub>	V <sub>CCR</sub>	V <sub>CCI</sub>	Power-Up Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

**Note:** No inputs should be driven (high or low) before completion of power-up.

## Power-Down Sequencing

Table 1-11 • Power-Down Sequencing

V <sub>CCA</sub>	V <sub>CCR</sub>	V <sub>CCI</sub>	Power-Down Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

**Note:** No inputs should be driven (high or low) after the beginning of the power-down sequence.

## Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

## Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}}$$

EQ 1-5

## DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • Standby Power

I <sub>CC</sub>	V <sub>CC</sub>	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

$$P_{\text{DC}} = (I_{\text{standby}}) \times V_{\text{CCA}} + (I_{\text{standby}}) \times V_{\text{CCR}} + (I_{\text{standby}}) \times V_{\text{CCI}} + xV_{\text{OL}} \times I_{\text{OL}} + y(V_{\text{CCI}} - V_{\text{OH}}) \times V_{\text{OH}}$$

EQ 1-6

## AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-7

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 \times (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 \times (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 \times (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-8

## Definition of Terms Used in Formula

- m = Number of logic modules switching at  $f_m$
- n = Number of input buffers switching at  $f_n$
- p = Number of output buffers switching at  $f_p$
- $q_1$  = Number of clock loads on the first routed array clock
- $q_2$  = Number of clock loads on the second routed array clock
- x = Number of I/Os at logic low
- y = Number of I/Os at logic high
- $r_1$  = Fixed capacitance due to first routed array clock
- $r_2$  = Fixed capacitance due to second routed array clock
- $s_1$  = Number of clock loads on the dedicated array clock
- $C_{\text{EQM}}$  = Equivalent capacitance of logic modules in pF
- $C_{\text{EQI}}$  = Equivalent capacitance of input buffers in pF
- $C_{\text{EQO}}$  = Equivalent capacitance of output buffers in pF
- $C_{\text{EQCR}}$  = Equivalent capacitance of routed array clock in pF
- $C_{\text{EQHV}}$  = Variable capacitance of dedicated array clock
- $C_{\text{EQHF}}$  = Fixed capacitance of dedicated array clock
- $C_L$  = Output lead capacitance in pF
- $f_m$  = Average logic module switching rate in MHz
- $f_n$  = Average input buffer switching rate in MHz
- $f_p$  = Average output buffer switching rate in MHz
- $f_{q1}$  = Average first routed array clock rate in MHz
- $f_{q2}$  = Average second routed array clock rate in MHz
- $f_{s1}$  = Average dedicated array clock rate in MHz

### Step 1: Define Terms Used in Formula

<b>Module</b>	$V_{CCA}$	3.3
Number of logic modules switching at $f_m$ (Used 50%)	$m$	264
Average logic modules switching rate $f_m$ (MHz) (Guidelines: $f/10$ )	$f_m$	20
Module capacitance $C_{EQM}$ (pF)	$C_{EQM}$	4.0
<b>Input Buffer</b>		
Number of input buffers switching at $f_n$	$n$	1
Average input switching rate $f_n$ (MHz) (Guidelines: $f/5$ )	$f_n$	40
Input buffer capacitance $C_{EQI}$ (pF)	$C_{EQI}$	3.4
<b>Output Buffer</b>		
Number of output buffers switching at $f_p$	$p$	1
Average output buffers switching rate $f_p$ (MHz) (Guidelines: $f/10$ )	$f_p$	20
Output buffers buffer capacitance $C_{EQO}$ (pF)	$C_{EQO}$	4.7
Output Load capacitance $C_L$ (pF)	$C_L$	35
<b>RCLKA</b>		
Number of Clock loads $q_1$	$q_1$	528
Capacitance of routed array clock (pF)	$C_{EQCR}$	1.6
Average clock rate (MHz)	$f_{q1}$	200
Fixed capacitance (pF)	$r_1$	138
<b>RCLKB</b>		
Number of Clock loads $q_2$	$q_2$	0
Capacitance of routed array clock (pF)	$C_{EQCR}$	1.6
Average clock rate (MHz)	$f_{q2}$	0
Fixed capacitance (pF)	$r_2$	138
<b>HCLK</b>		
Number of Clock loads	$s_1$	0
Variable capacitance of dedicated array clock (pF)	$C_{EQHV}$	0.61 5
Fixed capacitance of dedicated array clock (pF)	$C_{EQHF}$	96
Average clock rate (MHz)	$f_{s1}$	0

### Step 2: Calculate Dynamic Power Consumption

$V_{CCA} \times V_{CCA}$	10.89
$m \times f_m \times C_{EQM}$	0.02112
$n \times f_n \times C_{EQI}$	0.000136
$p \times f_p \times (C_{EQO} + C_L)$	0.000794
$0.5 (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1})$	0.11208
$0.5 (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2})$	0
$0.5 (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1})$	0
$P_{AC} = 1.461 \text{ W}$	

### Step 3: Calculate DC Power Dissipation

#### DC Power Dissipation

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + X \times V_{OL} \times I_{OL} + Y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-12

For a rough estimate of DC Power Dissipation, only use  $P_{DC} = (I_{standby}) \times V_{CCA}$ . The rest of the formula provides a very small number that can be considered negligible.

$$P_{DC} = (I_{standby}) \times V_{CCA}$$

$$P_{DC} = .55 \text{ mA} \times 3.3 \text{ V}$$

$$P_{DC} = 0.001815 \text{ W}$$

### Step 4: Calculate Total Power Consumption

$$P_{Total} = P_{AC} + P_{DC}$$

$$P_{Total} = 1.461 + 0.001815$$

$$P_{Total} = 1.4628 \text{ W}$$

### Step 5: Compare Estimated Power Consumption against Characterized Power Consumption

The estimated total power consumption for this design is 1.46 W. The characterized power consumption for this design at 200 MHz is 1.0164 W.



Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.

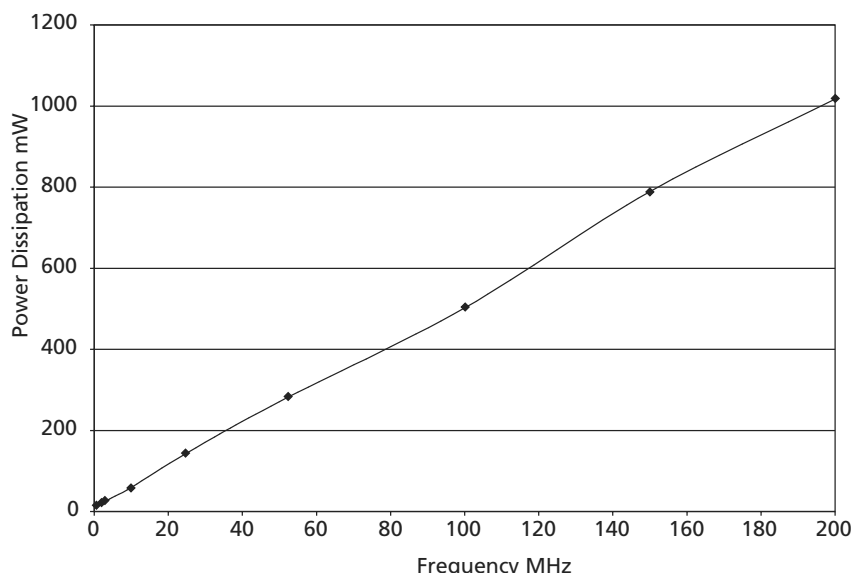


Figure 1-11 • Power Dissipation

## Junction Temperature ( $T_j$ )

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a$$

EQ 1-13

Where:

$T_a$  = Ambient Temperature

$\Delta T$  = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} \times P$$

$P$  = Power calculated from Estimating Power Consumption section

$\theta_{ja}$  = Junction to ambient of package.  $\theta_{ja}$  numbers are located in the "Package Thermal Characteristics" section.

## Package Thermal Characteristics

The device junction to case thermal characteristic is  $\theta_{jc}$ , and the junction to ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

The maximum junction temperature is 150 °C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ (°C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{28^\circ\text{C/W}} = 2.86 \text{ W}$$

EQ 1-14

**Table 1-15 • Package Thermal Characteristics**

Package Type	Pin Count	$\theta_{jc}$	$\theta_{ja}$ Still Air	$\theta_{ja}$ 300 ft/min.	Units
Plastic Leaded Chip Carrier (PLCC)	84	12	32	22	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Very Thin Quad Flatpack (VQFP)	100	10	38	32	°C/W
Plastic Quad Flat Pack (PQFP) without Heat Spreader	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	14.5	°C/W
Plastic Ball Grid Array (PBGA)	313	3	23	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W

**Note:** SX08 does not have a heat spreader.

**Table 1-16 • Temperature and Voltage Derating Factors\***

$V_{CCA}$	Junction Temperature						
	-55	-40	0	25	70	85	125
<b>3.0</b>	0.75	0.78	0.87	0.89	1.00	1.04	1.16
<b>3.3</b>	0.70	0.73	0.82	0.83	0.93	0.97	1.08
<b>3.6</b>	0.66	0.69	0.77	0.78	0.87	0.92	1.02

**Note:** \*Normalized to worst-case commercial,  $T_J = 70^\circ\text{C}$ ,  $V_{CCA} = 3.0\text{ V}$

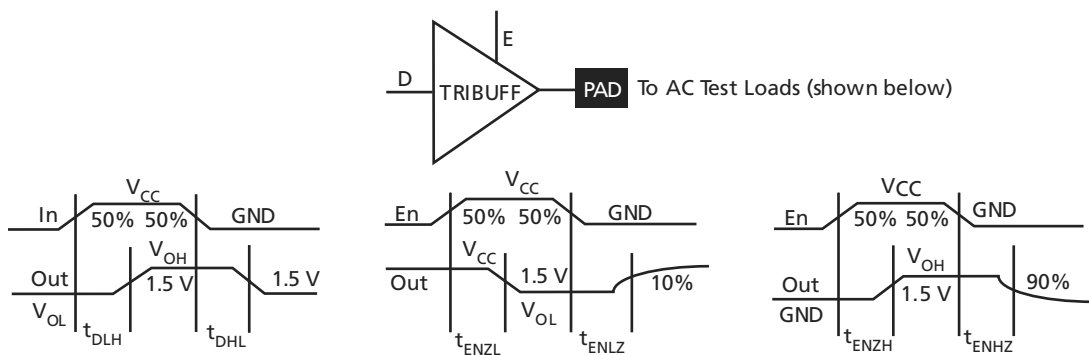


Figure 1-13 • Output Buffer Delays

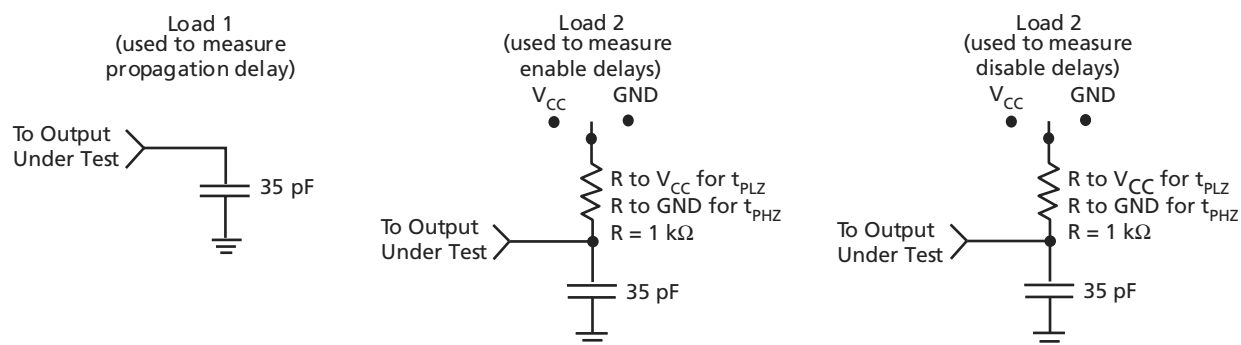


Figure 1-14 • AC Test Loads

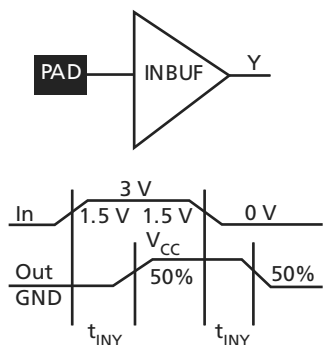


Figure 1-15 • Input Buffer Delays

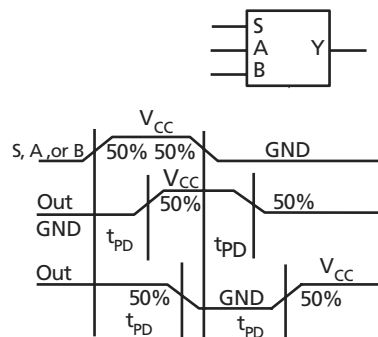


Figure 1-16 • C-Cell Delays

## A54SX16P Timing Characteristics

Table 1-19 • **A54SX16P Timing Characteristics**  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>1</sup>										
t <sub>PD</sub>	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays <sup>2</sup>										
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t <sub>RCO</sub>	Sequential Clock-to-Q	0.9		1.1		1.3		1.4		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t <sub>INYH</sub>	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t <sub>INYL</sub>	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays <sup>2</sup>										
t <sub>IRD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t <sub>IRD12</sub>	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

**Note:**

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 10 pF loading.

## A54SX32 Timing Characteristics

Table 1-20 • **A54SX32 Timing Characteristics**  
(Worst-Case Commercial Conditions,  $V_{CCR} = 4.75\text{ V}$ ,  $V_{CCA}, V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>1</sup>										
t <sub>PD</sub>	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays <sup>2</sup>										
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns
R-Cell Timing										
t <sub>RCO</sub>	Sequential Clock-to-Q	0.8		1.1		1.3		1.4		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t <sub>INYH</sub>	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t <sub>INYL</sub>	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Predicted Input Routing Delays <sup>2</sup>										
t <sub>IRD1</sub>	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay	0.7		0.8		0.9		1.0		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay	1.0		1.2		1.4		1.6		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay	1.4		1.6		1.8		2.1		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay	2.7		3.1		3.5		4.1		ns
t <sub>IRD12</sub>	FO = 12 Routing Delay	4.0		4.7		5.3		6.2		ns

### Note:

- For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except  $t_{ENZL}$  and  $t_{ENZH}$ . For  $t_{ENZL}$  and  $t_{ENZH}$  the loading is 5 pF.

## Pin Description

### CLKA/B Clock A and B

These pins are 3.3 V / 5.0 V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as bidirectional.)

### GND Ground

LOW supply voltage.

### HCLK Dedicated (hardwired) Array Clock

This pin is the 3.3 V / 5.0 V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

### I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, 3.3 V PCI or 5.0 V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

### NC No Connection

This pin is not connected to circuitry within the device.

### PRA, I/O Probe A

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

### PRB, I/O Probe B

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

### TCK Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### TDI Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### TDO Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-2 on page 1-6). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

### V<sub>CCI</sub> Supply Voltage

Supply voltage for I/Os. See Table 1-1 on page 1-5.

### V<sub>CCA</sub> Supply Voltage

Supply voltage for Array. See Table 1-1 on page 1-5.

### V<sub>CCR</sub> Supply Voltage

Supply voltage for input tolerance (required for internal biasing). See Table 1-1 on page 1-5.

84-Pin PLCC	
Pin Number	A54SX08 Function
1	V <sub>CCR</sub>
2	GND
3	V <sub>CCA</sub>
4	PRA, I/O
5	I/O
6	I/O
7	V <sub>CCI</sub>
8	I/O
9	I/O
10	I/O
11	TCK, I/O
12	TDI, I/O
13	I/O
14	I/O
15	I/O
16	TMS
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V <sub>CCI</sub>
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O

84-Pin PLCC	
Pin Number	A54SX08 Function
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V <sub>CCA</sub>
42	GND
43	V <sub>CCR</sub>
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V <sub>CCA</sub>
60	V <sub>CCI</sub>
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V <sub>CCA</sub>
69	GND
70	I/O

84-Pin PLCC	
Pin Number	A54SX08 Function
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	CLKA
84	CLKB

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	NC	I/O	I/O
5	I/O	I/O	I/O
6	NC	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	I/O	I/O	I/O
11	TMS	TMS	TMS
12	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
13	I/O	I/O	I/O
14	NC	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	NC	I/O	I/O
24	I/O	I/O	I/O
25	V <sub>CCR</sub>	V <sub>CCR</sub>	V <sub>CCR</sub>
26	GND	GND	GND
27	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
28	GND	GND	GND
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	NC	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	I/O	I/O
36	I/O	I/O	I/O

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	NC	I/O	I/O
40	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
41	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	NC	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	I/O	I/O	I/O
52	GND	GND	GND
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65*	I/O	I/O	NC*
66	I/O	I/O	I/O
67	NC	I/O	I/O
68	I/O	I/O	I/O
69	I/O	I/O	I/O
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O

**Note:** \* Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).



208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
73	NC	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND
78	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
79	GND	GND	GND
80	V <sub>CCR</sub>	V <sub>CCR</sub>	V <sub>CCR</sub>
81	I/O	I/O	I/O
82	HCLK	HCLK	HCLK
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	NC	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	NC	I/O	I/O
89	I/O	I/O	I/O
90	I/O	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	NC	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	NC	I/O	I/O
98	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	I/O	I/O
107	I/O	I/O	I/O
108	NC	I/O	I/O

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
115	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
116	NC	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	NC	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	NC	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	NC	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	GND	GND	GND
130	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
131	GND	GND	GND
132	V <sub>CCR</sub>	V <sub>CCR</sub>	V <sub>CCR</sub>
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	I/O	I/O	I/O

**Note:** \* Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

## 313-Pin PBGA

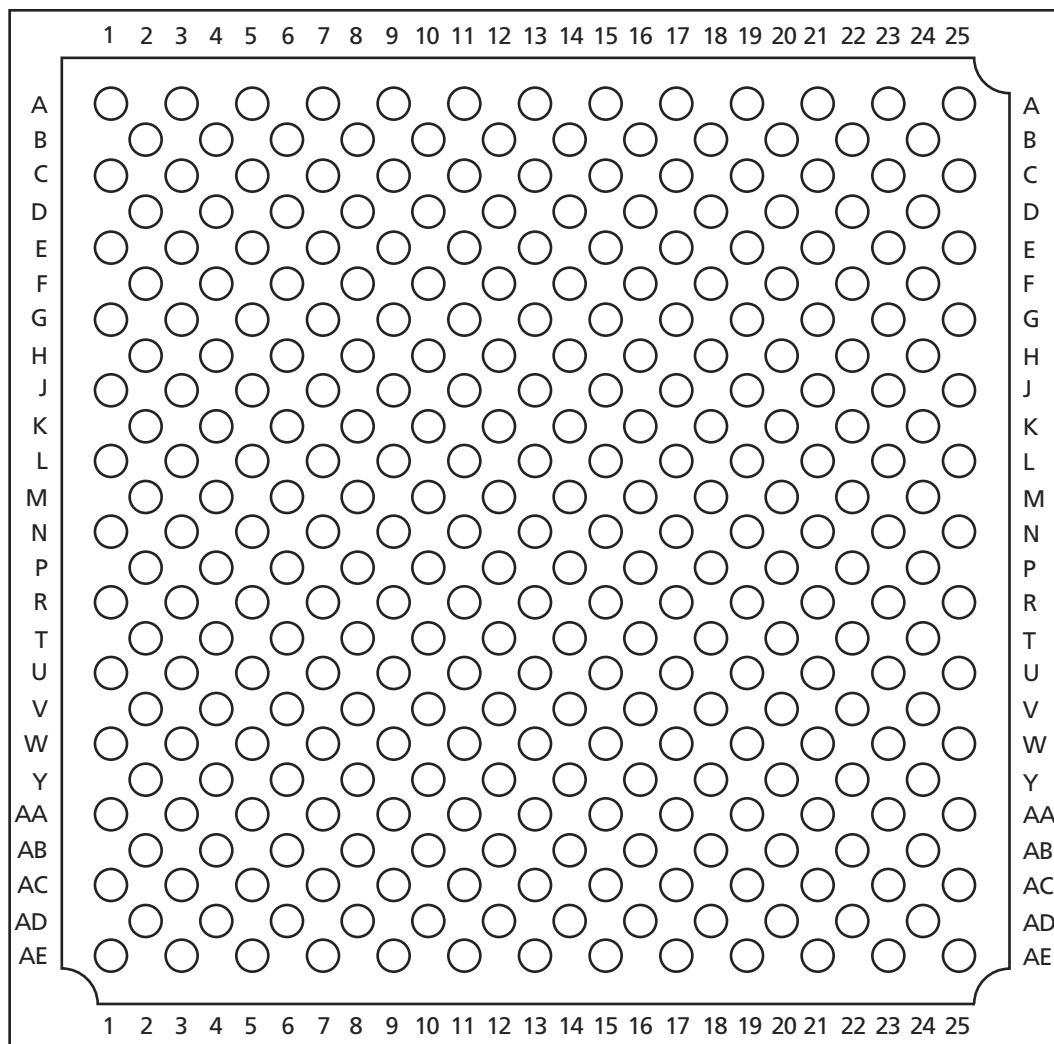


Figure 2-6 • 313-Pin PBGA (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

313-Pin PBGA		313-Pin PBGA		313-Pin PBGA		313-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
H20	I/O	L25	I/O	R5	I/O	V10	I/O
H22	V <sub>CCI</sub>	M2	I/O	R7	I/O	V12	I/O
H24	I/O	M4	I/O	R9	I/O	V14	I/O
J1	I/O	M6	I/O	R11	I/O	V16	NC
J3	I/O	M8	I/O	R13	GND	V18	I/O
J5	I/O	M10	I/O	R15	I/O	V20	I/O
J7	NC	M12	GND	R17	I/O	V22	V <sub>CCA</sub>
J9	I/O	M14	GND	R19	I/O	V24	V <sub>CCI</sub>
J11	I/O	M16	V <sub>CCI</sub>	R21	I/O	W1	I/O
J13	CLKA	M18	I/O	R23	I/O	W3	I/O
J15	I/O	M20	I/O	R25	I/O	W5	I/O
J17	I/O	M22	I/O	T2	I/O	W7	NC
J19	I/O	M24	I/O	T4	I/O	W9	I/O
J21	GND	N1	I/O	T6	I/O	W11	I/O
J23	I/O	N3	V <sub>CCA</sub>	T8	I/O	W13	V <sub>CCI</sub>
J25	I/O	N5	V <sub>CCR</sub>	T10	I/O	W15	I/O
K2	I/O	N7	I/O	T12	I/O	W17	I/O
K4	I/O	N9	V <sub>CCI</sub>	T14	HCLK	W19	I/O
K6	I/O	N11	GND	T16	I/O	W21	I/O
K8	V <sub>CCI</sub>	N13	GND	T18	I/O	W23	I/O
K10	I/O	N15	GND	T20	I/O	W25	I/O
K12	I/O	N17	I/O	T22	I/O	Y2	I/O
K14	I/O	N19	I/O	T24	I/O	Y4	I/O
K16	I/O	N21	I/O	U1	I/O	Y6	I/O
K18	I/O	N23	V <sub>CCR</sub>	U3	I/O	Y8	I/O
K20	V <sub>CCA</sub>	N25	V <sub>CCA</sub>	U5	V <sub>CCI</sub>	Y10	I/O
K22	I/O	P2	I/O	U7	I/O	Y12	I/O
K24	I/O	P4	I/O	U9	I/O	Y14	I/O
L1	I/O	P6	I/O	U11	I/O	Y16	I/O
L3	I/O	P8	I/O	U13	I/O	Y18	I/O
L5	I/O	P10	I/O	U15	I/O	Y20	NC
L7	I/O	P12	GND	U17	I/O	Y22	I/O
L9	I/O	P14	GND	U19	I/O	Y24	NC
L11	I/O	P16	I/O	U21	I/O		
L13	GND	P18	I/O	U23	I/O		
L15	I/O	P20	NC	U25	I/O		
L17	I/O	P22	I/O	V2	V <sub>CCA</sub>		
L19	I/O	P24	I/O	V4	I/O		
L21	I/O	R1	I/O	V6	I/O		
L23	I/O	R3	I/O	V8	I/O		

## 329-Pin PBGA

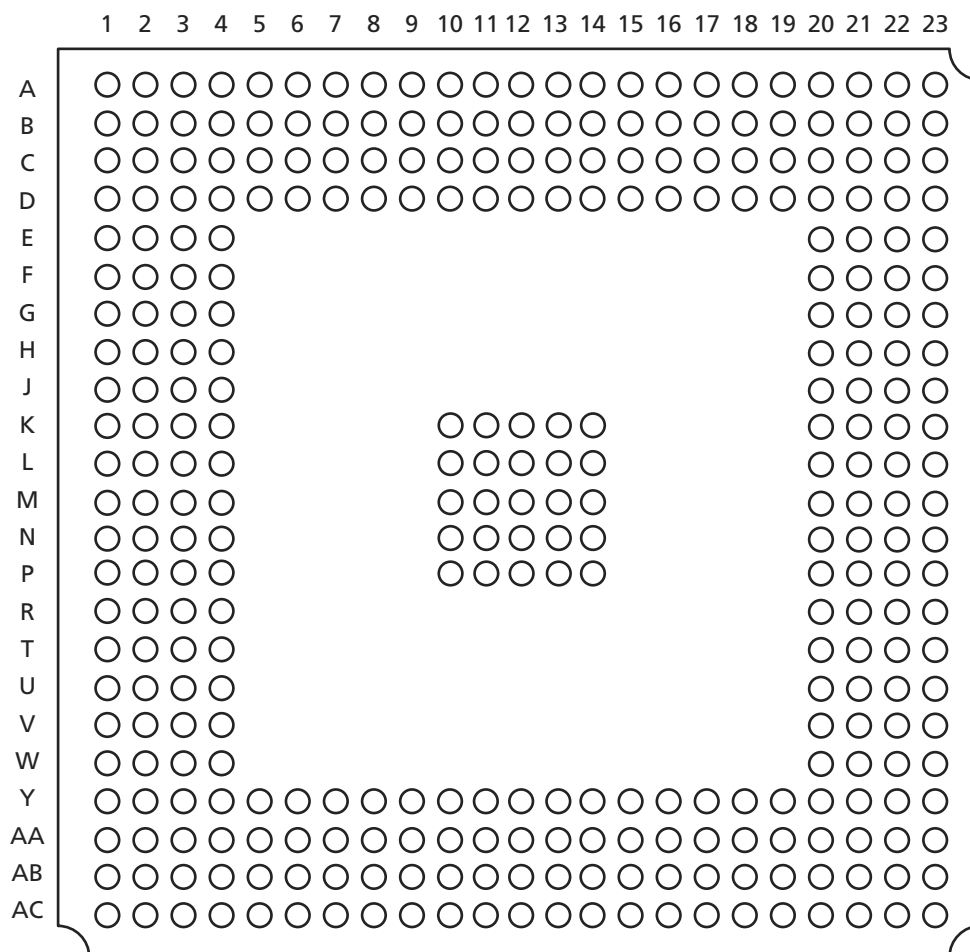


Figure 2-7 • 329-Pin PBGA (Top View)

### Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

# Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v3.2)	Page
v3.1 (June 2003)	The "Ordering Information" was updated to include RoHS information.	1-ii
	The Product Plan was removed since all products have been released.	N/A
	Information concerning the TRST pin in the "Probe Circuit Control Pins" section was removed.	1-6
	The "Dedicated Test Mode" section is new.	1-6
	The "Programming" section is new.	1-7
	A note was added to the "Power-Up Sequencing" table.	1-15
	A note was added to the "Power-Down Sequencing" table. The 3.3 V comments were updated for the following devices: A54SX08, A54SX16, A54SX32.	1-15
	U11 and U13 were added to the "313-Pin PBGA" table.	2-17
v3.0.1	Storage temperature in Table 1-3 was updated.	1-7
	Table 1-1 was updated.	1-5

## Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

### Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

### Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

### Unmarked (production)

This datasheet version contains information that is considered to be final.

### Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

## International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

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