Microchip Technology - A54SX32-PQG208 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	174
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-pqg208

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Ordering Information

A54SX16 – P 2 PQ G 208

Application (Temperature Range)
Blank = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
PP = Pre-production

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
BG = Ball Grid Array
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flat Pack
TQ = Thin (1.4 mm) Quad Flat Pack
VQ = Very Thin (1.0 mm) Quad Flat Pack
FG = Fine Pitch Ball Grid Array (1.0 mm)

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% Faster than Standard
–2 = Approximately 25% Faster than Standard
–3 = Approximately 35% Faster than Standard

Blank = Not PCI Compliant
P = PCI Compliant

Part Number
A54SX08 = 12,000 System Gates
A54SX16 = 24,000 System Gates
A54SX16P = 24,000 System Gates
A54SX32 = 48,000 System Gates

Plastic Device Resources

Device	**User I/Os (including clock buffers)**							
	PLCC 84-Pin	**VQFP 100-Pin**	**PQFP 208-Pin**	**TQFP 144-Pin**	**TQFP 176-Pin**	**PBGA 313-Pin**	**PBGA 329-Pin**	**FBGA 144-Pin**
A54SX08	69	81	130	113	128	–	–	111
A54SX16	–	81	175	–	147	–	–	–
A54SX16P	–	81	175	113	147	–	–	–
A54SX32	–	–	174	113	147	249	249	–

Note: *Package Definitions (Consult your local Actel sales representative for product availability):*
PLCC = Plastic Leaded Chip Carrier
PQFP = Plastic Quad Flat Pack
TQFP = Thin Quad Flat Pack
VQFP = Very Thin Quad Flat Pack
PBGA = Plastic Ball Grid Array
FBGA = Fine Pitch (1.0 mm) Ball Grid Array

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.

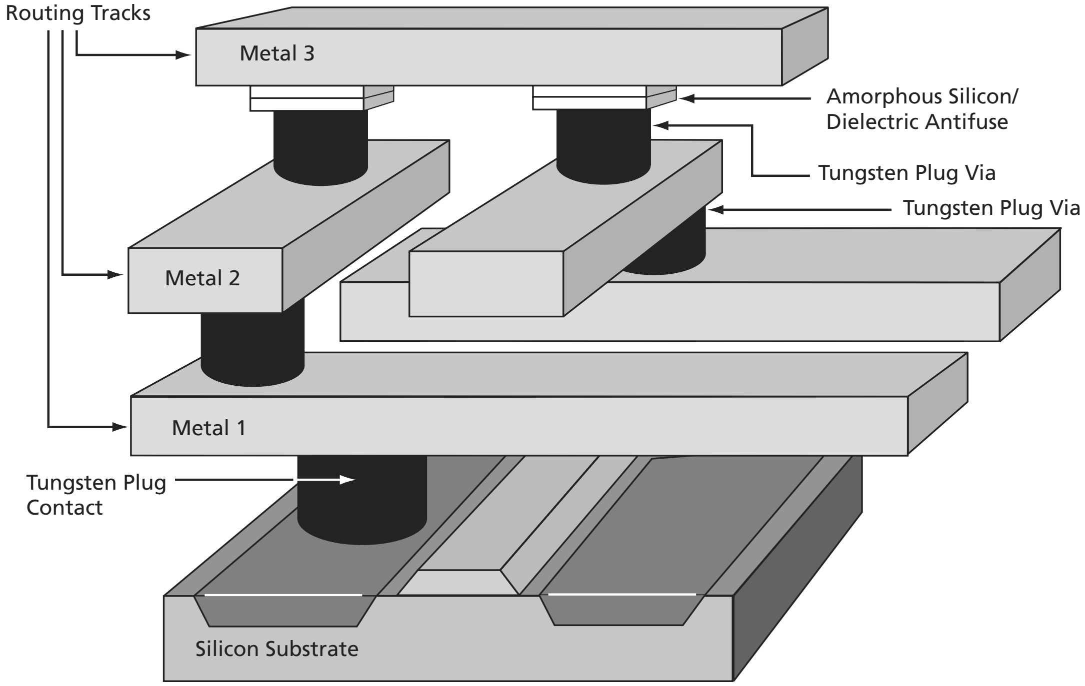

Figure 1-1 • **SX Family Interconnect Elements**

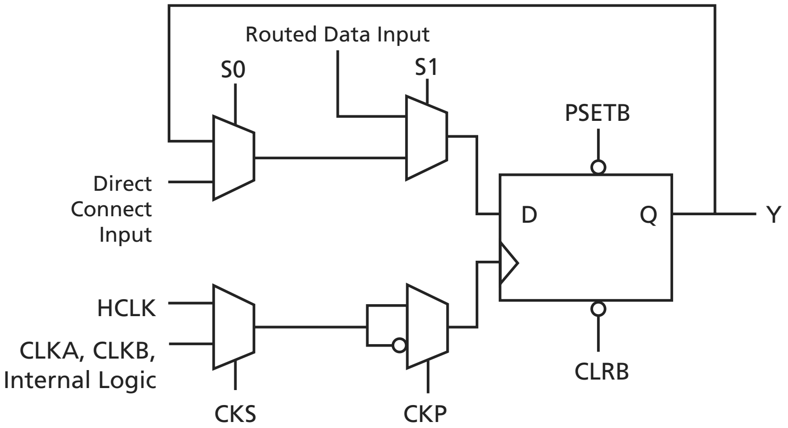

Figure 1-2 • **R-Cell**

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

Table 1-4 • **Recommended Operating Conditions**

Parameter	**Commercial**	**Industrial**	**Military**	**Units**
Temperature Range*	0 to + 70	–40 to + 85	–55 to +125	°C
3.3 V Power Supply Tolerance	±10	±10	±10	%V_{CC}
5.0 V Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note: **Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Table 1-5 • **Electrical Specifications**

		Commercial		**Industrial**		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{OH}	(I_{OH} = –20 µA) (CMOS) (I_{OH} = –8 mA) (TTL) (I_{OH} = –6 mA) (TTL)	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	V
V_{OL}	(I_{OL}= 20 µA) (CMOS) (I_{OL} = 12 mA) (TTL) (I_{OL} = 8 mA) (TTL)		0.10 0.50		 0.50	V
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		4.0	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See "Evaluating Power in SX Devices" on page 1-16.				

A54SX16P AC Specifications for (PCI Operation)

Table 1-7 • **A54SX16P AC Specifications for (PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 1.4$[1]	–44		mA
		$1.4 \le V_{OUT} < 2.4$[1, 2]	$-44 + (V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}$[1, 3]		EQ 1-1 on page 1-11	
	(Test Point)	$V_{OUT} = 3.1$[3]		–142	mA
$I_{OL(AC)}$	Switching Current High	$V_{OUT} \ge 2.2$[1]	95		mA
		$2.2 > V_{OUT} > 0.55$[1]	$V_{OUT}/0.023$		
		$0.71 > V_{OUT} > 0$[1, 3]		EQ 1-2 on page 1-11	mA
	(Test Point)	$V_{OUT} = 0.71$[3]		206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load[4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load[4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 1-9 on page 1-11. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half-size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 1-9 on page 1-11. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*

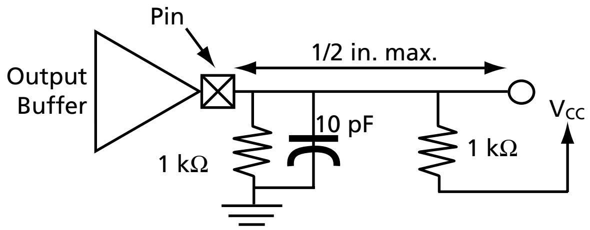

Figure 1-9 shows the 5.0 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

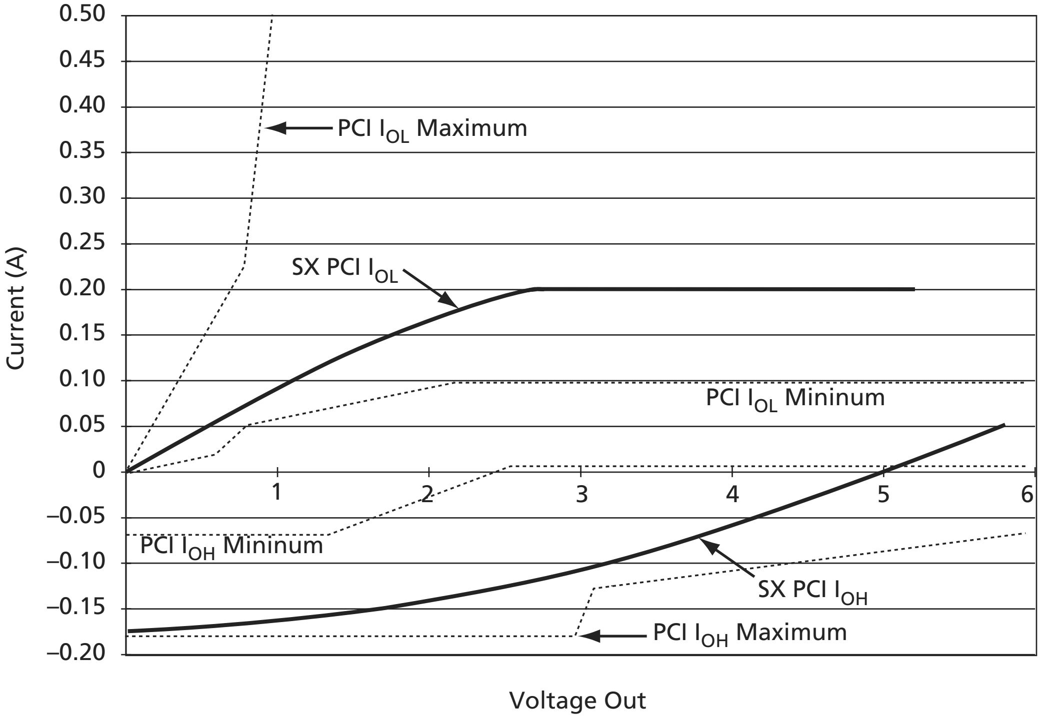

Figure 1-9 • **5.0 V PCI Curve for A54SX16P Device**

$I_{OH} = 11.9 \times (V_{OUT} - 5.25) \times (V_{OUT} + 2.45)$

for $V_{CC} > V_{OUT} > 3.1\ V$

EQ 1-1

$I_{OL} = 78.5 \times V_{OUT} \times (4.4 - V_{OUT})$

for $0\ V < V_{OUT} < 0.71\ V$

EQ 1-2

Figure 1-10 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

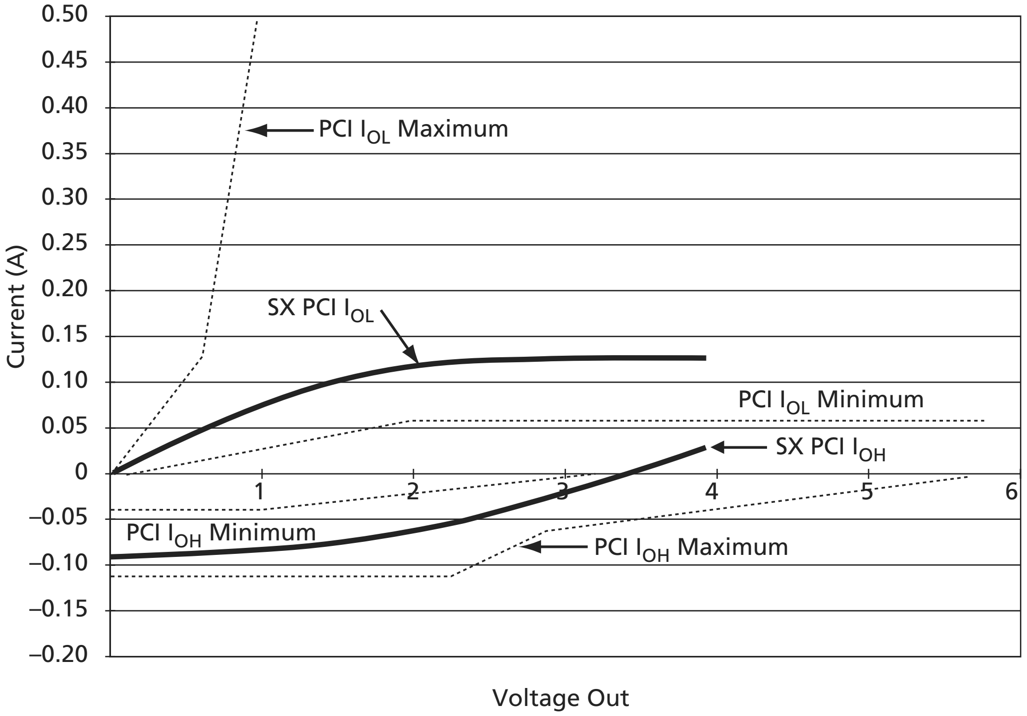

Figure 1-10 • **3.3 V PCI Curve for A54SX16P Device**

$I_{OH} = (98.0/V_{CC}) \times (V_{OUT} - V_{CC}) \times (V_{OUT} + 0.4V_{CC})$

for $V_{CC} > V_{OUT} > 0.7\ V_{CC}$

EQ 1-3

$I_{OL} = (256/V_{CC}) \times V_{OUT} \times (V_{CC} - V_{OUT})$

for $0\ V < V_{OUT} < 0.18\ V_{CC}$

EQ 1-4

Table 1-13 shows capacitance values for various devices.

Table 1-13 • **Capacitance Values for Devices**

	A54SX08	A54SX16	A54SX16P	A54SX32
C_{EQM} (pF)	4.0	4.0	4.0	4.0
C_{EQI} (pF)	3.4	3.4	3.4	3.4
C_{EQO} (pF)	4.7	4.7	4.7	4.7
C_{EQCR} (pF)	1.6	1.6	1.6	1.6
C_{EQHV}	0.615	0.615	0.615	0.615
C_{EQHF}	60	96	96	140
r_1 (pF)	87	138	138	171
r_2 (pF)	87	138	138	171

Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A54SX16P device. A pattern of 0101… was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101… caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

Table 1-14 • **Power Consumption Guidelines**

Description	Power Consumption Guideline
Logic Modules (m)	20% of modules
Inputs Switching (n)	# inputs/4
Outputs Switching (p)	# outputs/4
First Routed Array Clock Loads (q_1)	20% of register cells
Second Routed Array Clock Loads (q_2)	20% of register cells
Load Capacitance (C_L)	35 pF
Average Logic Module Switching Rate (f_m)	f/10
Average Input Switching Rate (f_n)	f/5
Average Output Switching Rate (f_p)	f/10
Average First Routed Array Clock Rate (f_{q1})	f/2
Average Second Routed Array Clock Rate (f_{q2})	f/2
Average Dedicated Array Clock Rate (f_{s1})	f
Dedicated Clock Array Clock Loads (s_1)	20% of regular modules

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{Total} = P_{AC} \text{ (dynamic power)} + P_{DC} \text{ (static power)}$$

EQ 1-9

AC Power Dissipation

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

EQ 1-10

$$\begin{aligned}P_{AC} = V_{CCA}^2 \times [&(m \times C_{EQM} \times f_m)_{Module} + \\ &(n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + \\ &(0.5\,(q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + \\ &(0.5\,(q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2}))_{RCLKB} + \\ &(0.5\,(s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]\end{aligned}$$

EQ 1-11

Table 1-15 • **Package Thermal Characteristics**

Package Type	**Pin Count**	θ_{jc}	θ_{ja} **Still Air**	θ_{ja} **300 ft/min.**	**Units**
Plastic Leaded Chip Carrier (PLCC)	84	12	32	22	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Very Thin Quad Flatpack (VQFP)	100	10	38	32	°C/W
Plastic Quad Flat Pack (PQFP) without Heat Spreader	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	14.5	°C/W
Plastic Ball Grid Array (PBGA)	313	3	23	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W

Note: *SX08 does not have a heat spreader.*

Table 1-16 • **Temperature and Voltage Derating Factors***

	Junction Temperature						
V_{CCA}	**–55**	**–40**	**0**	**25**	**70**	**85**	**125**
3.0	0.75	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.70	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.66	0.69	0.77	0.78	0.87	0.92	1.02

Note: **Normalized to worst-case commercial, T_J = 70°C, V_{CCA} = 3.0 V*

A54SX08 Timing Characteristics

Table 1-17 • **A54SX08 Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Input Module Predicted Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + $t_{PDn,}$ or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

Table 1-17 • **A54SX08 Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (pad to R-Cell input)		1.0		1.1		1.3		1.5	ns
t_{HCKL}	Input HIGH to LOW (pad to R-Cell input)		1.0		1.2		1.4		1.6	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.1		0.2		0.2		0.2	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)		1.3		1.5		1.7		2.0	ns
t_{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell Input)		1.4		1.6		1.8		2.1	ns
t_{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)		1.4		1.7		1.9		2.2	ns
t_{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)		1.5		1.7		2.0		2.3	ns
t_{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)		1.5		1.7		1.9		2.2	ns
t_{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)		1.5		1.8		2.0		2.3	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (light load)		0.1		0.2		0.2		0.2	ns
t_{RCKSW}	Maximum Skew (50% load)		0.3		0.3		0.4		0.4	ns
t_{RCKSW}	Maximum Skew (100% load)		0.3		0.3		0.4		0.4	ns
TTL Output Module Timing1										
t_{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

Table 1-18 • **A54SX16 Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (pad to R-Cell input)		1.2		1.4		1.5		1.8	ns
t_{HCKL}	Input HIGH to LOW (pad to R-Cell input)		1.2		1.4		1.6		1.9	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.3		0.3	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)		1.6		1.8		2.1		2.5	ns
t_{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell input)		1.8		2.0		2.3		2.7	ns
t_{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)		1.8		2.1		2.5		2.8	ns
t_{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)		2.0		2.2		2.5		3.0	ns
t_{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)		1.8		2.1		2.4		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)		2.0		2.2		2.5		3.0	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (light load)		0.5		0.5		0.5		0.7	ns
t_{RCKSW}	Maximum Skew (50% load)		0.5		0.6		0.7		0.8	ns
t_{RCKSW}	Maximum Skew (100% load)		0.5		0.6		0.7		0.8	ns
TTL Output Module Timing[3]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH}, the loading is 5 pF.*

Table 1-19 • **A54SX16P Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL/PCI Output Module Timing										
t_{DLH}	Data-to-Pad LOW to HIGH		1.5		1.7		2.0		2.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.9		2.2		2.4		2.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.3		2.6		3.0		3.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.5		1.7		1.9		2.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.7		3.1		3.5		4.1	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.7		4.4	ns
PCI Output Module Timing[3]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.8		2.0		2.3		2.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.7		2.0		2.2		2.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		0.8		1.0		1.1		1.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.2		1.2		1.5		1.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.0		1.1		1.3		1.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.1		1.3		1.5		1.7	ns
TTL Output Module Timing										
t_{DLH}	Data-to-Pad LOW to HIGH		2.1		2.5		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.0		2.3		2.6		3.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		2.9		3.2		3.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.0		3.5		3.9		4.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.3		2.7		3.1		3.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.7		4.4	ns

Note:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 10 pF loading.*

A54SX32 Timing Characteristics

Table 1-20 • **A54SX32 Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{RD3}	FO = 3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD4}	FO = 4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{RD8}	FO = 8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{RD12}	FO = 12 Routing Delay		4.0		4.7		5.3		6.2	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{IRD3}	FO = 3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD4}	FO = 4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{IRD8}	FO = 8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{IRD12}	FO = 12 Routing Delay		4.0		4.7		5.3		6.2	ns

Note:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.*

Pin Description

CLKA/B **Clock A and B**

These pins are 3.3 V / 5.0 V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as bidirectional.)

GND **Ground**

LOW supply voltage.

HCLK **Dedicated (hardwired) Array Clock**

This pin is the 3.3 V / 5.0 V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3 V PCI or 5.0 V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC **No Connection**

This pin is not connected to circuitry within the device.

PRA, I/O **Probe A**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality.

PRB, I/O **Probe B**

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK **Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the “logic reset” state.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-2 on page 1-6). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

V_{CCI} **Supply Voltage**

Supply voltage for I/Os. See Table 1-1 on page 1-5.

V_{CCA} **Supply Voltage**

Supply voltage for Array. See Table 1-1 on page 1-5.

V_{CCR} **Supply Voltage**

Supply voltage for input tolerance (required for internal biasing). See Table 1-1 on page 1-5.

Package Pin Assignments

84-Pin PLCC

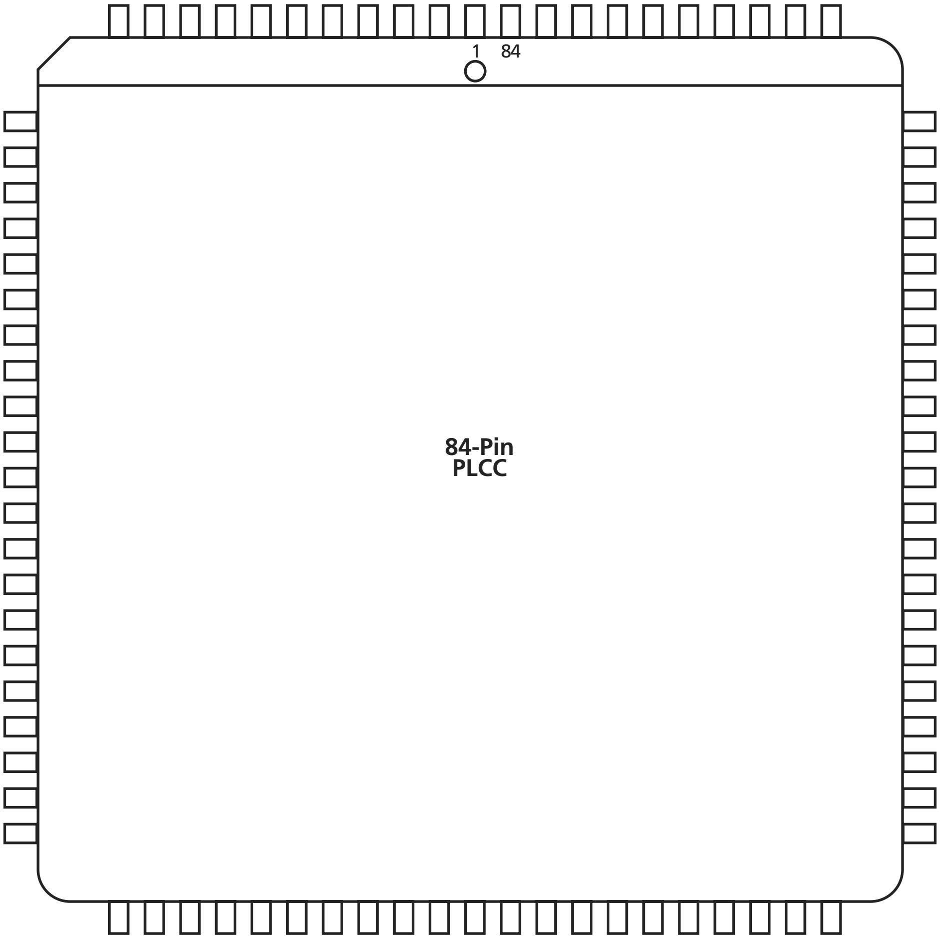

Figure 2-1 • **84-Pin PLCC (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	NC	I/O	I/O
5	I/O	I/O	I/O
6	NC	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	I/O	I/O	I/O
11	TMS	TMS	TMS
12	V_{CCI}	V_{CCI}	V_{CCI}
13	I/O	I/O	I/O
14	NC	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	NC	I/O	I/O
24	I/O	I/O	I/O
25	V_{CCR}	V_{CCR}	V_{CCR}
26	GND	GND	GND
27	V_{CCA}	V_{CCA}	V_{CCA}
28	GND	GND	GND
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	NC	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	I/O	I/O
36	I/O	I/O	I/O

208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	NC	I/O	I/O
40	V_{CCI}	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}	V_{CCA}
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	NC	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	I/O	I/O	I/O
52	GND	GND	GND
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65*	I/O	I/O	NC*
66	I/O	I/O	I/O
67	NC	I/O	I/O
68	I/O	I/O	I/O
69	I/O	I/O	I/O
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O

Note: ** Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

176-Pin TQFP

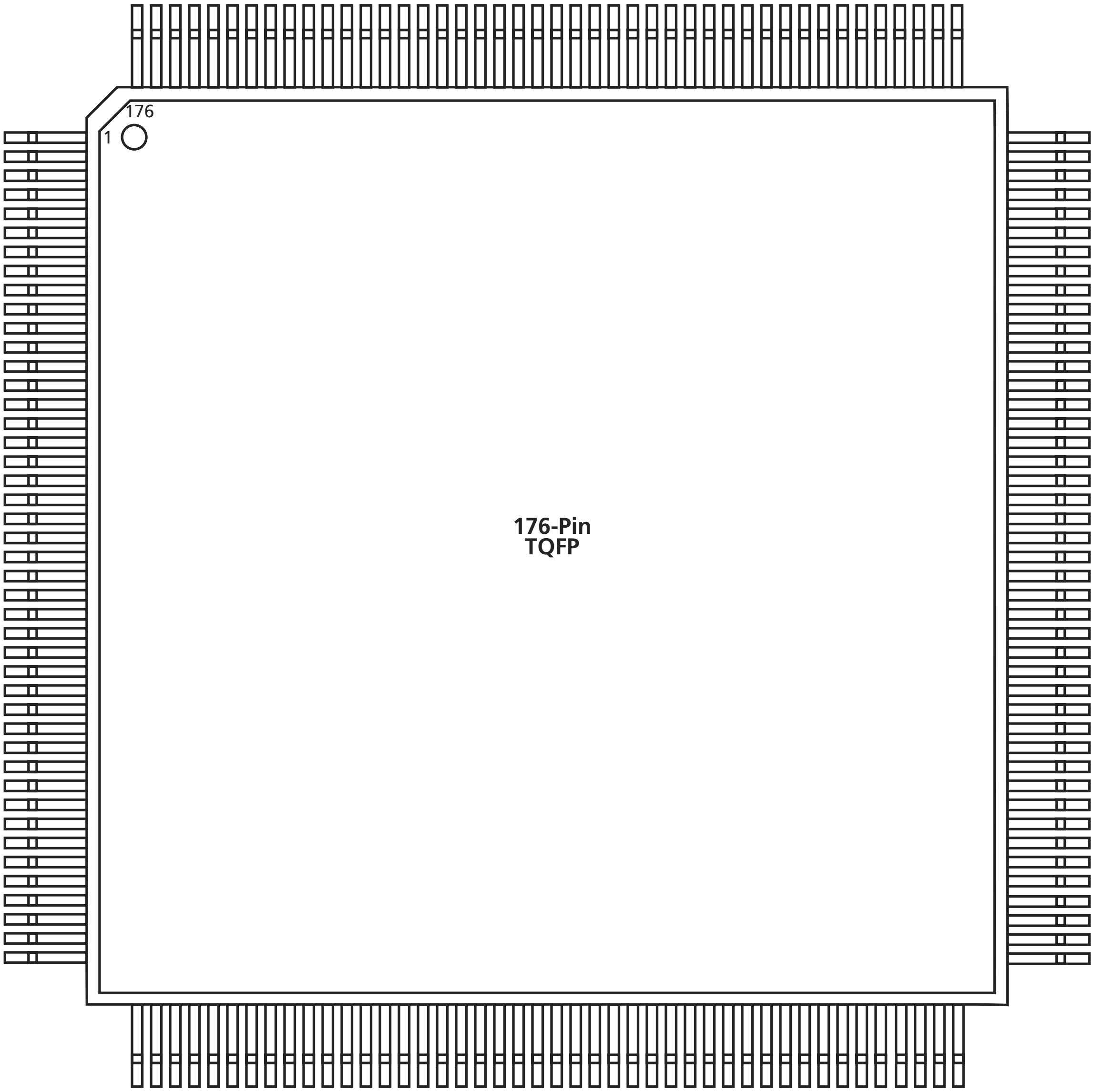

Figure 2-4 • **176-Pin TQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin FBGA	
Pin Number	**A54SX08 Function**
A1	I/O
A2	I/O
A3	I/O
A4	I/O
A5	V_{CCA}
A6	GND
A7	CLKA
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
B1	I/O
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	CLKB
B8	I/O
B9	I/O
B10	I/O
B11	GND
B12	I/O
C1	I/O
C2	I/O
C3	TCK, I/O
C4	I/O
C5	I/O
C6	PRA, I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O

144-Pin FBGA	
Pin Number	**A54SX08 Function**
D1	I/O
D2	V_{CCI}
D3	TDI, I/O
D4	I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	I/O
E1	I/O
E2	I/O
E3	I/O
E4	I/O
E5	TMS
E6	V_{CCI}
E7	V_{CCI}
E8	V_{CCI}
E9	V_{CCA}
E10	I/O
E11	GND
E12	I/O
F1	I/O
F2	I/O
F3	V_{CCR}
F4	I/O
F5	GND
F6	GND
F7	GND
F8	V_{CCI}
F9	I/O
F10	GND
F11	I/O
F12	I/O

144-Pin FBGA	
Pin Number	**A54SX08 Function**
G1	I/O
G2	GND
G3	I/O
G4	I/O
G5	GND
G6	GND
G7	GND
G8	V_{CCI}
G9	I/O
G10	I/O
G11	I/O
G12	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H5	V_{CCA}
H6	V_{CCA}
H7	V_{CCI}
H8	V_{CCI}
H9	V_{CCA}
H10	I/O
H11	I/O
H12	V_{CCR}
J1	I/O
J2	I/O
J3	I/O
J4	I/O
J5	I/O
J6	PRB, I/O
J7	I/O
J8	I/O
J9	I/O
J10	I/O
J11	I/O
J12	V_{CCA}

144-Pin FBGA	
Pin Number	**A54SX08 Function**
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K5	I/O
K6	I/O
K7	GND
K8	I/O
K9	I/O
K10	GND
K11	I/O
K12	I/O
L1	GND
L2	I/O
L3	I/O
L4	I/O
L5	I/O
L6	I/O
L7	HCLK
L8	I/O
L9	I/O
L10	I/O
L11	I/O
L12	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M5	I/O
M6	I/O
M7	V_{CCA}
M8	I/O
M9	I/O
M10	I/O
M11	TDO, I/O
M12	I/O

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