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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	113
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32-tqg144

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

The Actel high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hardwired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

Other Architectural Features

Technology

The Actel SX family is implemented on a high-voltage twin-well CMOS process using 0.35 μ design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25 Ω with a capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin.

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

Power Requirements

The SX family supports 3.3 V operation and is designed to tolerate 5.0 V inputs. (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest power architecture on the market.

Table 1-1 • **Supply Voltages**

Device	V_{CCA}	V_{CCI}	V_{CCR}	Maximum Input Tolerance	Maximum Output Drive
A54SX08 A54SX16 A54SX32	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
A54SX16-P*	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V

Note: **A54SX16-P has three different entries because it is capable of both a 3.3 V and a 5.0 V drive.*

Table 1-4 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to + 70	–40 to + 85	–55 to +125	°C
3.3 V Power Supply Tolerance	±10	±10	±10	$\%V_{CC}$
5.0 V Power Supply Tolerance	±5	±10	±10	$\%V_{CC}$

Note: **Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Table 1-5 • **Electrical Specifications**

		Commercial		Industrial		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{OH}	(I_{OH} = –20 µA) (CMOS) (I_{OH} = –8 mA) (TTL) (I_{OH} = –6 mA) (TTL)	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	V
V_{OL}	(I_{OL}= 20 µA) (CMOS) (I_{OL} = 12 mA) (TTL) (I_{OL} = 8 mA) (TTL)		0.10 0.50		 0.50	V
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		4.0	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See "Evaluating Power in SX Devices" on page 1-16.				

Figure 1-9 shows the 5.0 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

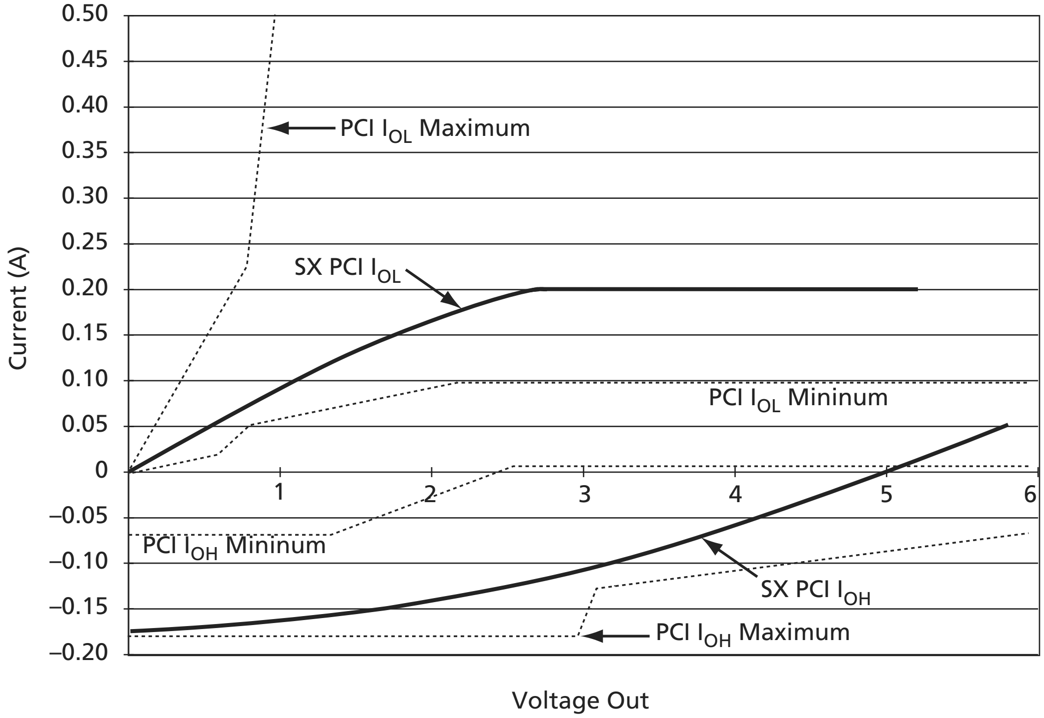


Figure 1-9 • **5.0 V PCI Curve for A54SX16P Device**

$I_{OH} = 11.9 \times (V_{OUT} - 5.25) \times (V_{OUT} + 2.45)$

for $V_{CC} > V_{OUT} > 3.1$ V

EQ 1-1

$I_{OL} = 78.5 \times V_{OUT} \times (4.4 - V_{OUT})$

for $0 \text{ V} < V_{OUT} < 0.71$ V

EQ 1-2

A54SX16P AC Specifications (3.3 V PCI Operation)

Table 1-9 • **A54SX16P AC Specifications (3.3 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CC}$ [1]			mA
		$0.3V_{CC} \leq V_{OUT} < 0.9V_{CC}$ [1]	$-12V_{CC}$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}$ [1, 2]	$-17.1 + (V_{CC} - V_{OUT})$	EQ 1-3 on page 1-14	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$ [2]		$-32V_{CC}$	mA
$I_{OL(AC)}$	Switching Current High	$V_{CC} > V_{OUT} \geq 0.6V_{CC}$ [1]			mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}$ [1]	$16V_{CC}$		mA
		$0.18V_{CC} > V_{OUT} > 0$ [1, 2]	$26.7V_{OUT}$	EQ 1-4 on page 1-14	mA
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ [2]		$38V_{CC}$	
I_{CL}	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$-3 < V_{IN} \leq -1$	$25 + (V_{IN} - V_{OUT} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate[3]	$0.2V_{CC}$ to $0.6V_{CC}$ load	1	4	V/ns
$slew_F$	Output Fall Slew Rate[3]	$0.6V_{CC}$ to $0.2V_{CC}$ load	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*

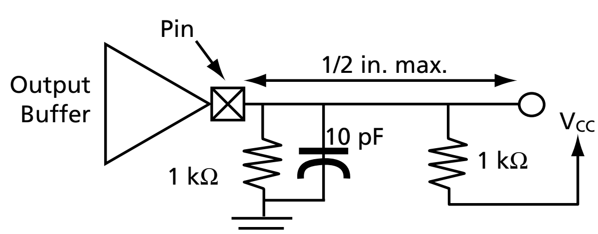


Figure 1-10 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

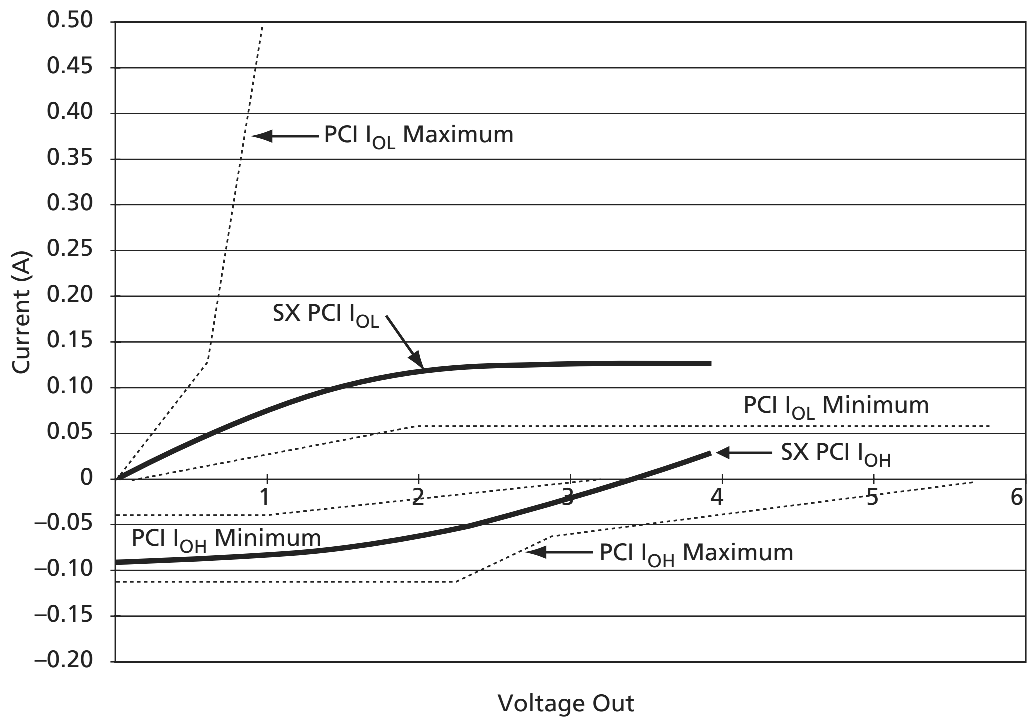


Figure 1-10 • **3.3 V PCI Curve for A54SX16P Device**

$$I_{OH} = (98.0/V_{CC}) \times (V_{OUT} - V_{CC}) \times (V_{OUT} + 0.4V_{CC})$$

for $V_{CC} > V_{OUT} > 0.7\ V_{CC}$

EQ 1-3

$$I_{OL} = (256/V_{CC}) \times V_{OUT} \times (V_{CC} - V_{OUT})$$

for $0\ V < V_{OUT} < 0.18\ V_{CC}$

EQ 1-4

Step 1: Define Terms Used in Formula

	V_{CCA}	3.3
Module		
Number of logic modules switching at f_m (Used 50%)	m	264
Average logic modules switching rate f_m (MHz) (Guidelines: f/10)	f_m	20
Module capacitance C_{EQM} (pF)	C_{EQM}	4.0
Input Buffer		
Number of input buffers switching at f_n	n	1
Average input switching rate f_n (MHz) (Guidelines: f/5)	f_n	40
Input buffer capacitance C_{EQI} (pF)	C_{EQI}	3.4
Output Buffer		
Number of output buffers switching at f_p	p	1
Average output buffers switching rate f_p(MHz) (Guidelines: f/10)	f_p	20
Output buffers buffer capacitance C_{EQO} (pF)	C_{EQO}	4.7
Output Load capacitance C_L (pF)	C_L	35
RCLKA		
Number of Clock loads q_1	q_1	528
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q1}	200
Fixed capacitance (pF)	r_1	138
RCLKB		
Number of Clock loads q_2	q_2	0
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q2}	0
Fixed capacitance (pF)	r_2	138
HCLK		
Number of Clock loads	s_1	0
Variable capacitance of dedicated array clock (pF)	C_{EQHV}	0.615
Fixed capacitance of dedicated array clock (pF)	C_{EQHF}	96
Average clock rate (MHz)	f_{s1}	0

Step 2: Calculate Dynamic Power Consumption

$V_{CCA} \times V_{CCA}$	10.89
$m \times f_m \times C_{EQM}$	0.02112
$n \times f_n \times C_{EQI}$	0.000136
$p \times f_p \times (C_{EQO}+C_L)$	0.000794
$0.5\ (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1})$	0.11208
$0.5(q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2})$	0
$0.5\ (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1})$	0

$P_{AC} = 1.461$ W

Step 3: Calculate DC Power Dissipation

DC Power Dissipation

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + X \times V_{OL} \times I_{OL} + Y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-12

For a rough estimate of DC Power Dissipation, only use $P_{DC} = (I_{standby}) \times V_{CCA}$. The rest of the formula provides a very small number that can be considered negligible.

$P_{DC} = (I_{standby}) \times V_{CCA}$

$P_{DC} = .55\text{ mA} \times 3.3\text{ V}$

$P_{DC} = 0.001815$ W

Step 4: Calculate Total Power Consumption

$P_{Total} = P_{AC} + P_{DC}$

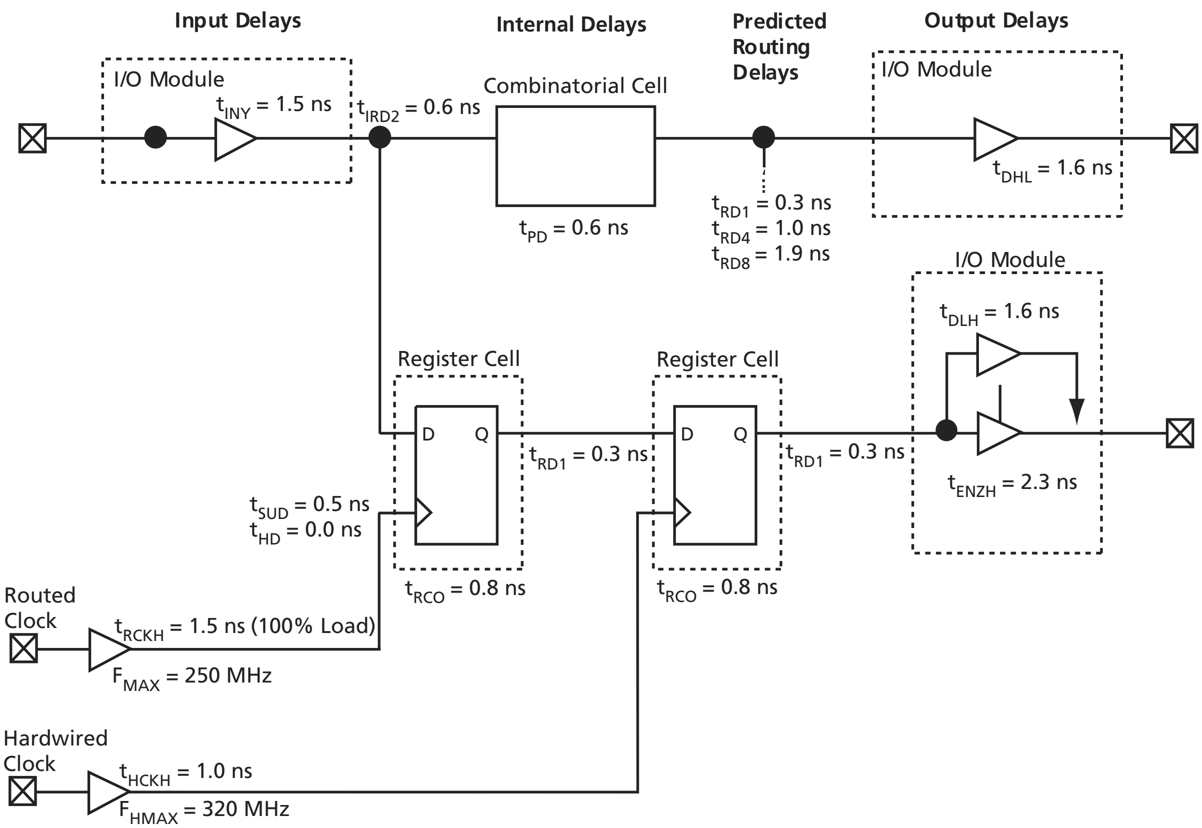
$P_{Total} = 1.461 + 0.001815$

$P_{Total} = 1.4628$ W

Step 5: Compare Estimated Power Consumption against Characterized Power Consumption

The estimated total power consumption for this design is 1.46 W. The characterized power consumption for this design at 200 MHz is 1.0164 W.

SX Timing Model



Note: *Values shown for A54SX08-3, worst-case commercial conditions.*

Figure 1-12 • **SX Timing Model**

Hardwired Clock

External Setup = $t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH}$

= 1.5 + 0.3 + 0.5 – 1.0 = 1.3 ns

EQ 1-15

Clock-to-Out (Pin-to-Pin)

= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.0 + 0.8 + 0.3 + 1.6 = 3.7 ns

EQ 1-16

Routed Clock

External Setup = $t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH}$

= 1.5 + 0.3 + 0.5 – 1.5 = 0.8 ns

EQ 1-17

Clock-to-Out (Pin-to-Pin)

= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.52+ 0.8 + 0.3 + 1.6 = 4.2 ns

EQ 1-18

Table 1-17 • **A54SX08 Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (pad to R-Cell input)		1.0		1.1		1.3		1.5	ns
t_{HCKL}	Input HIGH to LOW (pad to R-Cell input)		1.0		1.2		1.4		1.6	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.1		0.2		0.2		0.2	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)		1.3		1.5		1.7		2.0	ns
t_{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell Input)		1.4		1.6		1.8		2.1	ns
t_{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)		1.4		1.7		1.9		2.2	ns
t_{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)		1.5		1.7		2.0		2.3	ns
t_{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)		1.5		1.7		1.9		2.2	ns
t_{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)		1.5		1.8		2.0		2.3	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (light load)		0.1		0.2		0.2		0.2	ns
t_{RCKSW}	Maximum Skew (50% load)		0.3		0.3		0.4		0.4	ns
t_{RCKSW}	Maximum Skew (100% load)		0.3		0.3		0.4		0.4	ns
TTL Output Module Timing1										
t_{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns

Note:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics (Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH}, the loading is 5 pF.*

Table 1-18 • **A54SX16 Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (pad to R-Cell input)		1.2		1.4		1.5		1.8	ns
t_{HCKL}	Input HIGH to LOW (pad to R-Cell input)		1.2		1.4		1.6		1.9	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.3		0.3	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)		1.6		1.8		2.1		2.5	ns
t_{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell input)		1.8		2.0		2.3		2.7	ns
t_{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)		1.8		2.1		2.5		2.8	ns
t_{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)		2.0		2.2		2.5		3.0	ns
t_{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)		1.8		2.1		2.4		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)		2.0		2.2		2.5		3.0	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (light load)		0.5		0.5		0.5		0.7	ns
t_{RCKSW}	Maximum Skew (50% load)		0.5		0.6		0.7		0.8	ns
t_{RCKSW}	Maximum Skew (100% load)		0.5		0.6		0.7		0.8	ns
TTL Output Module Timing[3]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH}, the loading is 5 pF.*

Table 1-19 • **A54SX16P Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL/PCI Output Module Timing										
t_{DLH}	Data-to-Pad LOW to HIGH		1.5		1.7		2.0		2.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.9		2.2		2.4		2.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.3		2.6		3.0		3.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.5		1.7		1.9		2.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.7		3.1		3.5		4.1	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.7		4.4	ns
PCI Output Module Timing[3]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.8		2.0		2.3		2.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.7		2.0		2.2		2.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		0.8		1.0		1.1		1.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.2		1.2		1.5		1.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.0		1.1		1.3		1.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.1		1.3		1.5		1.7	ns
TTL Output Module Timing										
t_{DLH}	Data-to-Pad LOW to HIGH		2.1		2.5		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.0		2.3		2.6		3.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		2.9		3.2		3.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.0		3.5		3.9		4.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.3		2.7		3.1		3.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.7		4.4	ns

Note:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 10 pF loading.*

A54SX32 Timing Characteristics

Table 1-20 • **A54SX32 Timing Characteristics (Worst-Case Commercial Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)**

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{RD3}	FO = 3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD4}	FO = 4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{RD8}	FO = 8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{RD12}	FO = 12 Routing Delay		4.0		4.7		5.3		6.2	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{IRD3}	FO = 3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD4}	FO = 4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{IRD8}	FO = 8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{IRD12}	FO = 12 Routing Delay		4.0		4.7		5.3		6.2	ns

Note:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.*

Table 1-20 • **A54SX32 Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Network										
t_{HCKH}	Input LOW to HIGH (pad to R-Cell input)		1.9		2.1		2.4		2.8	ns
t_{HCKL}	Input HIGH to LOW (pad to R-Cell input)		1.9		2.1		2.4		2.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)		2.4		2.7		3.0		3.5	ns
t_{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell input)		2.4		2.7		3.1		3.6	ns
t_{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)		2.7		3.0		3.5		4.1	ns
t_{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)		2.7		3.1		3.6		4.2	ns
t_{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)		2.7		3.1		3.5		4.1	ns
t_{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)		2.8		3.2		3.6		4.3	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (light load)		0.85		0.98		1.1		1.3	ns
t_{RCKSW}	Maximum Skew (50% load)		1.23		1.4		1.6		1.9	ns
t_{RCKSW}	Maximum Skew (100% load)		1.30		1.5		1.7		2.0	ns
TTL Output Module Timing[3]										
t_{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.*

Package Pin Assignments

84-Pin PLCC

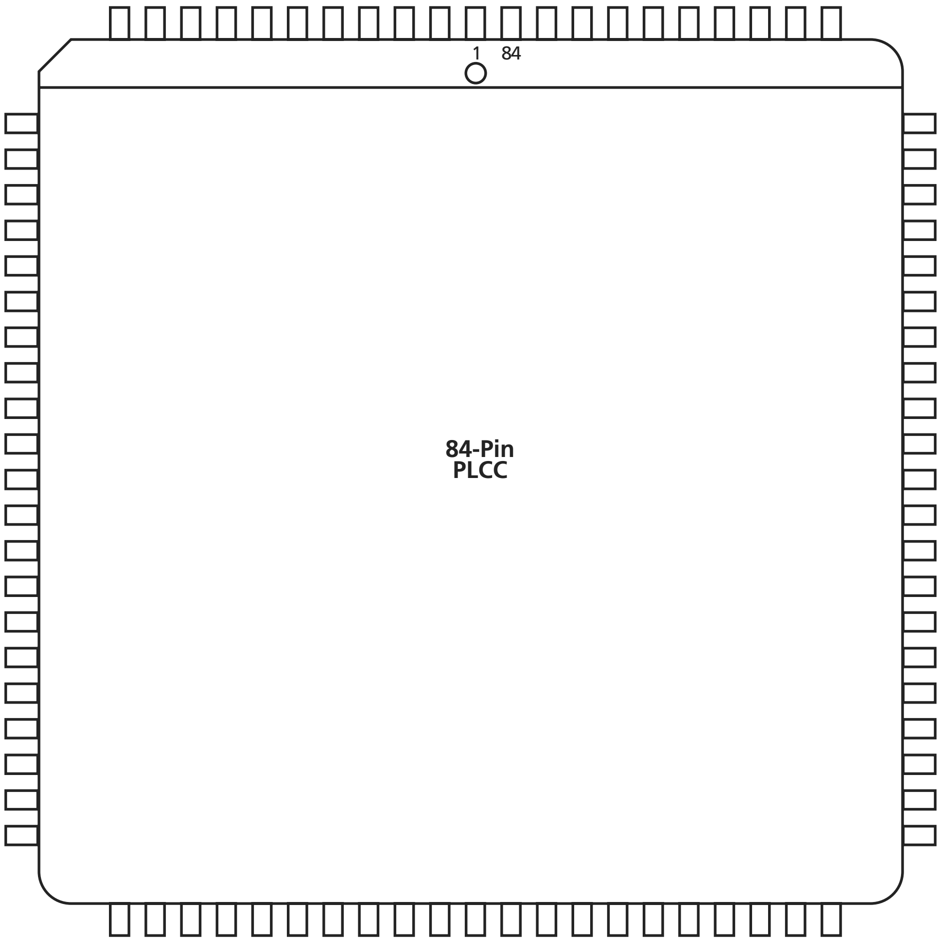


Figure 2-1 • **84-Pin PLCC (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V_{CCI}	V_{CCI}	V_{CCI}
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V_{CCA}	V_{CCA}	V_{CCA}
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V_{CCI}	V_{CCI}	V_{CCI}
33	V_{CCA}	V_{CCA}	V_{CCA}
34	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V_{CCI}	V_{CCI}	V_{CCI}
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V_{CCA}	V_{CCA}	V_{CCA}
67	V_{CCR}	V_{CCR}	V_{CCR}
68	I/O	I/O	I/O

313-Pin PBGA

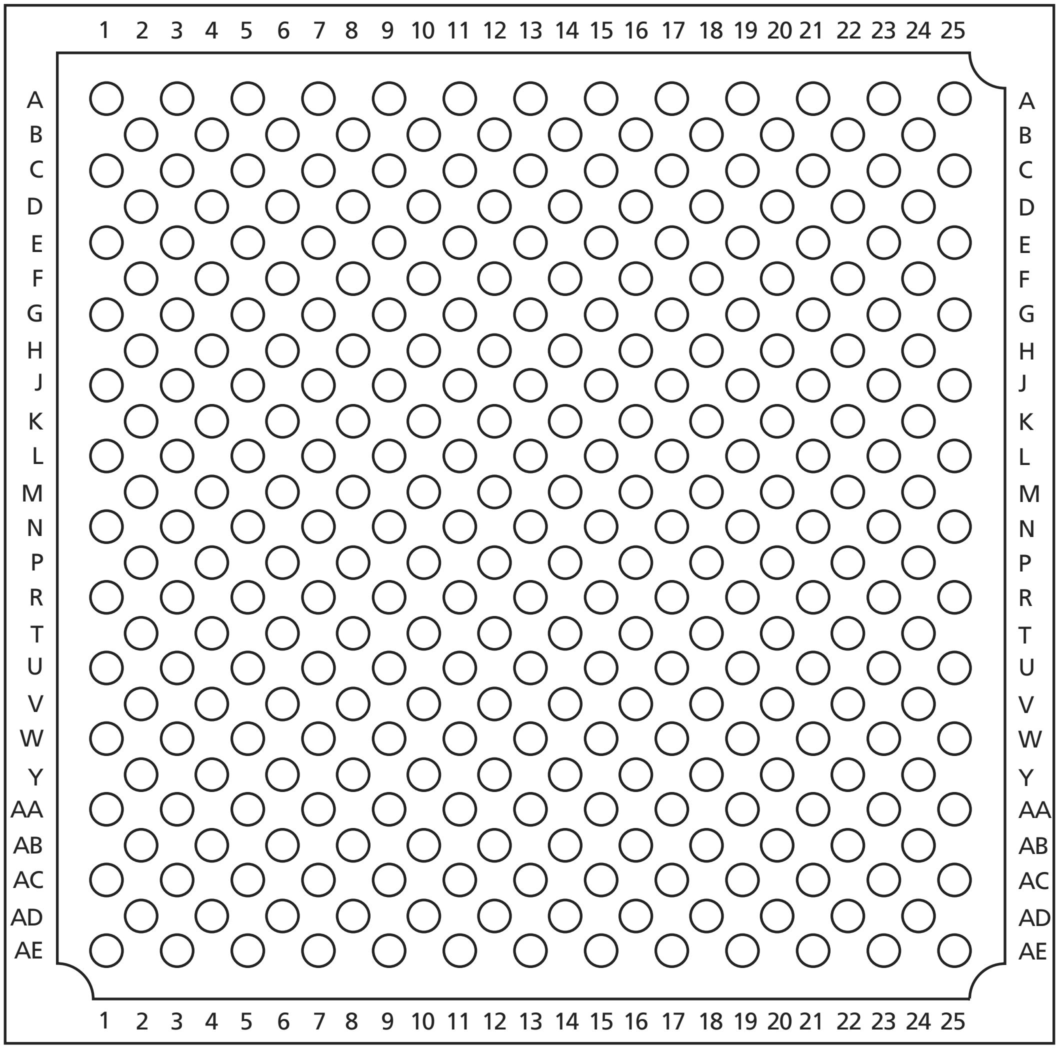


Figure 2-6 • **313-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin FBGA	
Pin Number	A54SX08 Function
A1	I/O
A2	I/O
A3	I/O
A4	I/O
A5	V_{CCA}
A6	GND
A7	CLKA
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
B1	I/O
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	CLKB
B8	I/O
B9	I/O
B10	I/O
B11	GND
B12	I/O
C1	I/O
C2	I/O
C3	TCK, I/O
C4	I/O
C5	I/O
C6	PRA, I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O

144-Pin FBGA	
Pin Number	A54SX08 Function
D1	I/O
D2	V_{CCI}
D3	TDI, I/O
D4	I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	I/O
E1	I/O
E2	I/O
E3	I/O
E4	I/O
E5	TMS
E6	V_{CCI}
E7	V_{CCI}
E8	V_{CCI}
E9	V_{CCA}
E10	I/O
E11	GND
E12	I/O
F1	I/O
F2	I/O
F3	V_{CCR}
F4	I/O
F5	GND
F6	GND
F7	GND
F8	V_{CCI}
F9	I/O
F10	GND
F11	I/O
F12	I/O

144-Pin FBGA	
Pin Number	A54SX08 Function
G1	I/O
G2	GND
G3	I/O
G4	I/O
G5	GND
G6	GND
G7	GND
G8	V_{CCI}
G9	I/O
G10	I/O
G11	I/O
G12	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H5	V_{CCA}
H6	V_{CCA}
H7	V_{CCI}
H8	V_{CCI}
H9	V_{CCA}
H10	I/O
H11	I/O
H12	V_{CCR}
J1	I/O
J2	I/O
J3	I/O
J4	I/O
J5	I/O
J6	PRB, I/O
J7	I/O
J8	I/O
J9	I/O
J10	I/O
J11	I/O
J12	V_{CCA}

144-Pin FBGA	
Pin Number	A54SX08 Function
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K5	I/O
K6	I/O
K7	GND
K8	I/O
K9	I/O
K10	GND
K11	I/O
K12	I/O
L1	GND
L2	I/O
L3	I/O
L4	I/O
L5	I/O
L6	I/O
L7	HCLK
L8	I/O
L9	I/O
L10	I/O
L11	I/O
L12	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M5	I/O
M6	I/O
M7	V_{CCA}
M8	I/O
M9	I/O
M10	I/O
M11	TDO, I/O
M12	I/O

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v3.2)	Page
v3.1 (June 2003)	The "Ordering Information" was updated to include RoHS information.	1-ii
	The Product Plan was removed since all products have been released.	N/A
	Information concerning the TRST pin in the "Probe Circuit Control Pins" section was removed.	1-6
	The "Dedicated Test Mode" section is new.	1-6
	The "Programming" section is new.	1-7
	A note was added to the "Power-Up Sequencing" table.	1-15
	A note was added to the "Power-Down Sequencing" table. The 3.3 V comments were updated for the following devices: A54SX08, A54SX16, A54SX32.	1-15
	U11 and U13 were added to the "313-Pin PBGA" table.	2-17
v3.0.1	Storage temperature in Table 1-3 was updated.	1-7
	Table 1-1 was updated.	1-5

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

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