Renesas Electronics America Inc - R5F364A6DFA#U0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f364a6dfa-u0

Table 1.2 Specifications for the 100-Pin Package (2/2)

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer functions	• Three-phase inverter control (timer A1, timer A2, timer A4, timer B2) • On-chip dead time timer
	Real-time clock	Count: seconds, minutes, hours, days of the week
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit only) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5 to UART7	Clock synchronous/asynchronous × 6 channels I^2C-bus, IEBus, special mode 2 SIM (UART2)
	SI/O3, SI/O4	Clock synchronization only × 2 channels
Multi-master I^2C-bus Interface		1 channel
CEC Functions (2)		CEC transmit/receive, arbitration lost detection, ACK automatic output, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		• Program and erase power supply voltage: 2.7 to 5.5 V • Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		25 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		Described in Electrical Characteristics
Operating Temperature		-20°C to 85°C, -40°C to 85°C (1)
Package		100-pin QFP: PRQP0100JD-B (Previous package code: 100P6F-A) 100-pin LQFP: PLQP0100KB-A (Previous package code: 100P6Q-A)

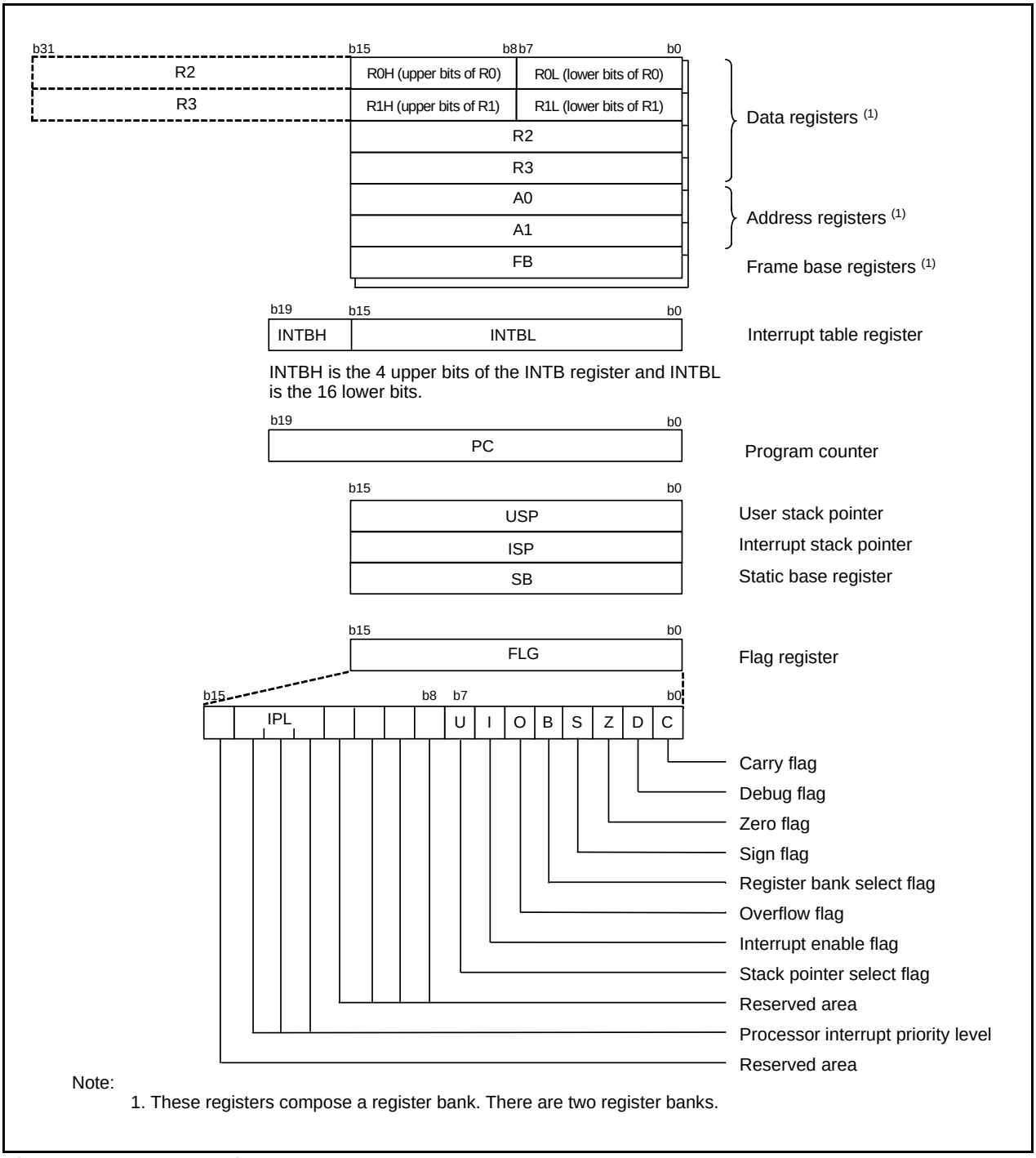
Notes:
1. See Table 1.3 “Product List” for the operating temperature.
2. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

Table 1.4 Pin Names for the 100-Pin Package (1/2)

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
1	99		P9_6			SOUT4	ANEX1	
2	100		P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN/PWM1		DA1	
4	2		P9_3		TB3IN/PWM0		DA0	
5	3		P9_2		TB2IN/PMC0	SOUT3		
6	4		P9_1		TB1IN/PMC1	SIN3		
7	5		P9_0		TB0IN	CLK3		
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	$\overline{\text{RESET}}$						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$	CEC		
18	16		P8_4	$\overline{\text{INT2}}$	ZP			
19	17		P8_3	$\overline{\text{INT1}}$				
20	18		P8_2	$\overline{\text{INT0}}$				
21	19		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$		
22	20		P8_0		TA4OUT/U	RXD5/SCL5		
23	21		P7_7		TA3IN	CLK5		
24	22		P7_6		$\overline{\text{TA3OUT}}$	$\overline{\text{TXD5}}$/SDA5		
25	23		P7_5		TA2IN/$\overline{\text{W}}$			
26	24		P7_4		TA2OUT/W			
27	25		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$		
28	26		P7_2		TA1OUT/V	CLK2		
29	27		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
30	28		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$ /CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0		RTCOUT	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
39	37	CLKOUT	P5_7					$\overline{\text{RDY}}$
40	38		P5_6					ALE
41	39		P5_5					$\overline{\text{HOLD}}$
42	40		P5_4					$\overline{\text{HLDA}}$
43	41		P5_3					BCLK
44	42		P5_2					$\overline{\text{RD}}$
45	43		P5_1					$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
46	44		P5_0					$\overline{\text{WRL}}$/$\overline{\text{WR}}$
47	45		P4_7		PWM1	TXD7/SDA7		$\overline{\text{CS3}}$
48	46		P4_6		PWM0	RXD7/SCL7		$\overline{\text{CS2}}$
49	47		P4_5			CLK7		$\overline{\text{CS1}}$
50	48		P4_4			$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$		$\overline{\text{CS0}}$

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. Seven registers (R0, R1, R2, R3, A0, A1, and FB) out of 13 compose a register bank, and there are two register banks.



Note:
1. These registers compose a register bank. There are two register banks.

Figure 2.1 CPU Registers

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	Reset Value
0040h			
0041h			
0042h	$\overline{\text{INT7}}$ Interrupt Control Register	INT7IC	XX00 X000b
0043h	$\overline{\text{INT6}}$ Interrupt Control Register	INT6IC	XX00 X000b
0044h	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC U1BCNIC	XXXX X000b
0047h	Timer B3 Interrupt Control Register UART0 Bus Collision Detection Interrupt Control Register	TB3IC U0BCNIC	XXXX X000b
0048h	SI/O4 Interrupt Control Register $\overline{\text{INT5}}$ Interrupt Control Register	S4IC INT5IC	XX00 X000b
0049h	SI/O3 Interrupt Control Register $\overline{\text{INT4}}$ Interrupt Control Register	S3IC INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
005Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
005Fh	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	Reset Value
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0183h			
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0187h			
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
018Dh			
018Eh			
018Fh			
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0193h			
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0197h			
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
019Dh			
019Eh			
019Fh			
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A3h			
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A7h			
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01ADh			
01AEh			
01AFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h	UART7 Special Mode Register 4	U7SMR4	00h
02A5h	UART7 Special Mode Register 3	U7SMR3	000X 0X0Xb
02A6h	UART7 Special Mode Register 2	U7SMR2	X000 0000b
02A7h	UART7 Special Mode Register	U7SMR	X000 0000b
02A8h	UART7 Transmit/Receive Mode Register	U7MR	00h
02A9h	UART7 Bit Rate Register	U7BRG	XXh
02AAh	UART7 Transmit Buffer Register	U7TB	XXh
02ABh			XXh
02ACh	UART7 Transmit/Receive Control Register 0	U7C0	0000 1000b
02ADh	UART7 Transmit/Receive Control Register 1	U7C1	0000 0010b
02AEh	UART7 Receive Buffer Register	U7RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h to 02FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Electrical Characteristics (Common to 3 V and 5 V)

5.1.1 Absolute Maximum Rating

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC1}	Supply voltage		$V_{CC1} = AV_{CC}$	–0.3 to 6.5	V
V_{CC2}	Supply voltage		$V_{CC1} = AV_{CC}$	–0.3 to V_{CC1} + 0.1 (1)	V
AV_{CC}	Analog supply voltage		$V_{CC1} = AV_{CC}$	–0.3 to 6.5	V
V_{REF}	Analog reference voltage		$V_{CC1} = AV_{CC}$	–0.3 to V_{CC1} + 0.1 (1)	V
V_I	Input voltage	$\overline{RESET}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN		–0.3 to V_{CC1} + 0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		–0.3 to V_{CC2} + 0.3 (1)	V
		P7_0, P7_1, P8_5		–0.3 to 6.5	V
V_O	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 XOUT		–0.3 to V_{CC1} + 0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		–0.3 to V_{CC2} + 0.3 (1)	V
		P7_0, P7_1, P8_5		–0.3 to 6.5	V
P_d	Power consumption		$-40°C < T_{opr} \leq 85°C$	300	mW
T_{opr}	Operating temperature	When the MCU is operating		–20 to 85/–40 to 85	°C
		Flash program erase	Program area	0 to 60	
			Data area	–20 to 85/–40 to 85	
T_{stg}	Storage temperature			–65 to 150	°C

Note:
1. Maximum value is 6.5 V.

Table 5.3 Recommended Operating Conditions (2/3)

V_{CC1} = V_{CC2} = 2.7 to 5.5 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$I_{OL(sum)}$	Low peak output current	Sum of $I_{OL(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			80.0	mA
$I_{OL(peak)}$	Low peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			10.0	mA
$I_{OL(avg)}$	Low average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			5.0	mA
$f_{(XIN)}$	Main clock input oscillation frequency	V_{CC1} = 2.7 V to 5.5 V	2		20	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768	50	kHz
$f_{(PLL)}$	PLL clock oscillation frequency	V_{CC1} = 2.7 V to 5.5 V	10		25	MHz
$f_{(BCLK)}$	CPU operation clock		2		25	MHz
$t_{SU(PLL)}$	PLL frequency synthesizer stabilization wait time	V_{CC1} = 5.0 V			2	ms
		V_{CC1} = 3.0 V			3	ms

Note:
1. The average output current is the mean value within 100 ms.

Table 5.4 Recommended Operating Conditions (3/3) (1)

V_{CC1} = 2.7 to 5.5 V, V_{SS} = 0 V, and T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.
The ripple voltage must not exceed $V_{r(VCC1)}$ and/or $dV_{r(VCC1)}/dt$.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$V_{r(VCC1)}$	Allowable ripple voltage	V_{CC1} = 5.0 V			0.5	Vp-p
		V_{CC1} = 3.0 V			0.3	Vp-p
$dV_{r(VCC1)}/dt$	Ripple voltage falling gradient	V_{CC1} = 5.0 V			0.3	V/ms
		V_{CC1} = 3.0 V			0.3	V/ms

Note:
1. The device is operationally guaranteed under these operating conditions.

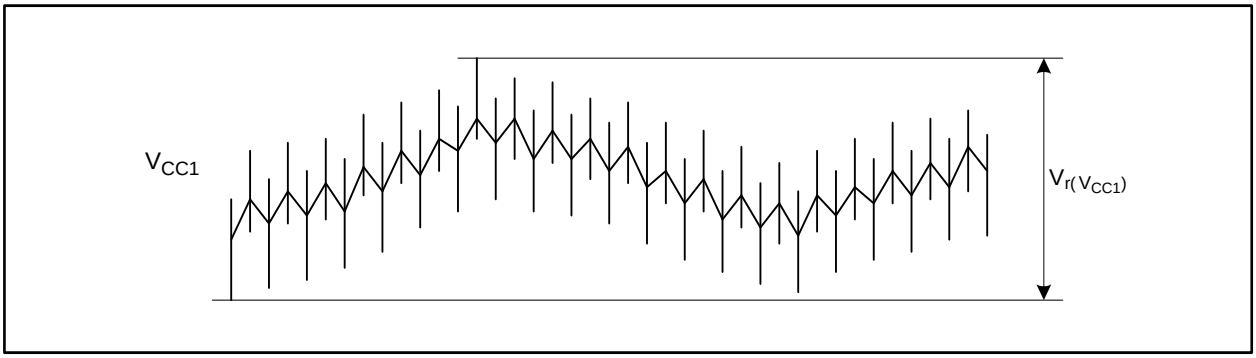


Figure 5.1 Ripple Waveform

Table 5.10 Flash Memory (Data Flash) Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C/-40 to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	V_{CC1} = 3.3 V, T_{opr} = 25°C	10,000 (2)			times
-	2 word program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		300	4000	µs
-	Lock bit program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		140	3000	µs
-	Block erase time	V_{CC1} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
-	Program, erase voltage		2.7		5.5	V
-	Read voltage		2.7		5.5	V
-	Program, erase temperature		–20/–40		85	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55 °C	20			year

Notes:
1. Definition of program and erase cycles
   The program and erase cycles refer to the number of per-block erasures.
   If the program and erase cycles are n (n = 10,000), each block can be erased n times.
   For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

5.1.6 Voltage Detector and Power Supply Circuit Electrical Characteristics

Table 5.11 Voltage Detector 0 Electrical Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)	When V_{CC1} is falling.	1.60	1.90	2.20	V
	Voltage detection level Vdet0_2 (1)	When V_{CC1} is falling.	2.55	2.85	3.15	V
-	Voltage detector 0 response time (3)	When V_{CC1} falls from 5 V to (Vdet0_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC25 = 1, V_{CC1} = 5.0 V		1.8		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (2)				100	µs

Notes:
1. Select the voltage detection level with the VDSEL1 bit in the OFS1 address.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.
3. Time from when passing the V_{det0} until when a voltage monitor 0 reset is generated.

Table 5.12 Voltage Detector 1 Electrical Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_6 (1)	When V_{CC1} is falling.	2.79	3.09	3.39	V
	Voltage detection level Vdet1_B (1)	When V_{CC1} is falling.	3.54	3.84	4.14	V
	Voltage detection level Vdet1_F (1)	When V_{CC1} is falling.	3.94	4.44	4.94	V
-	Hysteresis width when V_{CC1} of voltage detector 1 is rising			0.15		V
-	Voltage detector 1 response time (3)	When V_{CC1} falls from 5 V to (Vdet1_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC26 = 1, V_{CC1} = 5.0 V		1.8		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (2)				100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC26 bit in the VCR2 register to 0.
3. Time from when passing the V_{det1} until when a voltage monitor 1 reset is generated.

Table 5.13 Voltage Detector 2 Electrical Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	When V_{CC1} is falling	3.50	4.00	4.50	V
-	Hysteresis width at the rising of V_{CC1} in voltage detector 2			0.15		V
-	Voltage detector 2 response time (2)	When V_{CC1} falls from 5 V to (Vdet2_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC27 = 1, V_{CC1} = 5.0 V		1.8		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)				100	µs

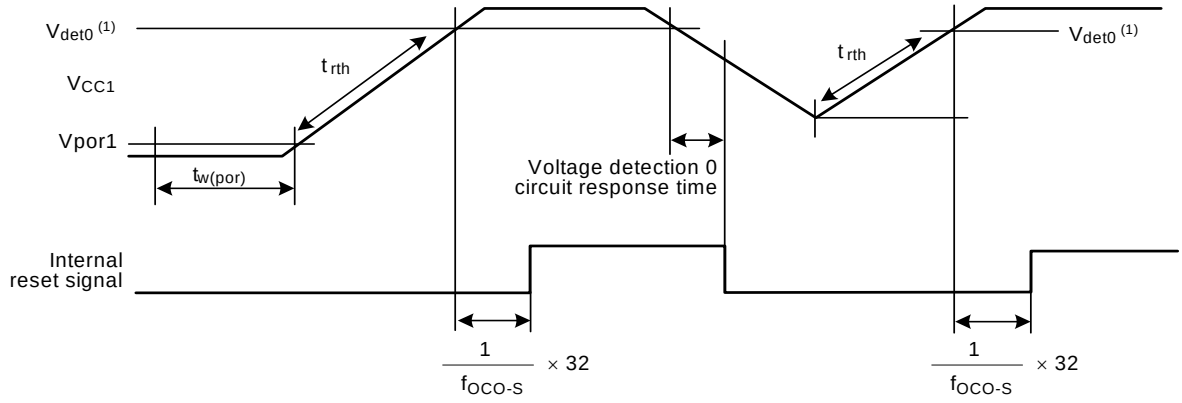
Notes:
1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.
2. Time from when passing the V_{det2} until when a voltage monitor 2 reset is generated.

Table 5.14 Power-On Reset Circuit

The measurement condition is V_{CC1} = 2.0 to 5.5 V, T_{opr} = -20°C to 85°C/ -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Voltage at which power-on reset enabled (1)				0.1	V
t_{rth}	External power V_{CC1} rise gradient		2.0		50000	mV/ms
$t_{w(por)}$	Time necessary to enable power-on reset		300			ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0. Also, set the VDSEL1 bit to 0 (Vdet0_2).



Note:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit.

Figure 5.3 Power-On Reset Circuit Electrical Characteristics

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.3 In 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus

Table 5.37 Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus) (5)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(Note 3)		ns
$t_{h(AD-ALE)}$	ALE signal output hold time (in relation to Address)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of address		0		ns
$t_{dz(RD-AD)}$	Address output floating start time			8	ns

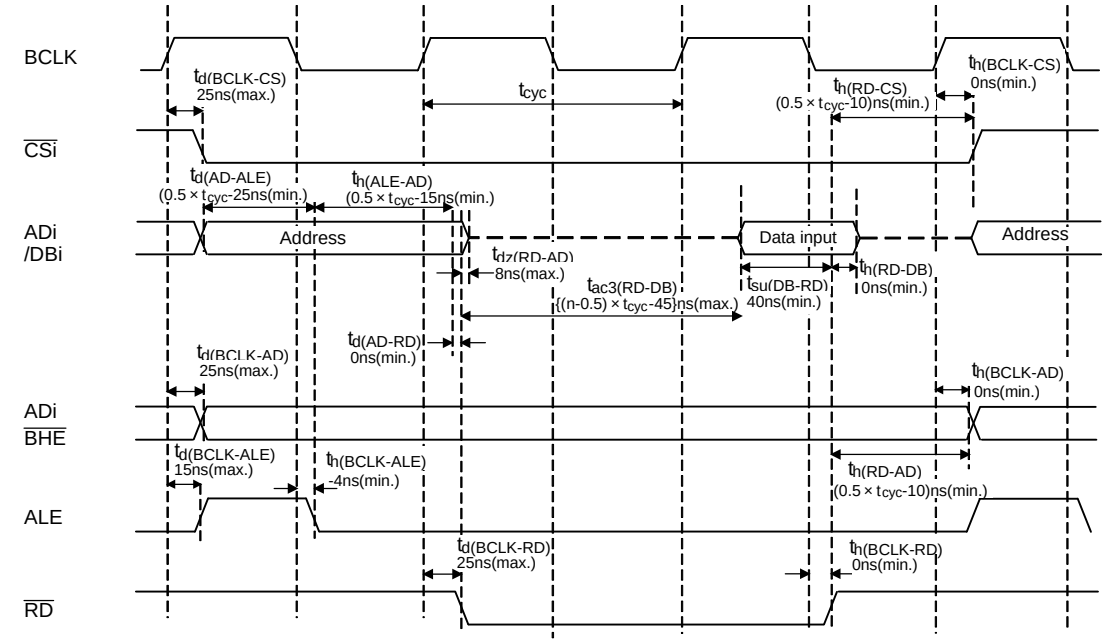
Notes:

1. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$$
2. Calculated according to the BCLK frequency as follows:
$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 40[ns]$$
n is 2 for 2-wait setting, 3 for 3-wait setting.
3. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 25[ns]$$
4. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[ns]$$
5. When using multiplex bus, set $f_{(BCLK)}$ 12.5 MHz or less.

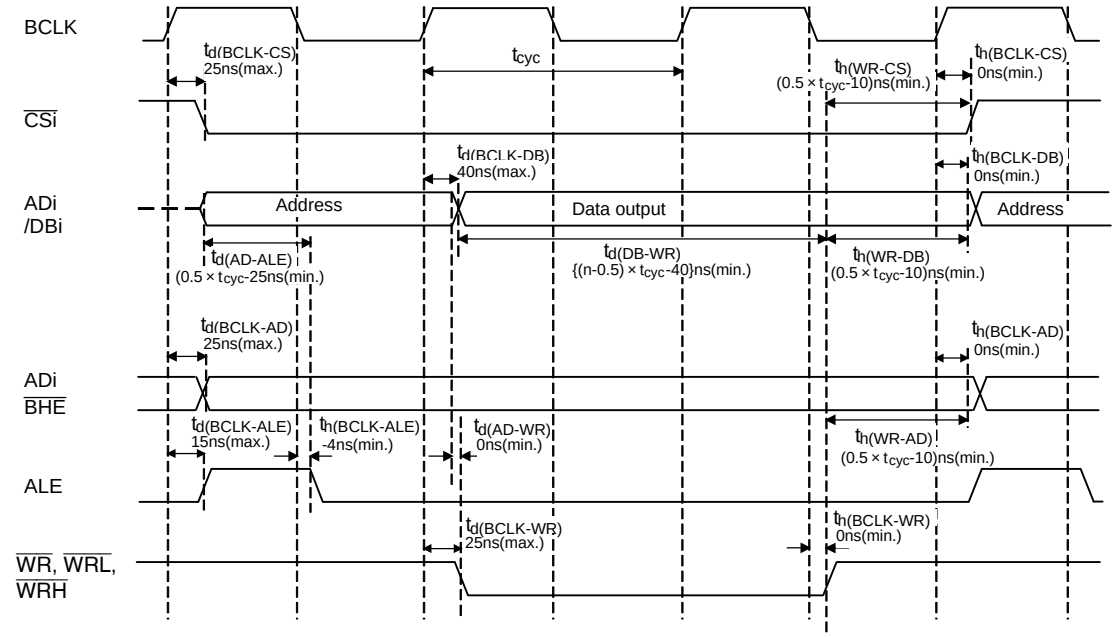
Memory Expansion Mode and Microprocessor Mode
(in 2 or 3 waits setting, and when accessing external area and using multiplexed bus)

$V_{CC1} = V_{CC2} = 5V$

Read timing



Write timing



Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

n: 2 (when 2 waits)
3 (when 3 waits)

Figure 5.17 Timing Diagram

$V_{CC1} = V_{CC2} = 3\ V$

5.3.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.41 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

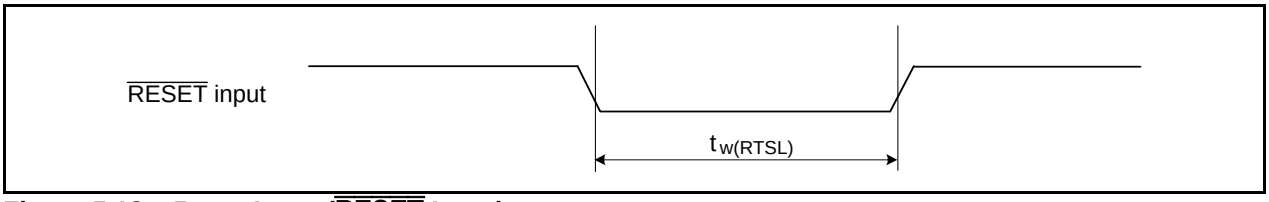


Figure 5.18 Reset Input ($\overline{\text{RESET}}$ Input)

5.3.2.2 External Clock Input

Table 5.42 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is $V_{CC1} = V_{CC2} = 2.7$ to 3.0 V.

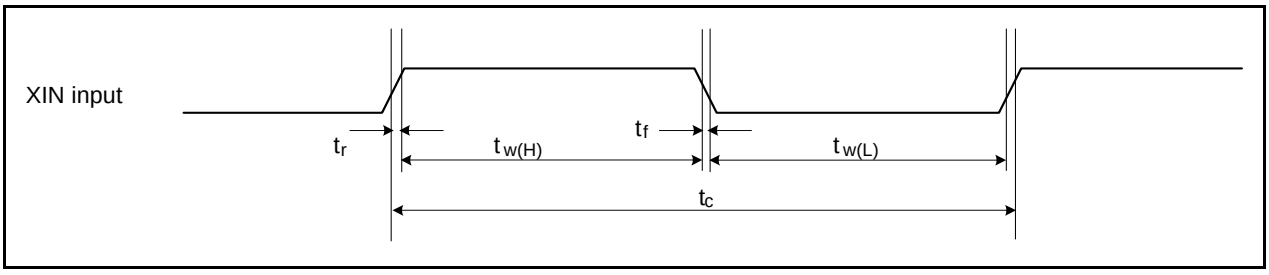


Figure 5.19 External Clock Input (XIN Input)

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.4 Timer B Input

Table 5.48 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	120		ns

Table 5.49 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

Table 5.50 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t^{w(TBL)}$	TBiIN input low pulse width	300		ns

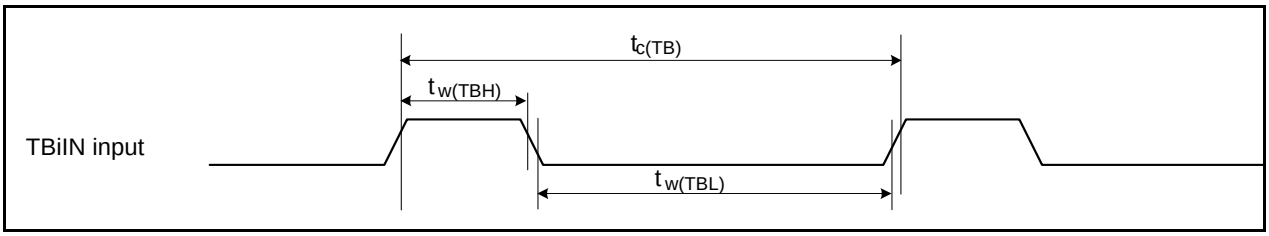


Figure 5.22 Timer B Input

$V_{CC1} = V_{CC2} = 3\ V$

5.3.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.1 In No Wait State Setting

Table 5.55 Memory Expansion and Microprocessor Modes (in No Wait State Setting)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.27		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

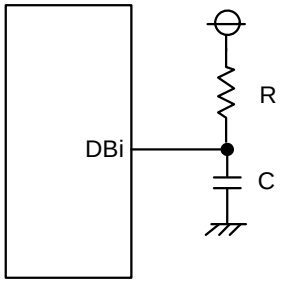
1. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$ $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ,
   hold time of output low level is
   $t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
   = 6.7 ns.



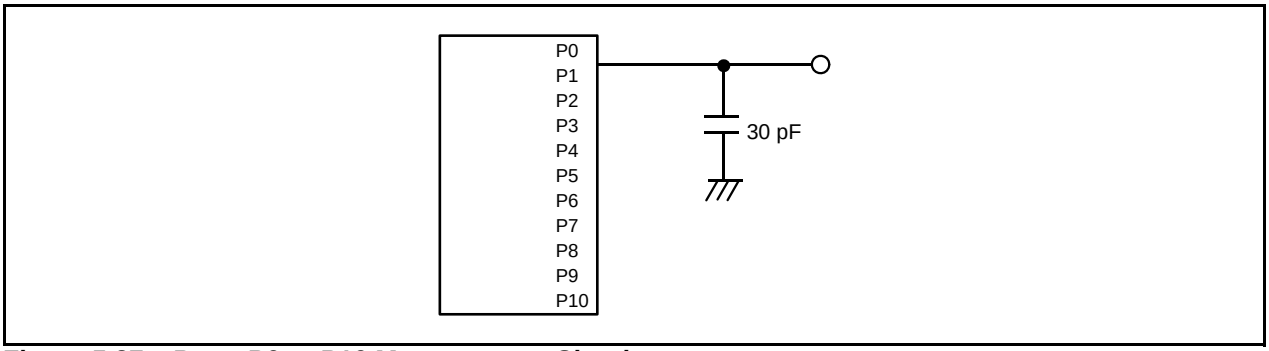


Figure 5.27 Ports P0 to P10 Measurement Circuit

$V_{CC1} = V_{CC2} = 3\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.2 In 1 to 3 Waits Setting and When Accessing External Area

Table 5.56 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.27		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

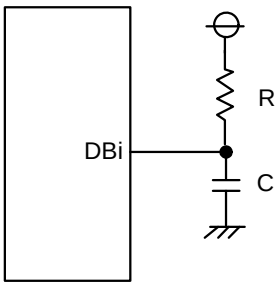
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.
When n = 1, $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

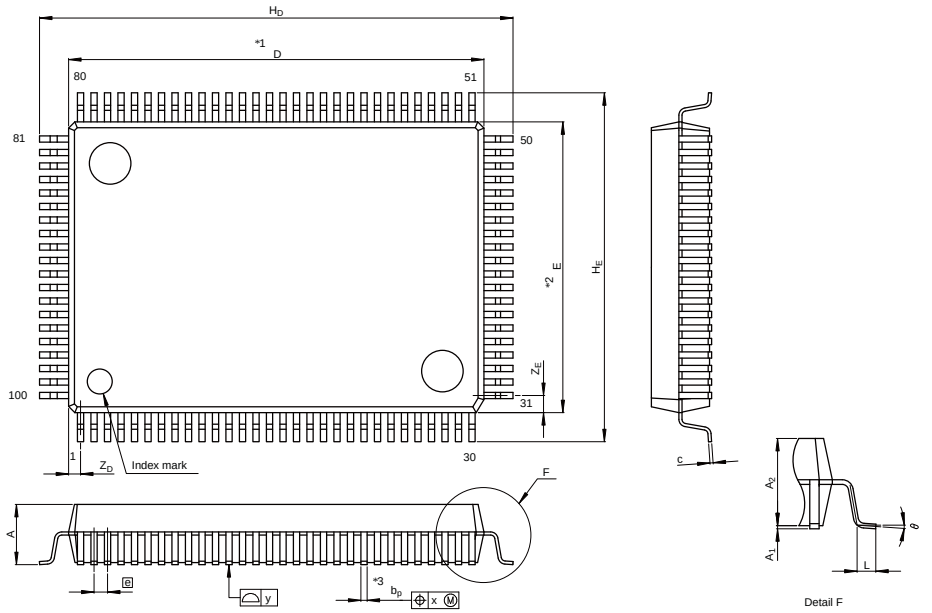
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



Appendix 1. Package Dimensions

The information on the latest package dimensions or packaging may be obtained from “Packages“ on the Renesas Electronics website.

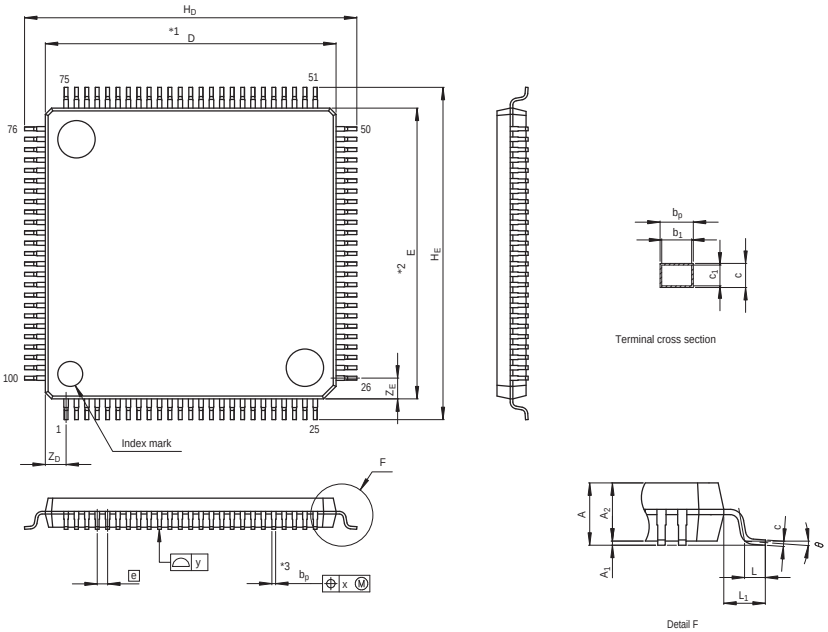
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JD-B	100P6F-A	1.8g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	M16C/64A Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.01	Feb 03, 2009	-	First Edition issued.
1.10	Jul 15, 2009	-	Watchdog Timer Reset Register → Watchdog Timer Refresh Register
		3	Table 1.2 Specifications for the 100-Pin Package (2/2) partially modified
		4	Table 1.3 Product List partially modified
		5	Figure 1.2 Marking Diagram (Top View) partially modified
		18	Figure 3.2 Memory Map 13800h → 13000h
		20	Table 4.1 “SFR Information (1/16)” reset value in VCR1 modified
		21	Table 4.2 “SFR Information (2/16)” partially modified
		29	Table 4.10 “SFR Information (10/16)” reset value in S11 modified
		37	Table 5.1 Absolute Maximum Ratings partially modified
		38	Table 5.2 Recommended Operating Conditions (1/3) partially modified
		39	Table 5.3 Recommended Operating Conditions (2/3) partially modified
		40	Table 5.4 Recommended Operating Conditions (3/3) added
		40	Figure 5.1 Ripple Waveform added
		41	Table 5.5 A/D Conversion Characteristics (1/2) partially modified
		41	Figure 5.2 A/D Accuracy Measure Circuit added
		42	Table 5.6 A/D Conversion Characteristics (2/2) partially modified
		44	Table 5.8 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$) partially modified
		44	Table 5.9 Flash Memory (Program ROM 1, 2) Electrical Characteristics notes modified
		46	Table 5.11 Voltage Detector 0 Electrical Characteristics partially modified
		46	Table 5.12 Voltage Detector 1 Electrical Characteristics partially modified
		47	Table 5.13 Voltage Detector 2 Electrical Characteristics partially modified
		47	Table 5.14 Power-On Reset Circuit partially modified
		48	Figure 5.3 Power-On Reset Circuit Electrical Characteristics partially modified
		50	Table 5.16 125 kHz On-Chip Oscillator Circuit Electrical Characteristics partially modified
		53	Table 5.19 Electrical Characteristics (3) partially modified
		54	Table 5.20 Electrical Characteristics (4) partially modified
		55	5.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input) added
		69	Table 5.37 Electrical Characteristics (1) partially modified
		70	Table 5.38 Electrical Characteristics (2) partially modified
		71	Table 5.39 Electrical Characteristics (3) partially modified
		73	5.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input) added
			Same modifications made to both 3 V and 5 V specifications.
2.00	Feb 07, 2011	Overall	001Ah Voltage Detector Operation Enable Register: Changed reset value from “000X 0000b”.
		Overall	002Ah Voltage Monitor 0 Control Register: Changed reset value from “1100 XX10b”.
		Overall	002Bh Voltage Monitor 1 Control Register: Changed reset value from “1000 1X10b”.
		Overall	0324h Increment/Decrement Flag: Changed name from Up/Down Flag.
		Overall	033Eh Timer B2 Special Mode Register: Changed reset value from “XX00 0000b”.
		Overall	03A2h Open-Circuit Detection Assist Function Register: Changed reset value from “XXXX XX00b”.
		Overall	03DCh D/A Control Register: Changed reset value from “XXXX XX00b”.
		Overall	D08Ah to D08Bh PMC0 Counter Value Register: Deleted.
		Overall	D09Eh to D09Fh PMC1 Counter Value Register: Deleted.
		Overall	Changed “high-speed clock mode” to “fast-mode”.
		Overview	
		3	Table 1.2 Specifications for the 100-Pin Package (2/2): Deleted note 1.
		4	Table 1.3 Product List: Added the new part numbers.
		5	Figure 1.1 Part No., with Memory Size and Package: Added “K” to the Memory capacity.
		11	Table 1.6 Pin Functions for the 100-Pin Package (1/3): Changed the description of $\overline{\text{HOLD}}$ pin.