Renesas Electronics America Inc - R5F364A6NFA#U0 Datasheet

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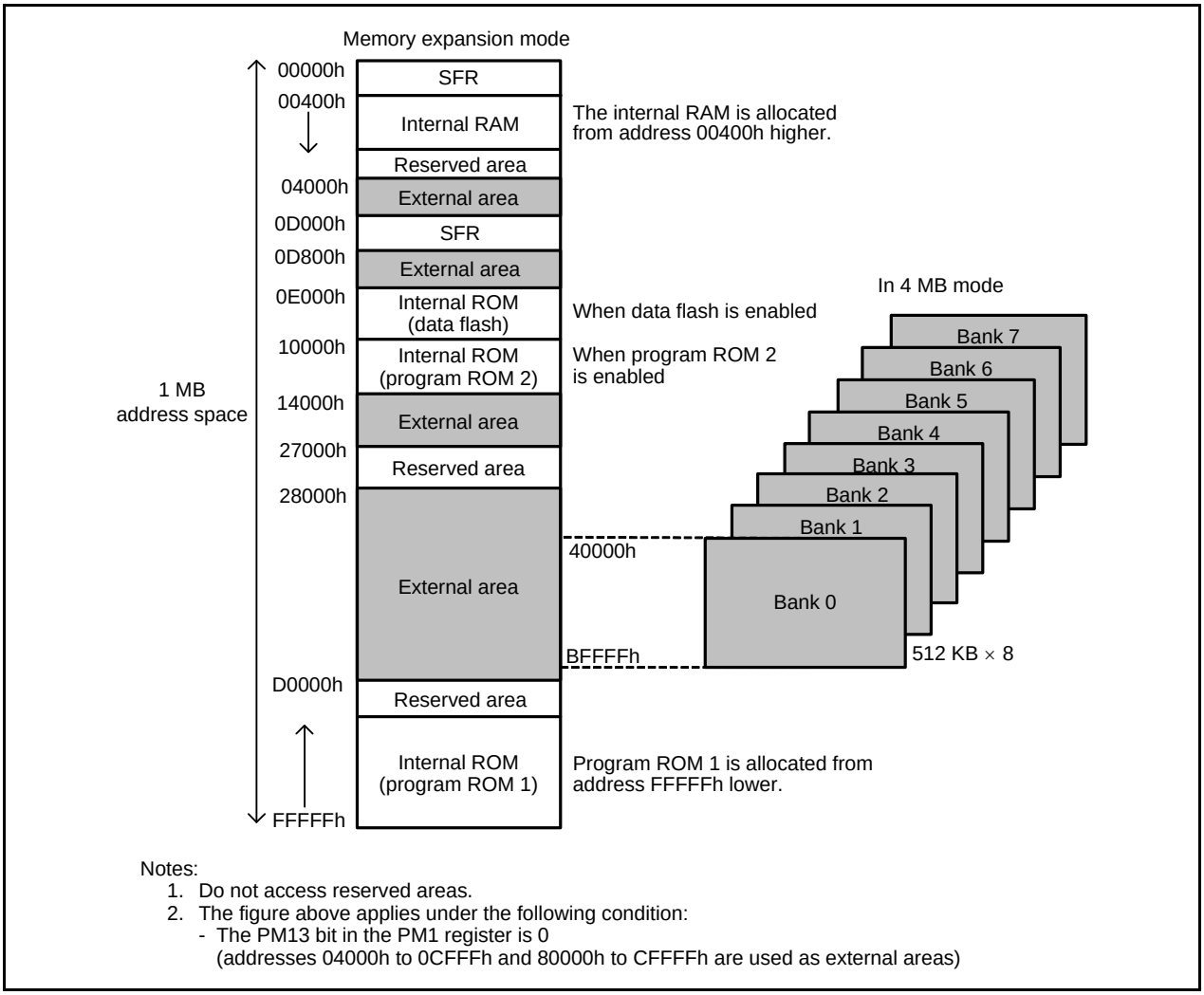
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f364a6nfa-u0

3. Address Space

3.1 Address Space

The M16C/64A Group has a 1 MB address space from 00000h to FFFFFh. Address space is expandable to 4 MB with the memory area expansion function. Addresses 40000h to BFFFFh can be used as external areas from bank 0 to bank 7. Figure 3.1 shows the Address Space. Areas that can be accessed vary depending on processor mode and the status of each control bit.



Notes:
1. Do not access reserved areas.
2. The figure above applies under the following condition:
   - The PM13 bit in the PM1 register is 0
     (addresses 04000h to 0CFFFh and 80000h to CFFFFh are used as external areas)

Figure 3.1 Address Space

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	Reset Value
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh	UART5 Bus Collision Detection Interrupt Control Register CEC1 Interrupt Control Register	U5BCNIC CEC1IC	XXXX X000b
006Ch	UART5 Transmit Interrupt Control Register CEC2 Interrupt Control Register	S5TIC CEC2IC	XXXX X000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXX X000b
006Eh	UART6 Bus Collision Detection Interrupt Control Register Real-Time Clock Periodic Interrupt Control Register	U6BCNIC RTCTIC	XXXX X000b
006Fh	UART6 Transmit Interrupt Control Register Real-Time Clock Compare Interrupt Control Register	S6TIC RTCCIC	XXXX X000b
0070h	UART6 Receive Interrupt Control Register	S6RIC	XXXX X000b
0071h	UART7 Bus Collision Detection Interrupt Control Register Remote Control Signal Receiver 0 Interrupt Control Register	U7BCNIC PMC0IC	XXXX X000b
0072h	UART7 Transmit Interrupt Control Register Remote Control Signal Receiver 1 Interrupt Control Register	S7TIC PMC1IC	XXXX X000b
0073h	UART7 Receive Interrupt Control Register	S7RIC	XXXX X000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh	I2C-bus Interface Interrupt Control Register	IICIC	XXXX X000b
007Ch	SCL/SDA Interrupt Control Register	SCLDAIC	XXXX X000b
007Dh			
007Eh			
007Fh			
0080h to 017Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	Reset Value
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	0000 0000b (2) 0000 0010b
0362h	Pull-Up Control Register 2	PUR2	00h
0363h			
0364h			
0365h			
0366h	Port Control Register	PCR	0000 0XX0b
0367h			
0368h			
0369h	NMI/SD Digital Filter Register	NMIDF	XXXX X000b
036Ah			
036Bh			
036Ch			
036Dh			
036Eh			
036Fh			
0370h	PWM Control Register 0	PWMCON0	00h
0371h			
0372h	PWM0 Prescaler	PWMPRE0	00h
0373h	PWM0 Register	PWMREG0	00h
0374h	PWM1 Prescaler	PWMPRE1	00h
0375h	PWM1 Register	PWMREG1	00h
0376h	PWM Control Register 1	PWMCON1	00h
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	00h (3)
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0380h to 038Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Values after hardware reset, power-on reset, or voltage monitor 0 reset are as follows:
 - 00000000b when a low-level signal is input to the CNVSS pin
 - 00000010b when a high-level signal is input to the CNVSS pin
 Values after voltage monitor 1 reset, voltage monitor 2 reset, software reset, watchdog timer reset, or oscillation stop detect reset are as follows:
 - 00000000b when bits PM01 and PM00 in the PM0 register are 00b (single-chip mode).
 - 00000010b when bits PM01 and PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode).
3. When the CSPROINI bit in the OFS1 address is 0, the reset value is 10000000b.

Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	Reset Value
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D5h			
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b
03D8h	D/A0 Register	DA0	00h
03D9h			
03DAh	D/A1 Register	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.17 SFR Information (17) (1)

Address	Register	Symbol	Reset Value
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h			
03F6h	Port P10 Direction Register	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.20 Read-Modify-Write Instructions

Function	Mnemonic
Transfer	MOV*Dir*
Bit processing	BCLR, BM*Cnd*, BNOT, BSET, BTSTC, and BTSTS
Shifting	ROLC, RORC, ROT, SHA, and SHL
Arithmetic operation	ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB
Decimal operation	DADC, DADD, DSBB, and DSUB
Logical operation	AND, NOT, OR, and XOR
Jump	ADJNZ, SBJNZ

5.1.5 Flash Memory Electrical Characteristics

Table 5.8 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$)

V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				10 (1)	MHz
f(SLOW_R)	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			fC(32.768)	35	kHz
-	Data flash read	2.7 V ≤ V_{CC1} ≤ 3.0 V			16 (2)	MHz
		3.0 V < V_{CC1} ≤ 5.5 V			20 (2)	MHz

Notes:
1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). When using 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is not necessary.

Table 5.9 Flash Memory (Program ROM 1, 2) Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V at T_{opr} = 0°C to 60°C (option: -40°C to 85°C), unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	V_{CC1} = 3.3 V, T_{opr} = 25°C	1,000 (2)			times
-	2 word program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		150	4000	µs
-	Lock bit program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		70	3000	µs
-	Block erase time	V_{CC1} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
-	Program, erase voltage		2.7		5.5	V
-	Read voltage	T_{opr}= -20°C to 85°C/-40°C to 85°C	2.7		5.5	V
-	Program, erase temperature		0		60	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:
1. Definition of program and erase cycles:
   The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 1,000), each block can be erased n times. For example, if a block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.10 Flash Memory (Data Flash) Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C/-40 to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	V_{CC1} = 3.3 V, T_{opr} = 25°C	10,000 (2)			times
-	2 word program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		300	4000	µs
-	Lock bit program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		140	3000	µs
-	Block erase time	V_{CC1} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
-	Program, erase voltage		2.7		5.5	V
-	Read voltage		2.7		5.5	V
-	Program, erase temperature		–20/–40		85	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55 °C	20			year

Notes:
1. Definition of program and erase cycles
   The program and erase cycles refer to the number of per-block erasures.
   If the program and erase cycles are n (n = 10,000), each block can be erased n times.
   For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.15 Power Supply Circuit Timing Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V and T_{opr} = 25°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply stability time when power is on (1)				5	ms
$t_{d(R-S)}$	STOP release time				150	µs
$t_{d(W-S)}$	Low power mode wait mode release time				150	µs

Note:
1. Waiting time until the internal power supply generator stabilizes when power is on.

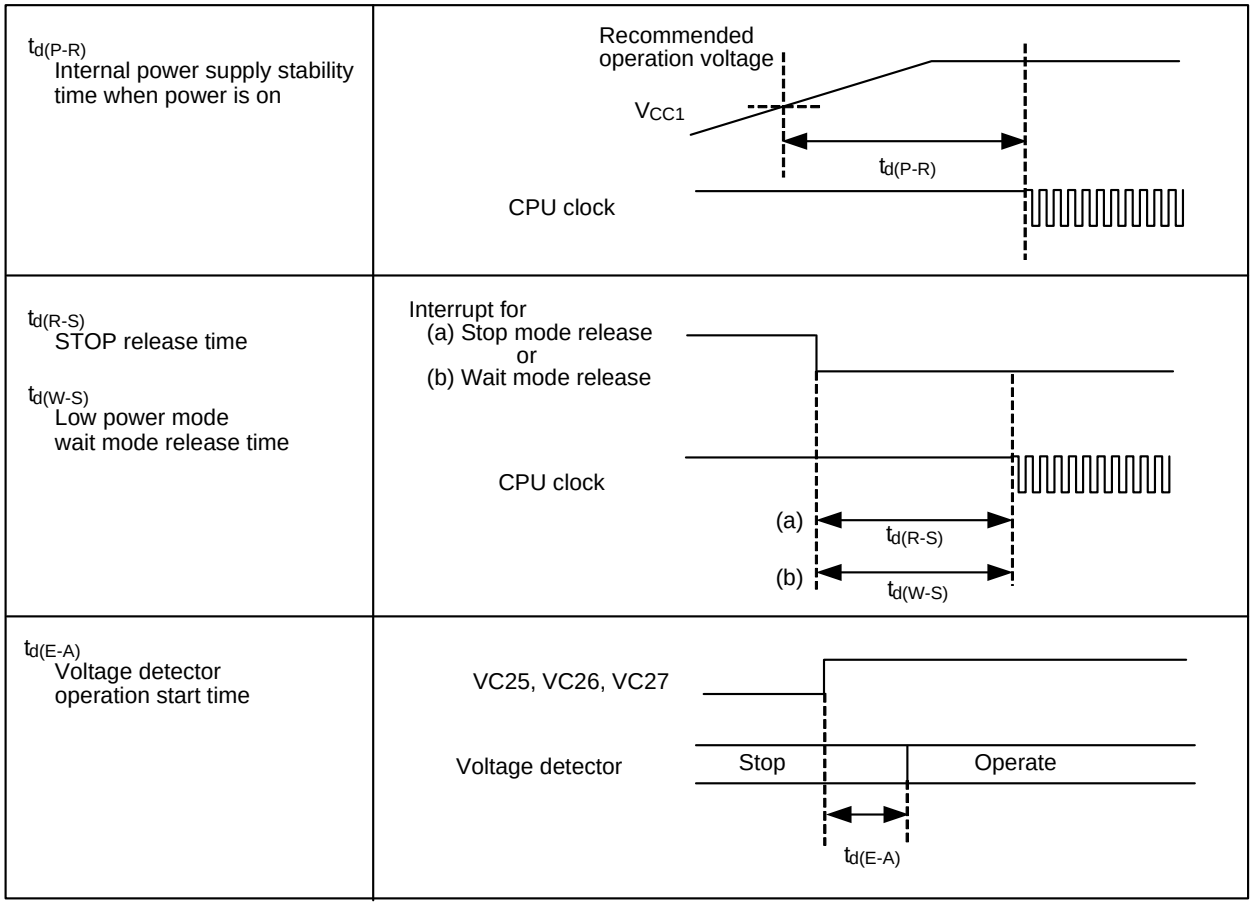


Figure 5.4 Power Supply Circuit Timing Diagram

5.2 Electrical Characteristics (V_{CC1} = V_{CC2} = 5 V)

5.2.1 Electrical Characteristics

V_{CC1} = V_{CC2} = 5 V

Table 5.17 Electrical Characteristics (1) [1]

V_{CC1} = V_{CC2} = 4.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = –20°C to 85°C/–40°C to 85°C, $f_{(BCLK)}$ = 25 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = –5 mA	V_{CC1} – 2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OH} = –5 mA	V_{CC2} – 2.0		V_{CC2}	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = –200 µA	V_{CC1} – 0.3		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OH} = –200 µA	V_{CC2} – 0.3		V_{CC2}	
V_{OH}	High output voltage XOUT		HIGH POWER	I_{OH} = –1 mA	V_{CC1} – 2.0		V_{CC1}	V
			LOW POWER	I_{OH} = –0.5 mA	V_{CC1} – 2.0		V_{CC1}	
	High output voltage XCOUT		HIGH POWER	With no load applied		2.6		V
			LOW POWER	With no load applied		2.2		
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OL} = 5 mA			2.0	
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 200 µA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OL} = 200 µA			0.45	
V_{OL}	Low output voltage XOUT		HIGH POWER	I_{OL} = 1 mA			2.0	V
			LOW POWER	I_{OL} = 0.5 mA			2.0	
	Low output voltage XCOUT		HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.20 Electrical Characteristics (4)

R5F364AKNFA, R5F364AKNFB, R5F364AKDFA, R5F364AKDFB
R5F364AMNFA, R5F364AMNFB, R5F364AMDFA, R5F364AMDFB

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/−40°C to 85°C, $f_{(BCLK)} = 25$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)}$ = 25 MHz XIN = 4.2 MHz (square wave), PLL multiplied by 6 125 kHz on-chip oscillator stopped		22.0		mA
			$f_{(BCLK)}$ = 25 MHz, A/D conversion XIN = 4.2 MHz (square wave), PLL multiplied by 6 125 kHz on-chip oscillator stopped		22.7		mA
			$f_{(BCLK)}$ = 20 MHz XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped		17.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		550.0		µA
		Low-power mode	$f_{(BCLK)}$ = 32 kHz In low-power mode FMR22 = FMR23 = 1 on flash memory (1)		170.0		µA
			$f_{(BCLK)}$ = 32 kHz In low-power mode on RAM (1)		45.0		µA
		Wait mode	Main clock stopped 125 kHz on-chip oscillator on Peripheral clock operating T_{opr} = 25°C		20.5		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity High) 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		11.0		µA
			$f_{(BCLK)}$ = 32 kHz (oscillation capacity low) 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		6.0		µA
		Stop mode	Main clock stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped T_{opr} = 25°C		1.7		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		30.0		mA

Note:
1. This indicates the memory in which the program to be executed exists.

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.3 Timer A Input

Table 5.23 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

Table 5.24 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

Table 5.25 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

Table 5.26 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

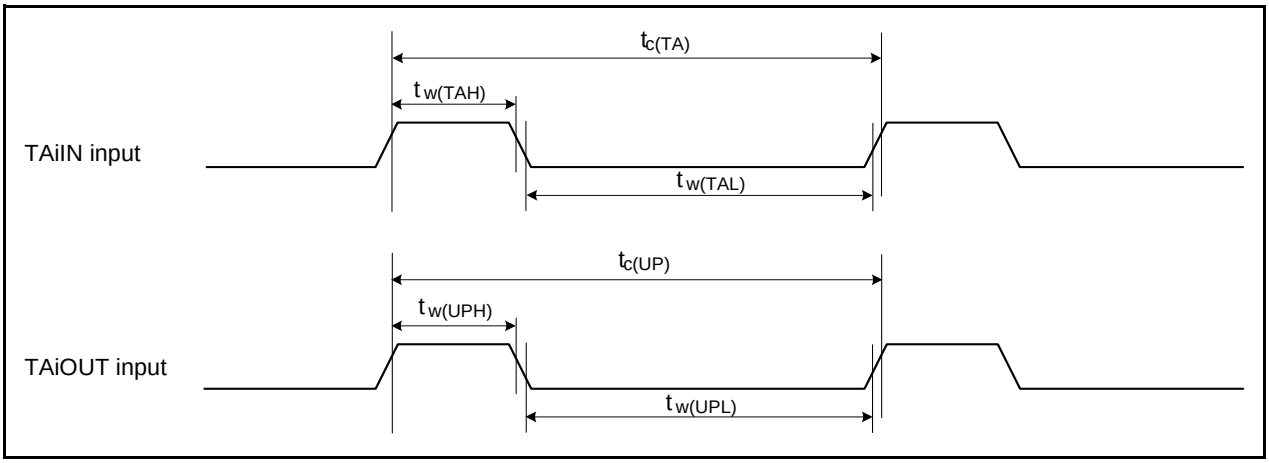


Figure 5.7 Timer A Input

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.2 In 1 to 3 Waits Setting and When Accessing External Area

Table 5.36 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)(3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

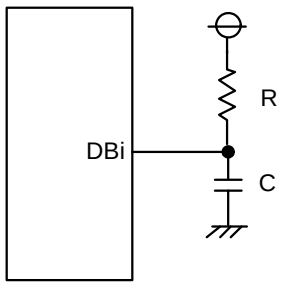
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.
When n = 1, $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.3 In 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus

Table 5.37 Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus) (5)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(Note 3)		ns
$t_{h(AD-ALE)}$	ALE signal output hold time (in relation to Address)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of address		0		ns
$t_{dz(RD-AD)}$	Address output floating start time			8	ns

Notes:

1. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$$
2. Calculated according to the BCLK frequency as follows:
$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 40[ns]$$
n is 2 for 2-wait setting, 3 for 3-wait setting.
3. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 25[ns]$$
4. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[ns]$$
5. When using multiplex bus, set $f_{(BCLK)}$ 12.5 MHz or less.

$V_{CC1} = V_{CC2} = 3\ V$

5.3.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.41 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

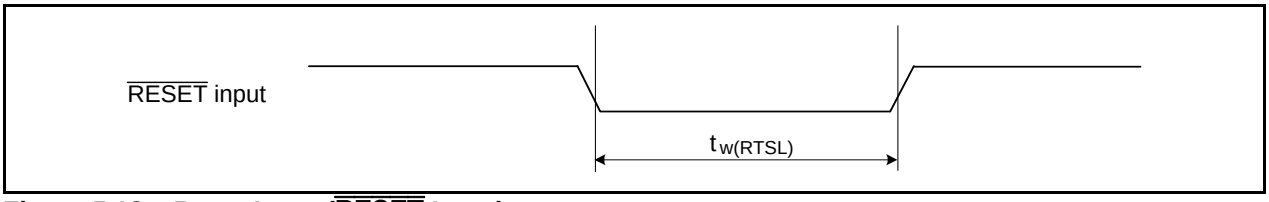


Figure 5.18 Reset Input ($\overline{\text{RESET}}$ Input)

5.3.2.2 External Clock Input

Table 5.42 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is $V_{CC1} = V_{CC2} = 2.7$ to 3.0 V.

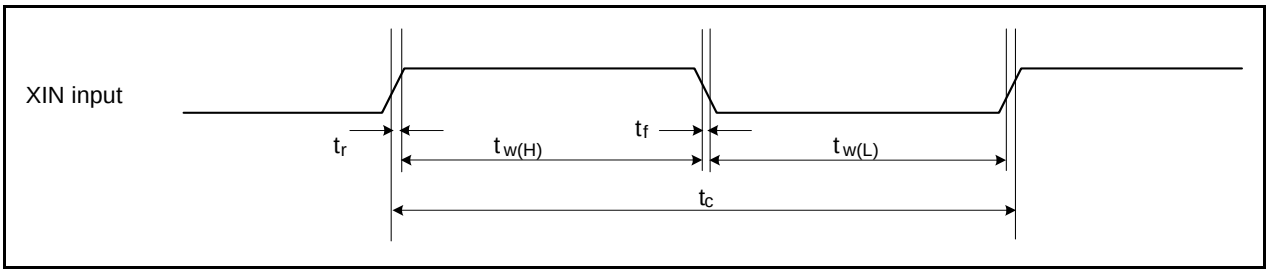


Figure 5.19 External Clock Input (XIN Input)

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.5 Serial Interface

Table 5.51 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

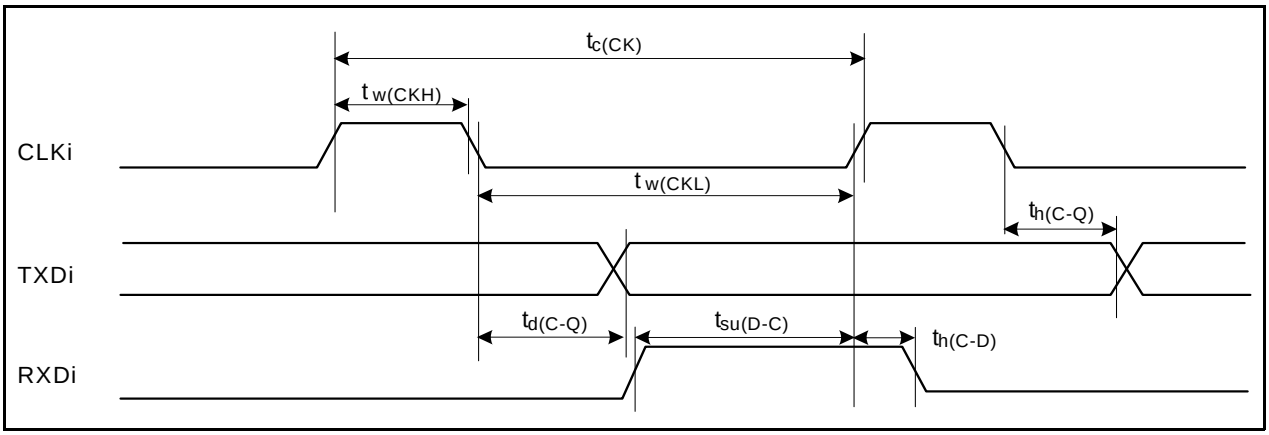


Figure 5.23 Serial Interface

5.3.2.6 External Interrupt $\overline{INTi}$ Input

Table 5.52 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	380		ns

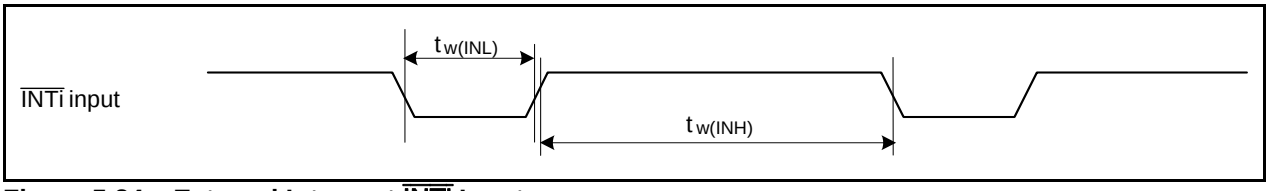


Figure 5.24 External Interrupt $\overline{INTi}$ Input

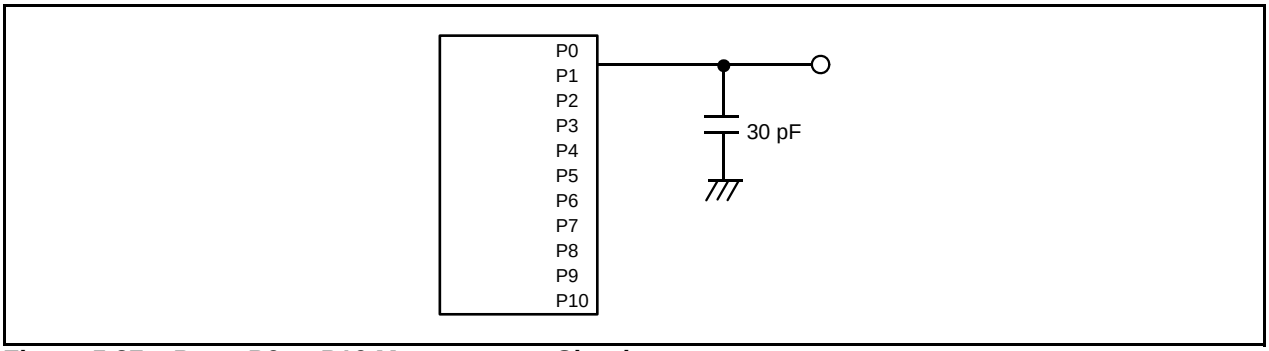


Figure 5.27 Ports P0 to P10 Measurement Circuit

$V_{CC1} = V_{CC2} = 3\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.2 In 1 to 3 Waits Setting and When Accessing External Area

Table 5.56 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.27		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

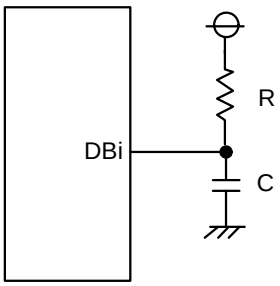
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.
When n = 1, $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

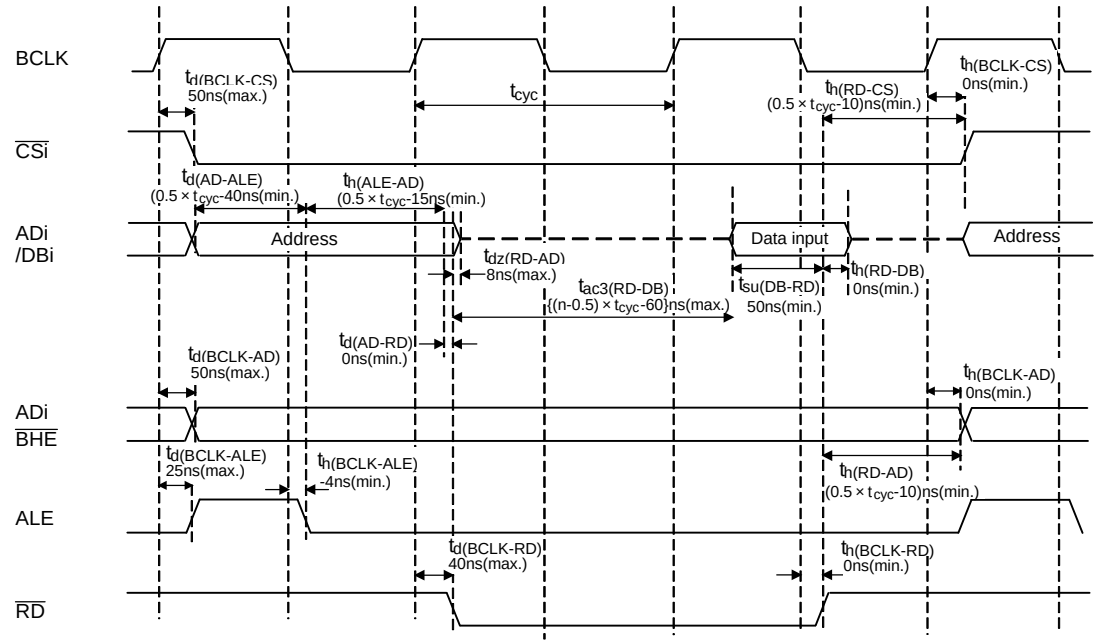
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



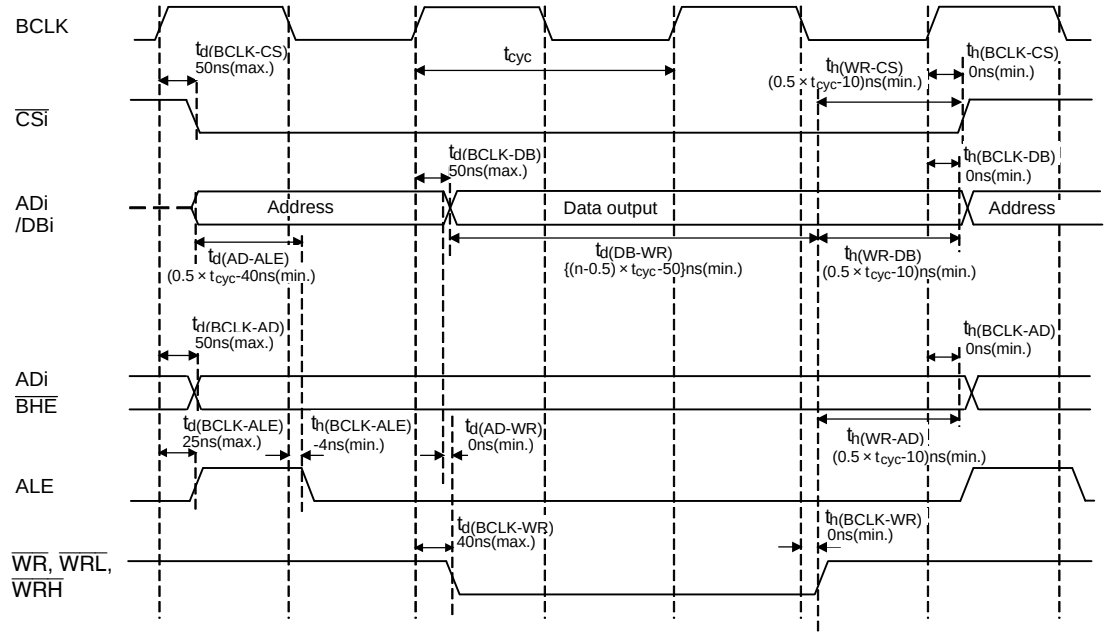
Memory Expansion Mode and Microprocessor Mode
(in 2 or 3 waits setting, and when accessing external area and using multiplexed bus)

$V_{CC1} = V_{CC2} = 3V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 2 (when 2 waits)
3 (when 3 waits)

Figure 5.30 Timing Diagram

REVISION HISTORY	M16C/64A Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.01	Feb 03, 2009	-	First Edition issued.
1.10	Jul 15, 2009	-	Watchdog Timer Reset Register → Watchdog Timer Refresh Register
		3	Table 1.2 Specifications for the 100-Pin Package (2/2) partially modified
		4	Table 1.3 Product List partially modified
		5	Figure 1.2 Marking Diagram (Top View) partially modified
		18	Figure 3.2 Memory Map 13800h → 13000h
		20	Table 4.1 “SFR Information (1/16)” reset value in VCR1 modified
		21	Table 4.2 “SFR Information (2/16)” partially modified
		29	Table 4.10 “SFR Information (10/16)” reset value in S11 modified
		37	Table 5.1 Absolute Maximum Ratings partially modified
		38	Table 5.2 Recommended Operating Conditions (1/3) partially modified
		39	Table 5.3 Recommended Operating Conditions (2/3) partially modified
		40	Table 5.4 Recommended Operating Conditions (3/3) added
		40	Figure 5.1 Ripple Waveform added
		41	Table 5.5 A/D Conversion Characteristics (1/2) partially modified
		41	Figure 5.2 A/D Accuracy Measure Circuit added
		42	Table 5.6 A/D Conversion Characteristics (2/2) partially modified
		44	Table 5.8 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$) partially modified
		44	Table 5.9 Flash Memory (Program ROM 1, 2) Electrical Characteristics notes modified
		46	Table 5.11 Voltage Detector 0 Electrical Characteristics partially modified
		46	Table 5.12 Voltage Detector 1 Electrical Characteristics partially modified
		47	Table 5.13 Voltage Detector 2 Electrical Characteristics partially modified
		47	Table 5.14 Power-On Reset Circuit partially modified
		48	Figure 5.3 Power-On Reset Circuit Electrical Characteristics partially modified
		50	Table 5.16 125 kHz On-Chip Oscillator Circuit Electrical Characteristics partially modified
		53	Table 5.19 Electrical Characteristics (3) partially modified
		54	Table 5.20 Electrical Characteristics (4) partially modified
		55	5.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input) added
		69	Table 5.37 Electrical Characteristics (1) partially modified
		70	Table 5.38 Electrical Characteristics (2) partially modified
		71	Table 5.39 Electrical Characteristics (3) partially modified
		73	5.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input) added
			Same modifications made to both 3 V and 5 V specifications.
2.00	Feb 07, 2011	Overall	001Ah Voltage Detector Operation Enable Register: Changed reset value from “000X 0000b”.
		Overall	002Ah Voltage Monitor 0 Control Register: Changed reset value from “1100 XX10b”.
		Overall	002Bh Voltage Monitor 1 Control Register: Changed reset value from “1000 1X10b”.
		Overall	0324h Increment/Decrement Flag: Changed name from Up/Down Flag.
		Overall	033Eh Timer B2 Special Mode Register: Changed reset value from “XX00 0000b”.
		Overall	03A2h Open-Circuit Detection Assist Function Register: Changed reset value from “XXXX XX00b”.
		Overall	03DCh D/A Control Register: Changed reset value from “XXXX XX00b”.
		Overall	D08Ah to D08Bh PMC0 Counter Value Register: Deleted.
		Overall	D09Eh to D09Fh PMC1 Counter Value Register: Deleted.
		Overall	Changed “high-speed clock mode” to “fast-mode”.
		Overview	
		3	Table 1.2 Specifications for the 100-Pin Package (2/2): Deleted note 1.
		4	Table 1.3 Product List: Added the new part numbers.
		5	Figure 1.1 Part No., with Memory Size and Package: Added “K” to the Memory capacity.
		11	Table 1.6 Pin Functions for the 100-Pin Package (1/3): Changed the description of $\overline{\text{HOLD}}$ pin.