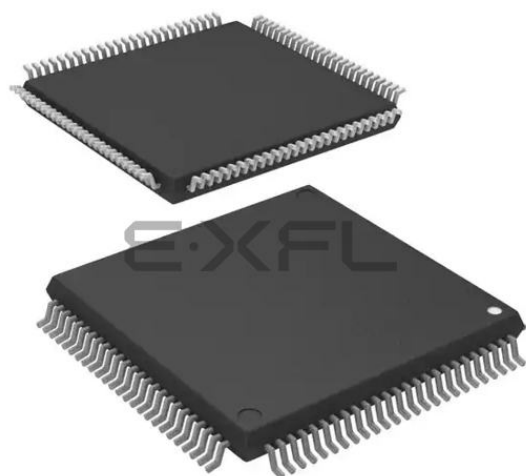




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Details

Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I ² C, SIO, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f364aenfb-30

Table 1.4 Pin Names for the 100-Pin Package (1/2)

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
1	99		P9_6			SOUT4	ANEX1	
2	100		P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN/PWM1		DA1	
4	2		P9_3		TB3IN/PWM0		DA0	
5	3		P9_2		TB2IN/PMC0	SOUT3		
6	4		P9_1		TB1IN/PMC1	SIN3		
7	5		P9_0		TB0IN	CLK3		
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	RESET						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	NMI	SD	CEC		
18	16		P8_4	INT2	ZP			
19	17		P8_3	INT1				
20	18		P8_2	INT0				
21	19		P8_1		TA4IN/U	CTS5/RTS5		
22	20		P8_0		TA4OUT/U	RXD5/SCL5		
23	21		P7_7		TA3IN	CLK5		
24	22		P7_6		TA3OUT	TXD5/SDA5		
25	23		P7_5		TA2IN/W			
26	24		P7_4		TA2OUT/W			
27	25		P7_3		TA1IN/V	CTS2/RTS2		
28	26		P7_2		TA1OUT/V	CLK2		
29	27		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
30	28		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			CTS1/RTS1/CTS0/CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0		RTCOUT	CTS0/RTS0		
39	37	CLKOUT	P5_7					RDY
40	38		P5_6					ALE
41	39		P5_5					HOLD
42	40		P5_4					HLDA
43	41		P5_3					BCLK
44	42		P5_2					RD
45	43		P5_1					WRH/BHE
46	44		P5_0					WRL/WR
47	45		P4_7		PWM1	TXD7/SDA7		CS3
48	46		P4_6		PWM0	RXD7/SCL7		CS2
49	47		P4_5			CLK7		CS1
50	48		P4_4			CTS7/RTS7		CS0

3. Address Space

3.1 Address Space

The M16C/64A Group has a 1 MB address space from 00000h to FFFFFh. Address space is expandable to 4 MB with the memory area expansion function. Addresses 40000h to BFFFFh can be used as external areas from bank 0 to bank 7. Figure 3.1 shows the Address Space. Areas that can be accessed vary depending on processor mode and the status of each control bit.

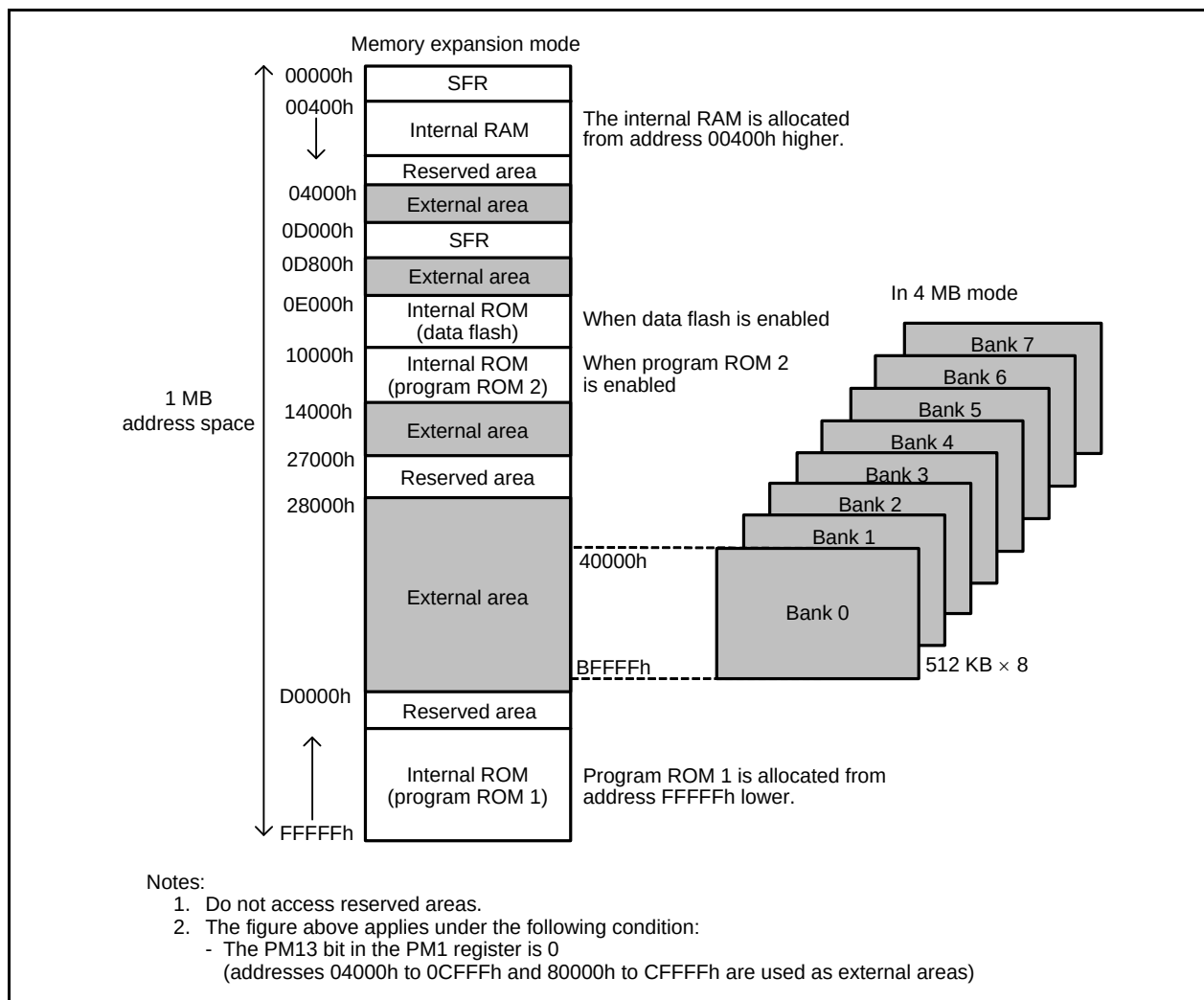


Figure 3.1 Address Space

4. Special Function Registers (SFRs)

4.1 SFRs

An SFR is a control register for a peripheral function.

Table 4.1 SFR Information (1) ⁽¹⁾

Address	Register	Symbol	Reset Value
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	0000 0000b (CNVSS pin is low) 0000 0011b (CNVSS pin is high) ⁽²⁾
0005h	Processor Mode Register 1	PM1	0000 1000b
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h	Chip Select Control Register	CSR	01h
0009h			
000Ah	Protect Register	PRCR	00h
000Bh	Data Bank Register	DBR	00h
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b ⁽³⁾
000Dh			
000Eh			
000Fh			
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b
0011h			
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0013h			
0014h			
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
0016h			
0017h			
0018h	Reset Source Determine Register	RSTFR	XX00 001Xb (hardware reset) ⁽⁴⁾
0019h	Voltage Detector 2 Flag Register	VCR1	0000 1000b ⁽⁵⁾
001Ah	Voltage Detector Operation Enable Register	VCR2	00h ⁽⁵⁾
001Bh	Chip Select Expansion Control Register	CSE	00h
001Ch	PLL Control Register 0	PLC0	0X01 X010b
001Dh			
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
001Fh			

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. Software reset, watchdog timer reset, oscillator stop detect reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect the following bits: bits PM01 and PM00 in the PM0 register.
3. Oscillator stop detect reset does not affect bits CM20, CM21, and CM27.
4. The state of bits in the RSTFR register depends on the reset type.
5. This is the reset value after hardware reset. Refer to the explanation of each register for details.

Table 4.3 SFR Information (3) ⁽¹⁾

Address	Register	Symbol	Reset Value
0040h			
0041h			
0042h	INT7 Interrupt Control Register	INT7IC	XX00 X000b
0043h	INT6 Interrupt Control Register	INT6IC	XX00 X000b
0044h	INT3 Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC U1BCNIC	XXXX X000b
0047h	Timer B3 Interrupt Control Register UART0 Bus Collision Detection Interrupt Control Register	TB3IC U0BCNIC	XXXX X000b
0048h	SI/O4 Interrupt Control Register INT5 Interrupt Control Register	S4IC INT5IC	XX00 X000b
0049h	SI/O3 Interrupt Control Register INT4 Interrupt Control Register	S3IC INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
005Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
005Fh	INT2 Interrupt Control Register	INT2IC	XX00 X000b

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.6 SFR Information (6) ⁽¹⁾

Address	Register	Symbol	Reset Value
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.8 SFR Information (8) ⁽¹⁾

Address	Register	Symbol	Reset Value
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0213h			
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0217h			
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Bh			
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
021Fh			
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.12 SFR Information (12) ⁽¹⁾

Address	Register	Symbol	Reset Value
0300h	Timer B3/B4/B5 Count Start Flag	TBSR	000X XXXXb
0301h			
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
030Fh			
0310h	Timer B3 Register	TB3	XXh
0311h			XXh
0312h	Timer B4 Register	TB4	XXh
0313h			XXh
0314h	Timer B5 Register	TB5	XXh
0315h			XXh
0316h			
0317h			
0318h	Port Function Control Register	PFCR	0011 1111b
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	00h
0321h			
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Increment/Decrement Flag	UDF	00h
0325h			
0326h	Timer A0 Register	TA0	XXh
0327h			XXh
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Ch	Timer A3 Register	TA3	XXh
032Dh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.13 SFR Information (13) ⁽¹⁾

Address	Register	Symbol	Reset Value
0330h	Timer B0 Register	TB0	XXh
0331h			XXh
0332h	Timer B1 Register	TB1	XXh
0333h			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
033Eh	Timer B2 Special Mode Register	TB2SC	X000 0000b
033Fh			
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0347h			
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h	CEC Function Control Register 1	CECC1	XXXX X000b
0351h	CEC Function Control Register 2	CECC2	00h
0352h	CEC Function Control Register 3	CECC3	XXXX 0000b
0353h	CEC Function Control Register 4	CECC4	00h
0354h	CEC Flag Register	CECFLG	00h
0355h	CEC Interrupt Source Select Register	CISEL	00h
0356h	CEC Transmit Buffer Register 1	CCTB1	00h
0357h	CEC Transmit Buffer Register 2	CCTB2	XXXX XX00b
0358h	CEC Receive Buffer Register 1	CCRB1	00h
0359h	CEC Receive Buffer Register 2	CCRB2	XXXX X000b
035Ah	CEC Receive Follower Address Set Register 1	CRADRI1	00h
035Bh	CEC Receive Follower Address Set Register 2	CRADRI2	00h
035Ch			
035Dh			
035Eh			
035Fh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.16 SFR Information (16) ⁽¹⁾

Address	Register	Symbol	Reset Value
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D5h			
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b
03D8h	D/A0 Register	DA0	00h
03D9h			
03DAh	D/A1 Register	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

5.1.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions (1/3)

$V_{CC1} = V_{CC2} = 2.7$ to 5.5 V at $T_{opr} = -20^{\circ}\text{C}$ to 85°C / -40°C to 85°C unless otherwise specified.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1} , V_{CC2}	Supply voltage ($V_{CC1} \geq V_{CC2}$)	CEC function is not used	2.7	5.0	5.5	V
		CEC function is used	2.7		3.63	V
AV_{CC}	Analog supply voltage			V_{CC1}		V
V_{SS}	Supply voltage			0		V
AV_{SS}	Analog supply voltage			0		V
V_{IH}	High input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7	$0.8V_{CC2}$		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode)	$0.8V_{CC2}$		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor modes)	$0.5V_{CC2}$		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS, BYTE	$0.8V_{CC1}$		V_{CC1}	V
		P7_0, P7_1, P8_5	$0.8V_{CC1}$		6.5	V
		CEC	$0.7V_{CC1}$			V
V_{IL}	Low input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7	0		$0.2V_{CC2}$	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode)	0		$0.2V_{CC2}$	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor mode)	0		$0.16V_{CC2}$	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS, BYTE	0		$0.2V_{CC1}$	V
		CEC			$0.26V_{CC1}$	V
$I_{OH(sum)}$	High peak output current	Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7			-40.0	mA
		Sum of $I_{OH(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7			-40.0	mA
		Sum of $I_{OH(peak)}$ at P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4			-40.0	mA
		Sum of $I_{OH(peak)}$ at P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			-40.0	mA
$I_{OH(peak)}$	High peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			-10.0	mA
$I_{OH(avg)}$	High average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			-5.0	mA

Note:

1. The average output current is the mean value within 100 ms.

Table 5.10 Flash Memory (Data Flash) Electrical Characteristics

$V_{CC1} = 2.7$ to 5.5 V at $T_{opr} = -20$ to $85^{\circ}\text{C}/-40$ to 85°C , unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	$V_{CC1} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$	10,000 (2)			times
-	2 word program time	$V_{CC1} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		300	4000	μs
-	Lock bit program time	$V_{CC1} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		140	3000	μs
-	Block erase time	$V_{CC1} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		0.2	3.0	s
-	Program, erase voltage		2.7		5.5	V
-	Read voltage		2.7		5.5	V
-	Program, erase temperature		-20/-40		85	$^{\circ}\text{C}$
t_{PS}	Flash memory circuit stabilization wait time				50	μs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:

- Definition of program and erase cycles
The program and erase cycles refer to the number of per-block erasures.
If the program and erase cycles are n ($n = 10,000$), each block can be erased n times.
For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
- Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
- The data hold time includes time that the power supply is off or the clock is not supplied.

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Table 5.20 Electrical Characteristics (4)

R5F364AKNFA, R5F364AKNFB, R5F364AKDFA, R5F364AKDFB

R5F364AMNFA, R5F364AMNFB, R5F364AMDFA, R5F364AMDFB

 $V_{CC1} = V_{CC2} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$ at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C , $f_{(BCLK)} = 25 \text{ MHz}$ unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)} = 25 \text{ MHz}$ XIN = 4.2 MHz (square wave), PLL multiplied by 6 125 kHz on-chip oscillator stopped	22.0		mA
			$f_{(BCLK)} = 25 \text{ MHz}$, A/D conversion XIN = 4.2 MHz (square wave), PLL multiplied by 6 125 kHz on-chip oscillator stopped	22.7		mA
			$f_{(BCLK)} = 20 \text{ MHz}$ XIN = 20 MHz (square wave) 125 kHz on-chip oscillator stopped	17.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)	550.0		μA
		Low-power mode	$f_{(BCLK)} = 32 \text{ kHz}$ In low-power mode FMR22 = FMR23 = 1 on flash memory ⁽¹⁾	170.0		μA
			$f_{(BCLK)} = 32 \text{ kHz}$ In low-power mode on RAM ⁽¹⁾	45.0		μA
		Wait mode	Main clock stopped 125 kHz on-chip oscillator on Peripheral clock operating $T_{opr} = 25^{\circ}\text{C}$	20.5		μA
			$f_{(BCLK)} = 32 \text{ kHz}$ (oscillation capacity High) 125 kHz on-chip oscillator stopped Peripheral clock operating $T_{opr} = 25^{\circ}\text{C}$	11.0		μA
			$f_{(BCLK)} = 32 \text{ kHz}$ (oscillation capacity low) 125 kHz on-chip oscillator stopped Peripheral clock operating $T_{opr} = 25^{\circ}\text{C}$	6.0		μA
		Stop mode	Main clock stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped $T_{opr} = 25^{\circ}\text{C}$	1.7		μA
		During flash memory program	$f_{(BCLK)} = 10 \text{ MHz}$, PM17 = 1 (one wait) $V_{CC1} = 5.0 \text{ V}$	20.0		mA
		During flash memory erase	$f_{(BCLK)} = 10 \text{ MHz}$, PM17 = 1 (one wait) $V_{CC1} = 5.0 \text{ V}$	30.0		mA

Note:

1. This indicates the memory in which the program to be executed exists.

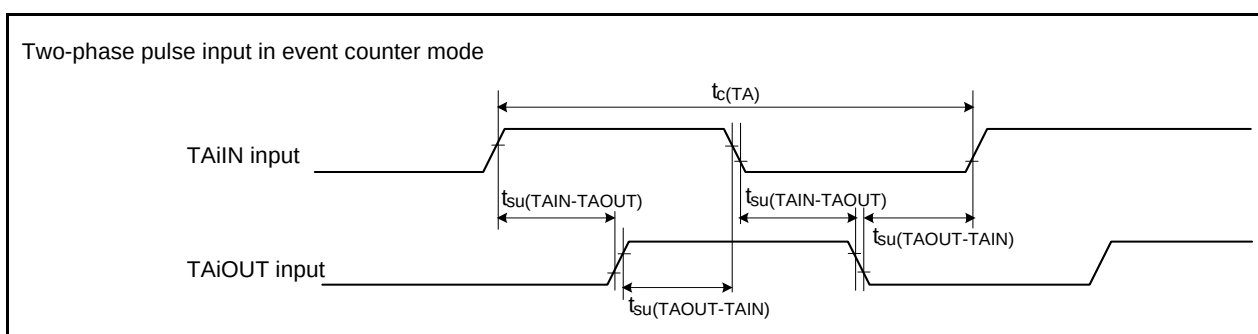
$$V_{CC1} = V_{CC2} = 5\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

Table 5.27 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

**Figure 5.8 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

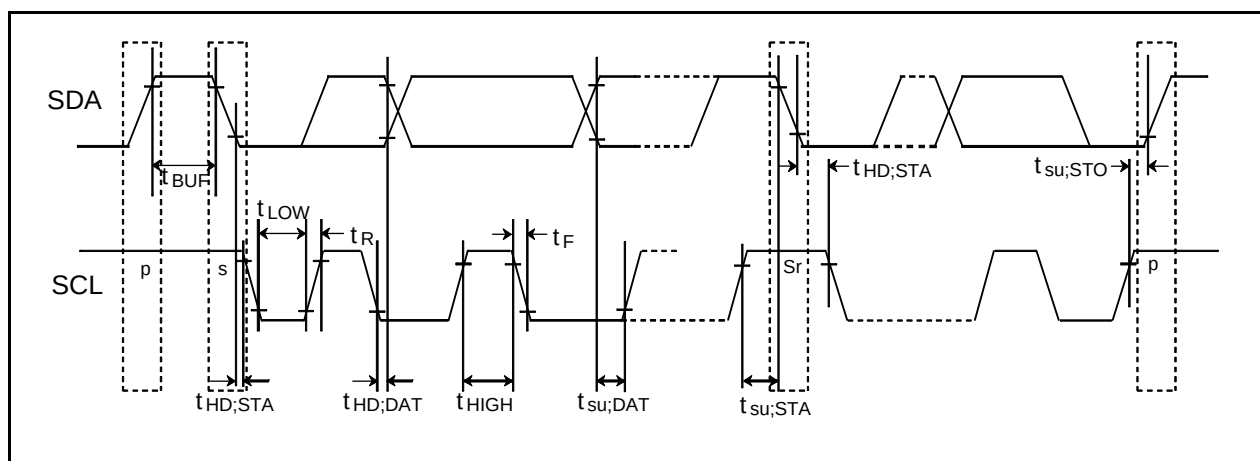
$$V_{CC1} = V_{CC2} = 5\text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.2.2.7 Multi-master I²C-bus**Table 5.33 Multi-master I²C-bus**

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		μs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		μs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		μs
t_R	SCL, SDA signals' rising time		1000	$20 + 0.1 C_b$	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	μs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		μs
t_F	SCL, SDA signals' falling time		300	$20 + 0.1 C_b$	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		μs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		μs

**Figure 5.12 Multi-master I²C-bus**

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5 \text{ V}$, $V_{SS} = 0 \text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.2.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

Table 5.34 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with 1 to 3 waits)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{su(DB-RD)}$	Data input setup time	40		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	80		ns
$t_h(RD-DB)$	Data input hold time	0		ns
$t_h(BCLK-RDY)$	$\overline{RDY}$ input hold time	0		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(BCLK)}} - 45[ns] \quad n \text{ is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 45[ns] \quad n \text{ is 2 for 2 waits setting, and 3 for 3 waits setting.}$$

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

5.2.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode)

($V_{CC1} = V_{CC2} = 5 \text{ V}$, $V_{SS} = 0 \text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.2.4.1 In No Wait State Setting

Table 5.35 Memory Expansion Mode and Microprocessor Mode (in No Wait State Setting)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.14		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) ⁽³⁾		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) ⁽³⁾		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^{-9}}{f_{(BCLK)}} - 40[\text{ns}] \quad f_{(BCLK)} \text{ is 12.5 MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^{-9}}{f_{(BCLK)}} - 10[\text{ns}]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

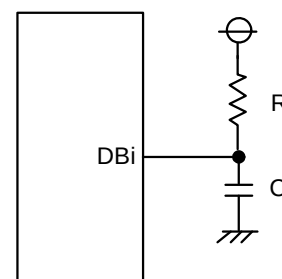
Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2V_{CC2}$, $C = 30 \text{ pF}$, $R = 1 \text{ k}\Omega$, hold time of output low level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2}) \\ = 6.7 \text{ ns.}$$



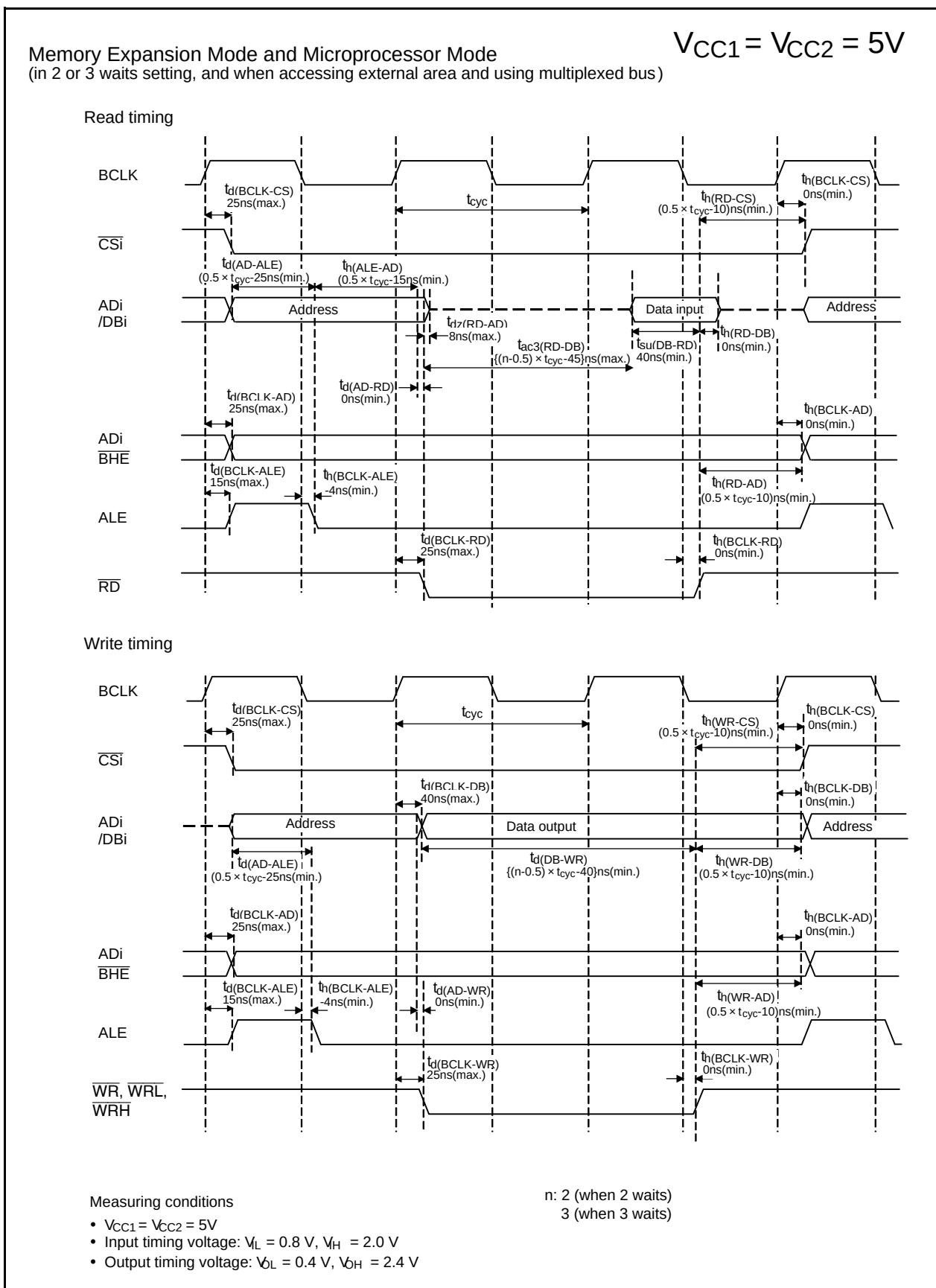


Figure 5.17 Timing Diagram

$$V_{CC1} = V_{CC2} = 3 \text{ V}$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3 \text{ V}$, $V_{SS} = 0 \text{ V}$, at $T_{opr} = -20^{\circ}\text{C}$ to $85^{\circ}\text{C}/-40^{\circ}\text{C}$ to 85°C unless otherwise specified)

5.3.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

Table 5.54 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1}(\text{RD-DB})$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2}(\text{RD-DB})$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3}(\text{RD-DB})$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{su}(\text{DB-RD})$	Data input setup time	50		ns
$t_{su}(\text{RDY-BCLK})$	$\overline{\text{RDY}}$ input setup time	85		ns
$t_h(\text{RD-DB})$	Data input hold time	0		ns
$t_h(\text{BCLK-RDY})$	$\overline{\text{RDY}}$ input hold time	0		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

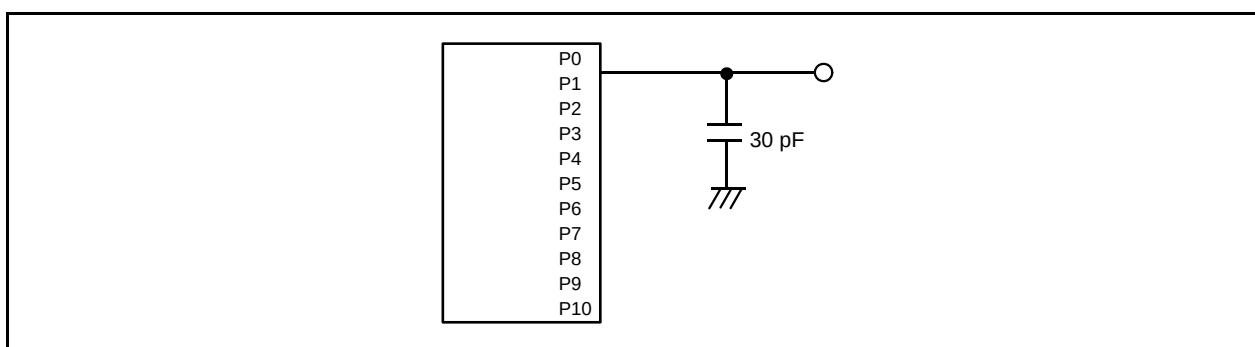
$$\frac{0.5 \times 10^9}{f_{(\text{BCLK})}} - 60[\text{ns}]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(\text{BCLK})}} - 60[\text{ns}] \quad n \text{ is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(\text{BCLK})}} - 60[\text{ns}] \quad n \text{ is 2 for 2 waits setting, 3 for 3 waits setting.}$$

**Figure 5.27 Ports P0 to P10 Measurement Circuit**

REVISION HISTORY	M16C/64A Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.01	Feb 03, 2009	-	First Edition issued.
1.10	Jul 15, 2009	-	Watchdog Timer Reset Register → Watchdog Timer Refresh Register
		3	Table 1.2 Specifications for the 100-Pin Package (2/2) partially modified
		4	Table 1.3 Product List partially modified
		5	Figure 1.2 Marking Diagram (Top View) partially modified
		18	Figure 3.2 Memory Map 13800h → 13000h
		20	Table 4.1 "SFR Information (1/16)" reset value in VCR1 modified
		21	Table 4.2 "SFR Information (2/16)" partially modified
		29	Table 4.10 "SFR Information (10/16)" reset value in S11 modified
		37	Table 5.1 Absolute Maximum Ratings partially modified
		38	Table 5.2 Recommended Operating Conditions (1/3) partially modified
		39	Table 5.3 Recommended Operating Conditions (2/3) partially modified
		40	Table 5.4 Recommended Operating Conditions (3/3) added
		40	Figure 5.1 Ripple Waveform added
		41	Table 5.5 A/D Conversion Characteristics (1/2) partially modified
		41	Figure 5.2 A/D Accuracy Measure Circuit added
		42	Table 5.6 A/D Conversion Characteristics (2/2) partially modified
		44	Table 5.8 CPU Clock When Operating Flash Memory (f_{BCLK}) partially modified
		44	Table 5.9 Flash Memory (Program ROM 1, 2) Electrical Characteristics notes modified
		46	Table 5.11 Voltage Detector 0 Electrical Characteristics partially modified
		46	Table 5.12 Voltage Detector 1 Electrical Characteristics partially modified
		47	Table 5.13 Voltage Detector 2 Electrical Characteristics partially modified
		47	Table 5.14 Power-On Reset Circuit partially modified
		48	Figure 5.3 Power-On Reset Circuit Electrical Characteristics partially modified
		50	Table 5.16 125 kHz On-Chip Oscillator Circuit Electrical Characteristics partially modified
		53	Table 5.19 Electrical Characteristics (3) partially modified
		54	Table 5.20 Electrical Characteristics (4) partially modified
		55	5.2.2.1 Reset Input (RESET Input) added
		69	Table 5.37 Electrical Characteristics (1) partially modified
		70	Table 5.38 Electrical Characteristics (2) partially modified
		71	Table 5.39 Electrical Characteristics (3) partially modified
		73	5.3.2.1 Reset Input (RESET Input) added
			Same modifications made to both 3 V and 5 V specifications.
2.00	Feb 07, 2011	Overall	001Ah Voltage Detector Operation Enable Register: Changed reset value from "000X 0000b".
		Overall	002Ah Voltage Monitor 0 Control Register: Changed reset value from "1100 XX10b".
		Overall	002Bh Voltage Monitor 1 Control Register: Changed reset value from "1000 1X10b".
		Overall	0324h Increment/Decrement Flag: Changed name from Up/Down Flag.
		Overall	033Eh Timer B2 Special Mode Register: Changed reset value from "XX00 0000b".
		Overall	03A2h Open-Circuit Detection Assist Function Register: Changed reset value from "XXXX XX00b".
		Overall	03DCh D/A Control Register: Changed reset value from "XXXX XX00b".
		Overall	D08Ah to D08Bh PMC0 Counter Value Register: Deleted.
		Overall	D09Eh to D09Fh PMC1 Counter Value Register: Deleted.
		Overall	Changed "high-speed clock mode" to "fast-mode".
		Overview	
		3	Table 1.2 Specifications for the 100-Pin Package (2/2): Deleted note 1.
		4	Table 1.3 Product List: Added the new part numbers.
		5	Figure 1.1 Part No., with Memory Size and Package: Added "K" to the Memory capacity.
		11	Table 1.6 Pin Functions for the 100-Pin Package (1/3): Changed the description of HOLD pin.