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What is "Embedded - Microcontrollers"?

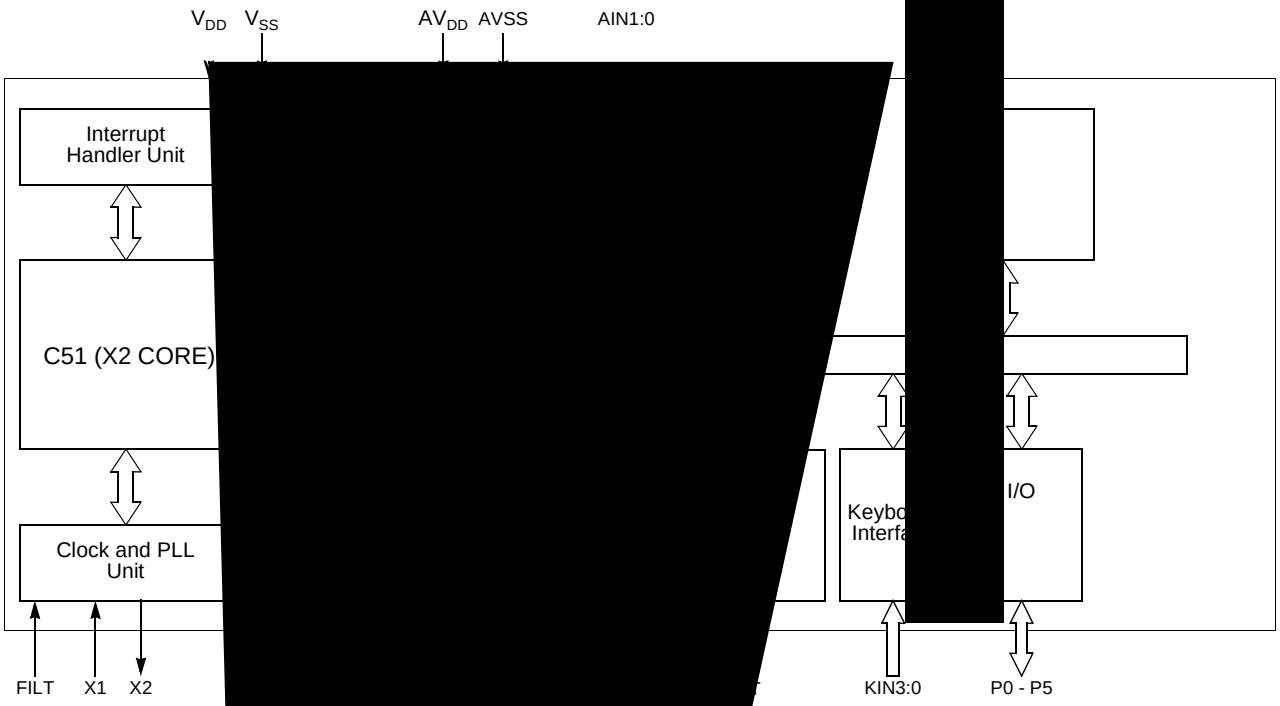
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	20MHz
Connectivity	IDE/ATAPI, I²C, Memory Card, PCM, SPI, UART/USART, USB
Peripherals	I²S, POR, WDT
Number of I/O	44
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5132-rorul

Block Diagram

Figure 1. AT89C5132 Block Diagram



Notes: 1. Alternate function
2. Alternate function
3. Alternate function

Table 3. Timer 0 and Timer 1 Signal Description

Signal Name	Type	Description	Alternate Function
$\overline{\text{INT0}}$	I	**Timer 0 Gate Input** $\overline{\text{INT0}}$ serves as external run control for timer 0, when selected by GATE0 bit in TCON register. **External Interrupt 0** $\overline{\text{INT0}}$ input sets IE0 in the TCON register. If bit IT0 in this register is set, bit IE0 is set by a falling edge on INT0#. If bit IT0 is cleared, bit IE0 is set by a low level on INT0#.	P3.2
$\overline{\text{INT1}}$	I	**Timer 1 Gate Input** $\overline{\text{INT1}}$ serves as external run control for timer 1, when selected by GATE1 bit in TCON register. **External Interrupt 1** $\overline{\text{INT1}}$ input sets IE1 in the TCON register. If bit IT1 in this register is set, bit IE1 is set by a falling edge on INT1#. If bit IT1 is cleared, bit IE1 is set by a low level on INT1#.	P3.3
T0	I	**Timer 0 External Clock Input** When timer 0 operates as a counter, a falling edge on the T0 pin increments the count.	P3.4
T1	I	**Timer 1 External Clock Input** When timer 1 operates as a counter, a falling edge on the T1 pin increments the count.	P3.5

Table 4. Audio Interface Signal Description

Signal Name	Type	Description	Alternate Function
DCLK	O	**DAC Data Bit Clock**	-
DOUT	O	**DAC Audio Data**	-
DSEL	O	**DAC Channel Select Signal** DSEL is the sample rate clock output.	-
SCLK	O	**DAC System Clock** SCLK is the oversampling clock synchronized to the digital audio data (DOUT) and the channel selection signal (DSEL).	-

Table 5. USB Controller Signal Description

Signal Name	Type	Description	Alternate Function
D+	I/O	**USB Positive Data Upstream Port** This pin requires an external 1.5 KΩ pull-up to V_{DD} for full speed operation.	-
D-	I/O	**USB Negative Data Upstream Port**	-

Table 6.

Table 7. MutiMediaCard Interface Signal Description

Signal Name	Type	Description	Alternate Function
MCLK	O	**MMC Clock output** Data or command clock transfer.	-
MCMD	I/O	**MMC Command line** Bidirectional command channel used for card initialization and data transfer commands. To avoid any parasitic current consumption, unused MCMD input must be polarized to V_{DD} or V_{SS}.	-
MDAT	I/O	**MMC Data line** Bidirectional data channel. To avoid any parasitic current consumption, unused MDAT input must be polarized to V_{DD} or V_{SS}.	-

Table 8. UART Signal Description

Signal Name	Type	Description	Alternate Function
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
TXD	O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1

Table 9. SPI Controller Signal Description

Signal Name	Type	Description	Alternate Function
MISO	I/O	**SPI Master Input Slave Output Data Line** When in master mode, MISO receives data from the slave peripheral. When in slave mode, MISO outputs data to the master controller.	P4.0
MOSI	I/O	**SPI Master Output Slave Input Data Line** When in master mode, MOSI outputs data to the slave peripheral. When in slave mode, MOSI receives data from the master controller.	P4.1
SCK	I/O	**SPI Clock Line** When in master mode, SCK outputs clock to the slave peripheral. When in slave mode, SCK receives clock from the master controller.	P4.2
$\overline{SS}$	I	**SPI Slave Select Line** When in controlled slave mode, $\overline{SS}$ enables the slave mode.	P4.3

Table 10. TWI Controller Signal Description

Signal Name	Type	Description	Alternate Function
SCL	I/O	**TWI Serial Clock** When TWI controller is in master mode, SCL outputs the serial clock to the slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller.	P1.6
SDA	I/O	**TWI Serial Data** SDA is the bidirectional Two Wire data line.	P1.7

Table 11. A/D Converter Signal Description

Signal Name	Type	Description	Alternate Function
AIN1:0	I	**A/D Converter Analog Inputs**	-
AREFP	I	**Analog Positive Voltage Reference Input**	-
AREFN	I	**Analog Negative Voltage Reference Input** This pin is internally connected to AVSS.	-

Table 12. Keypad Interface Signal Description

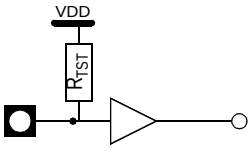
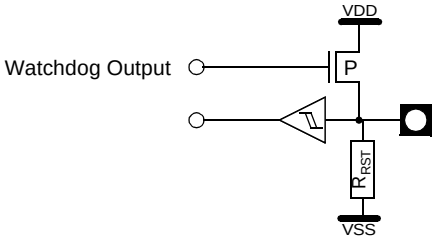
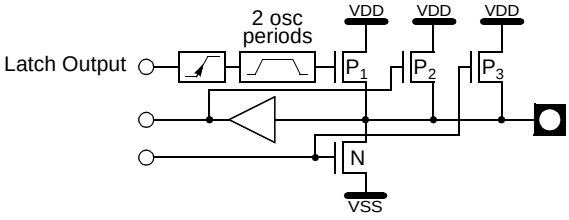
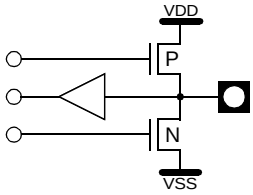
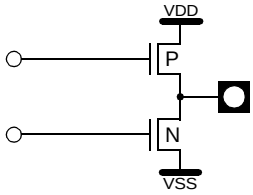
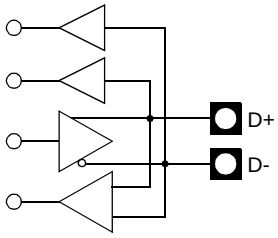
Signal Name	Type	Description	Alternate Function
KIN3:0	I	**Keypad Input Lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt.	P1.3:0

Table 13. External Access Signal Description

Signal Name	Type	Description	Alternate Function
A15:8	I/O	**Address Lines** Upper address lines for the external bus. Multiplexed higher address and data lines for the IDE interface.	P2.7:0
AD7:0	I/O	**Address/Data Lines** Multiplexed lower address and data lines for the external memory or the IDE interface.	P0.7:0
ALE	O	**Address Latch Enable Output** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A7:0. An external latch is used to demultiplex the address from address/data bus.	-
$\overline{\text{ISP}}$	I/O	**ISP Enable Input** This signal must be held to GND through a pull-down resistor at the falling reset to force execution of the internal bootloader.	-
$\overline{\text{RD}}$	O	**Read Signal** Read signal asserted during external data memory read operation.	P3.7
$\overline{\text{WR}}$	O	**Write Signal** Write signal asserted during external data memory write operation.	P3.6

Internal Pin Structure

Table 16. Detailed Internal Pin Structure

Circuit[1]	Type	Pins
	Input	$\overline{TST}$
	Input/Output	RST
	Input/Output	P1[2] P2[3] P3 P4 P53:0
	Input/Output	P0 MCMD MDAT $\overline{ISP}$ $\overline{PSEN}$
	Output	ALE SCLK DCLK DOUT DSEL MCLK
	Input/Output	D+ D-

Notes:
1. For information on resistors value, input/output levels, and drive capability, refer to the Section “DC Characteristics”, page 183.
2. When the Two Wire controller is enabled, P_1, P_2, and P_3 transistors are disabled allowing pseudo open-drain structure.
3. In Port 2, P_1 transistor is continuously driven when outputting a high level bit address (A15:8).

Address Spaces

The AT8xC5132 derivatives implement four different address spaces:

- Program/Code Memory
- Boot Memory
- Data Memory
- Special Function Registers (SFRs)

Code Memory

The AT89C5132 implements 64K Bytes of on-chip program/code memory in Flash technology.

The Flash memory increases ROM functionality by enabling in-circuit electrical erasure and programming. Thanks to the internal charge pump, the high voltage needed for programming or erasing Flash cells is generated on-chip using the standard V_{DD} voltage. Thus, the AT89C5132 can be programmed using only one voltage and allows in application software programming commonly known as IAP. Hardware programming mode is also available using specific programming tools.

Boot Memory

The AT89C5132 implements 4K Bytes of on-chip boot memory provided in Flash technology. This boot memory is delivered programmed with a standard bootloader software allowing in system programming commonly known as ISP. It also contains some Application Programming Interfaces routines commonly known as API allowing user to develop his own bootloader.

Data Memory

The AT89C5132 derivatives implement 2304 bytes of on-chip data RAM. This memory is divided in two separate areas:

- 256 bytes of on-chip RAM memory (standard C51 memory).
- 2048 bytes of on-chip expanded RAM memory (ERAM accessible via MOVX instructions).

Peripherals

The AT8xC5132 peripherals are briefly described in the following sections. For further details on how to interface (hardware and software) to these peripherals, please refer to the AT8xC5132 complete datasheet.

Clock Generator System

The AT8xC5132 internal clocks are extracted from an on-chip PLL fed by an on-chip oscillator. Four clocks are generated respectively for the C51 core, the audio interface, and the other peripherals. The C51 and peripheral clocks are derived from the oscillator clock. The audio interface sample rates are also obtained by dividing the PLL output clock.

Ports

The AT8xC5132 implement five 8-bit ports (P0 to P4) and one 4-bit port (P5). In addition to performing general-purpose I/Os, some ports are capable of external data memory operations; others allow for alternate functions. All I/O Ports are bidirectional. Each Port contains a latch, an output driver and an input buffer. Port 0 and Port 2 output drivers and input buffers facilitate external memory operations. Some Port 1, Port 3 and Port 4 pins serve for both general-purpose I/Os and alternate functions.

Timers/Counters

The AT8xC5132 implement the two general-purpose, 16-bit Timers/Counters of a standard C51. They are identified as Timer 0, Timer 1, and can independently be configured each to operate in a variety of modes as a Timer or as an event Counter. When operating as a Timer, a Timer/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

Watchdog Timer

The AT8xC5132 implement a hardware Watchdog Timer that automatically resets the chip if it is allowed to time out. The WDT provides a means of recovering from routines that do not complete successfully due to software or hardware malfunctions.

Audio Output Interface

The AT8xC5132 implements an audio output interface allowing the decoded audio bitstream to be output in various formats. They are compatible with right and left justification PCM and I^2S formats and the on-chip PLL allows connection of almost all commercial audio DAC families available on the market.

Universal Serial Bus Interface

The AT8xC5132 implements a full-speed Universal Serial Bus Interface. The USB interface can be used for the following purposes:

- Download of files by supporting the USB mass storage class.
- In-System Programming by supporting the USB firmware upgrade class.

MultiMedia Card Interface

The AT8xC5132 implements a MultiMedia Card (MMC) interface compliant to the V2.2 specification in MultiMedia Card mode. The MMC allows storage of files in removable Flash memory cards that can be easily plugged or removed from the application. It can also be used for In-System Programming.

IDE/ATAPI Interface

The AT8xC5132 provide an IDE/ATAPI interface allowing connection of devices such as CD-ROM reader, CompactFlash™ cards, Hard Disk Drive, etc. It consists of a 16-bit bidirectional bus part of the low-level ANSI ATA/ATAPI specification. It is provided for mass storage interface but could be used for In-System Programming using CD-ROM.

Table 1. Digital DC Characteristics
V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
I_{LI}	Input Leakage Current (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			10	µA	0.45< V_{IN}< V_{DD}
I_{TL}	Logical 1 to 0 Transition Current (P1, P2, P3, P4 and P5)			-650	µA	Vin = 2.0 V
R_{RST}	Pull-Down Resistor	50	90	200	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A= 25°C
V_{RET}	V_{DD} Data Retention Limit			1.8	V	
I_{DD}	Operating Current		(3)	X1 / X2 mode 6.5 / 10.5 8 / 13.5 9.5 / 17	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
I_{DL}	Idle Mode Current		(3)	X1 / X2 mode 5.3 / 8.1 6.4 / 10.3 7.5 / 13	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
I_{PD}	Power-Down Mode Current		20	500	µA	V_{RET} < V_{DD} < 3.3 V

Notes:
1. Typical values are obtained using V_{DD}= 3 V and T_A= 25°C. They are not tested and there is no guarantee on these values.
2. Flash retention is guaranteed with the same formula for V_{DD} min down to 0V.
3. See Table 154 for typical consumption in player mode.

I_{DD}, I_{DL} and I_{PD} Test Conditions

Figure 1. I_{DD} Test Condition, Active Mode

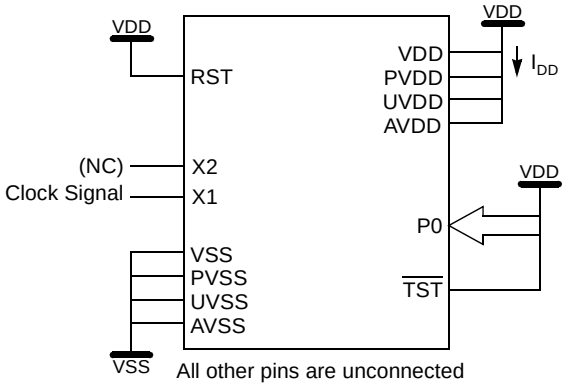


Table 3. External 8-bit Bus Cycle – Data Write AC Timings
V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLWL}	ALE Low to $\overline{WR}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{WHLH}	$\overline{WR}$ High to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	$7 \cdot T_{CLCL}$-20		$3.5 \cdot T_{CLCL}$-20		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{CLCL}-15		$0.5 \cdot T_{CLCL}$-15		ns

Waveforms

Figure 1. External 8-bit Bus Cycle – Data Read Waveforms

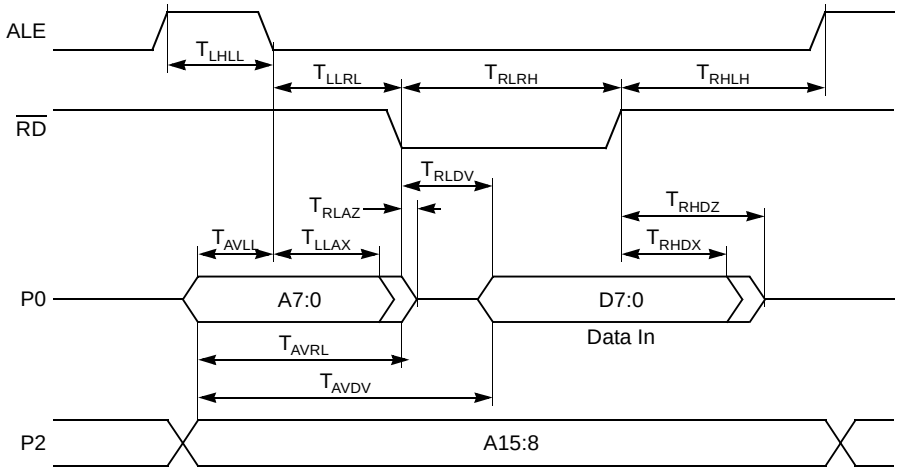
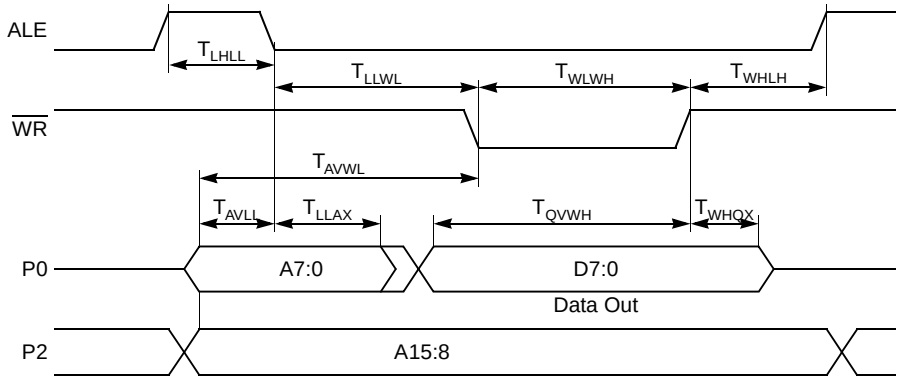


Figure 2. External 8-bit Bus Cycle – Data Write Waveforms



External IDE 16-bit Bus Cycles

Definition of Symbols

Table 4. External IDE 16-bit Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	$\overline{RD}$
W	$\overline{WR}$

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

Test conditions: capacitive load on all pins = 50 pF.

Table 5. External IDE 16-bit Bus Cycle – Data Read AC Timings
V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

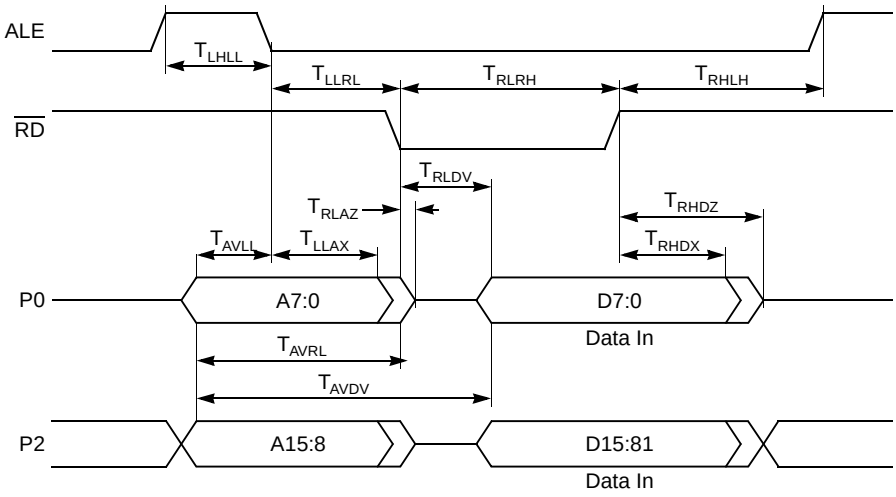
Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLRL}	ALE Low to $\overline{RD}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{RHLH}	$\overline{RD}$ high to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}$-65		$4.5 \cdot T_{CLCL}$-65	ns
T_{AVRL}	Address Valid to $\overline{RD}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{RLDV}	$\overline{RD}$ Low to Valid Data		$5 \cdot T_{CLCL}$-30		$2.5 \cdot T_{CLCL}$-30	ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
T_{RHDX}	Data Hold After $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Instruction Float After $\overline{RD}$ High		$2 \cdot T_{CLCL}$-25		T_{CLCL}-25	ns

Table 6. External IDE 16-bit Bus Cycle – Data Write AC Timings
V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLWL}	ALE Low to $\overline{WR}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{WHLH}	$\overline{WR}$ High to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	$7 \cdot T_{CLCL}$-20		$3.5 \cdot T_{CLCL}$-20		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{CLCL}-15		$0.5 \cdot T_{CLCL}$-15		ns

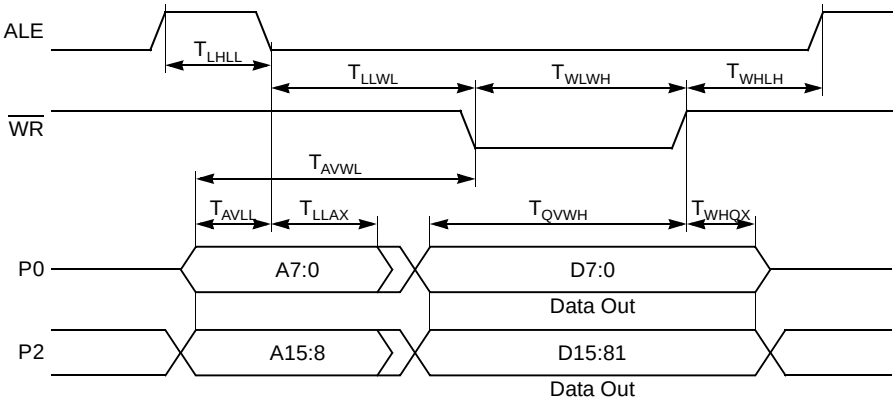
Waveforms

Figure 3. External IDE 16-bit Bus Cycle – Data Read Waveforms



Note: D15:8 is written in DAT16H SFR.

Figure 4. External IDE 16-bit Bus Cycle – Data Write Waveforms



Note: D15:8 is the content of DAT16H SFR.

SPI Interface

Definition of Symbols

Table 7. SPI Interface Timing Symbol Definitions

Signals	
C	Clock
I	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

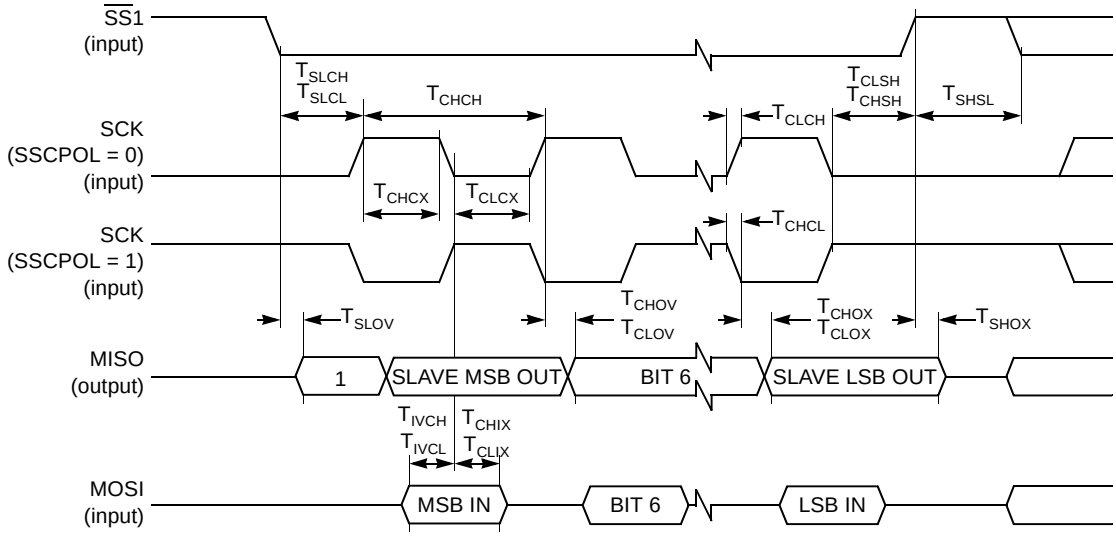
Timings

Table 8. SPI Interface Master AC Timing
V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Min	Max	Unit
Slave Mode				
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	$\overline{SS}$ Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	$\overline{SS}$ High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	$\overline{SS}$ Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after $\overline{SS}$ High		130	ns
T_{SHSL}	$\overline{SS}$ High to $\overline{SS}$ Low	(1)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise Time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master Mode				
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise Time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

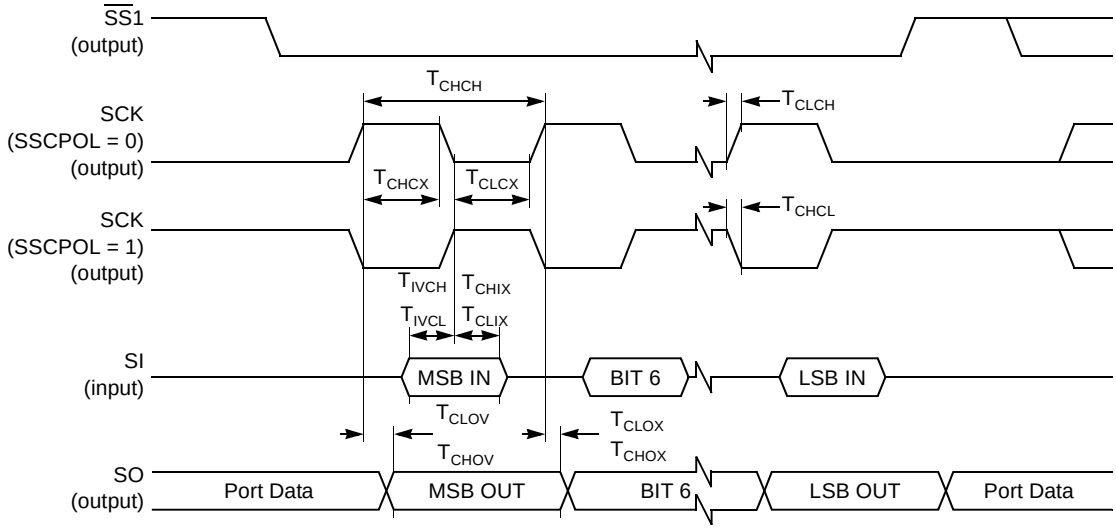
Notes: 1. Value of this parameter depends on software.
2. Test conditions: capacitive load on all pins = 100 pF

Figure 7. SPI Master Waveforms (SSCPHA = 0)



Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

Figure 8. SPI Master Waveforms (SSCPHA = 1)



Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

Two-wire Interface

Timings

Table 1. TWI Interface AC Timing

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	INPUT Min Max	OUTPUT Min Max
T_{HD}; STA	Start condition hold time	$14 \cdot T_{CLCL}$(4)	4.0 µs(1)
T_{LOW}	SCL low time	$16 \cdot T_{CLCL}$(4)	4.7 µs(1)
T_{HIGH}	SCL high time	$14 \cdot T_{CLCL}$(4)	4.0 µs(1)
T_{RC}	SCL rise time	1 µs	-(2)
T_{FC}	SCL fall time	0.3 µs	0.3 µs(3)
T_{SU}; DAT1	Data set-up time	250 ns	$20 \cdot T_{CLCL}$(4)- T_{RD}
T_{SU}; DAT2	SDA set-up time (before repeated START condition)	250 ns	1 µs(1)
T_{SU}; DAT3	SDA set-up time (before STOP condition)	250 ns	$8 \cdot T_{CLCL}$(4)
T_{HD}; DAT	Data hold time	0 ns	$8 \cdot T_{CLCL}$(4) - T_{FC}
T_{SU}; STA	Repeated START set-up time	$14 \cdot T_{CLCL}$(4)	4.7 µs(1)
T_{SU}; STO	STOP condition set-up time	$14 \cdot T_{CLCL}$(4)	4.0 µs(1)
T_{BUF}	Bus free time	$14 \cdot T_{CLCL}$(4)	4.7 µs(1)
T_{RD}	SDA rise time	1 µs	-(2)
T_{FD}	SDA fall time	0.3 µs	0.3 µs(3)

Notes:
1. At 100 kbit/s. At other bit-rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-up resistor, this must be < 1 µs.
3. Spikes on the SDA and SCL lines with a duration of less than $3 \cdot T_{CLCL}$ will be filtered out. Maximum capacitance on bus-lines SDA and SCL= 400 pF.
4. T_{CLCL}= T_{OSC}= one oscillator clock period.

Waveforms

Figure 9. Two Wire Waveforms

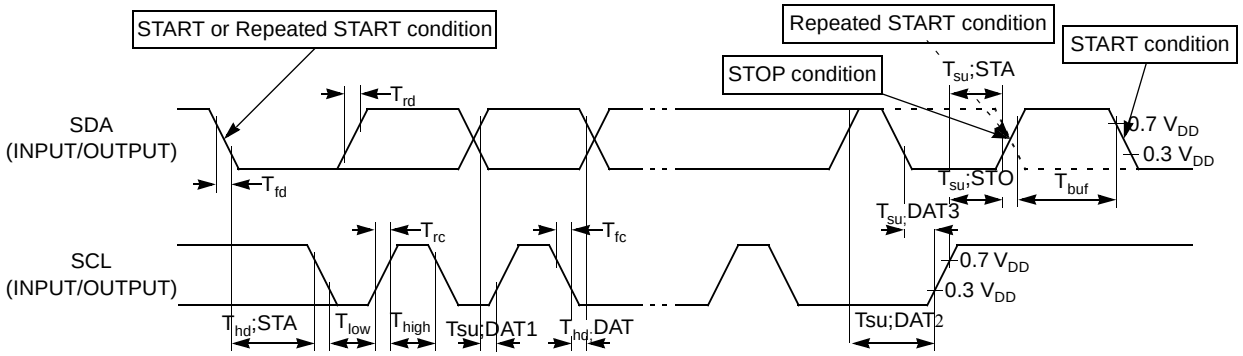
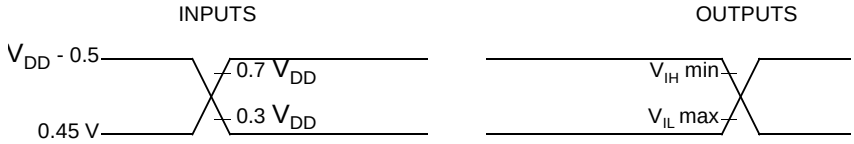
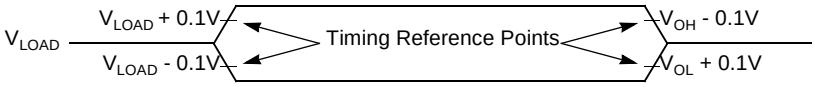


Figure 17. AC Testing Input/Output Waveforms



Notes: 1. During AC testing, all inputs are driven at V_{DD} -0.5V for a logic 1 and 0.45V for a logic 0.
2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Figure 18. Float Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} = \pm 20$ mA.

Ordering Information

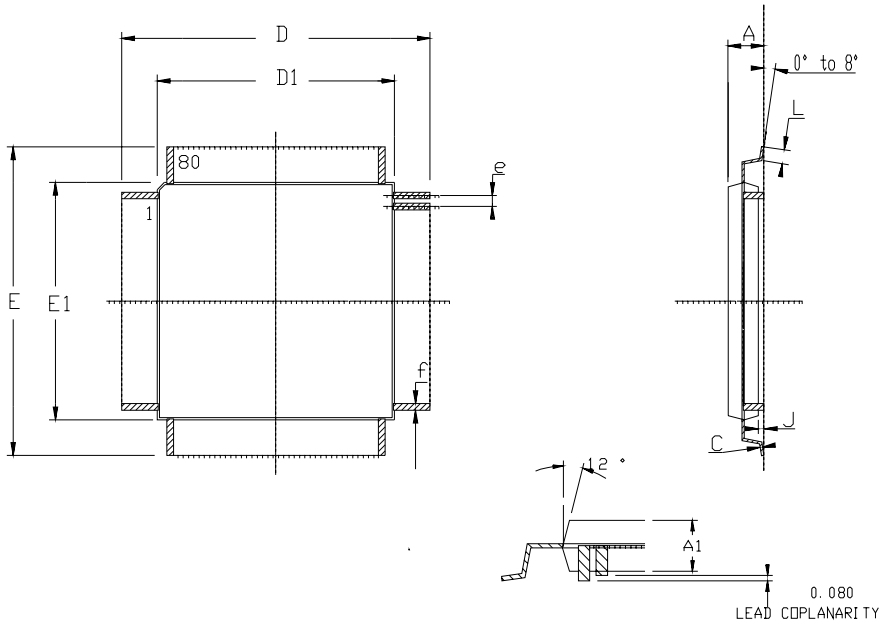
Possible Order Entries[1]

Part Number	Memory Size (Bytes)	Supply Voltage	Temperature Range	Max Frequency (MHz)	Package	Packing	Product Marking
AT89C5132-ROTIL	64K Flash	3V	Industrial	40	TQFP80	Tray	895132-IL

Note: 1. PLCC84 package only available for development board.

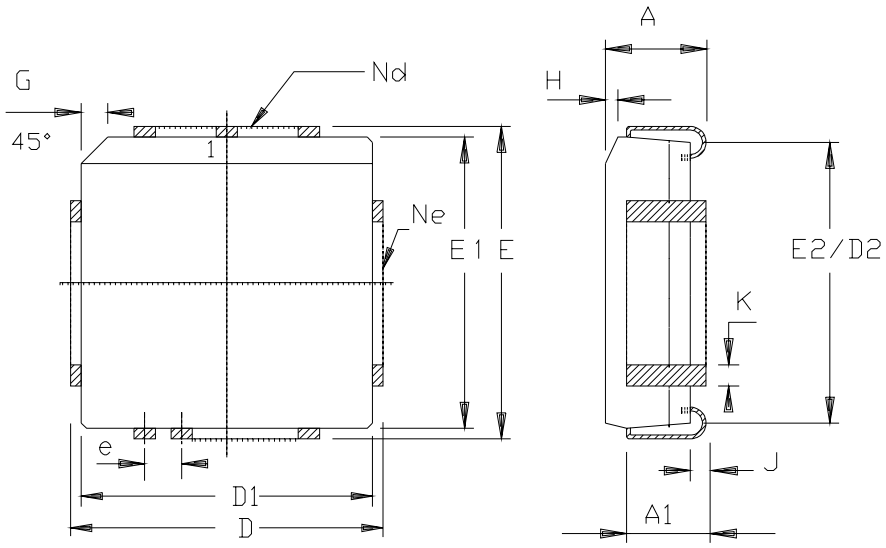
Package Information

TQFP80



	MM		INCH	
	Min	Max	Min	Max
A	1.40	1.60	.055	.063
A1	1.35	1.45	.053	.057
C	0.17 BSC		.007 BSC	
D	15.80	16.20	.622	.638
D1	13.90	14.10	.547	.555
E	15.80	16.20	.622	.638
E1	13.90	14.10	.547	.555
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.65 BSC		.0256 BSC	
f	0.30 BSC		.012 BSC	

PLCC84



	MM		INCH	
A	4.20	5.08	.165	.200
A1	2.29	3.30	.090	.130
D	30.10	30.35	1.185	1.195
D1	29.21	29.41	1.150	1.158
D2	27.69	28.70	1.090	1.130
E	30.10	30.35	1.185	1.195
E1	29.21	29.41	1.150	1.158
E2	27.69	28.70	1.090	1.130
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	21		21	
Ne	21		21	
PKG STD	00			

Datasheet Change Log for AT89C5132

Changes from 4173A-08/02 to 4173B-03/04

1. Supression of ROM product version.
2. Supression of TQFP64 package.

Changes from 4173B-03/04 - 4173C - 07/04

1. Add USB connection schematic in USB section.
2. Add USB termination characteristics in DC Characteristics section.
3. Page access mode clarification in Data Memory section.