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What is "Embedded - Microcontrollers"?

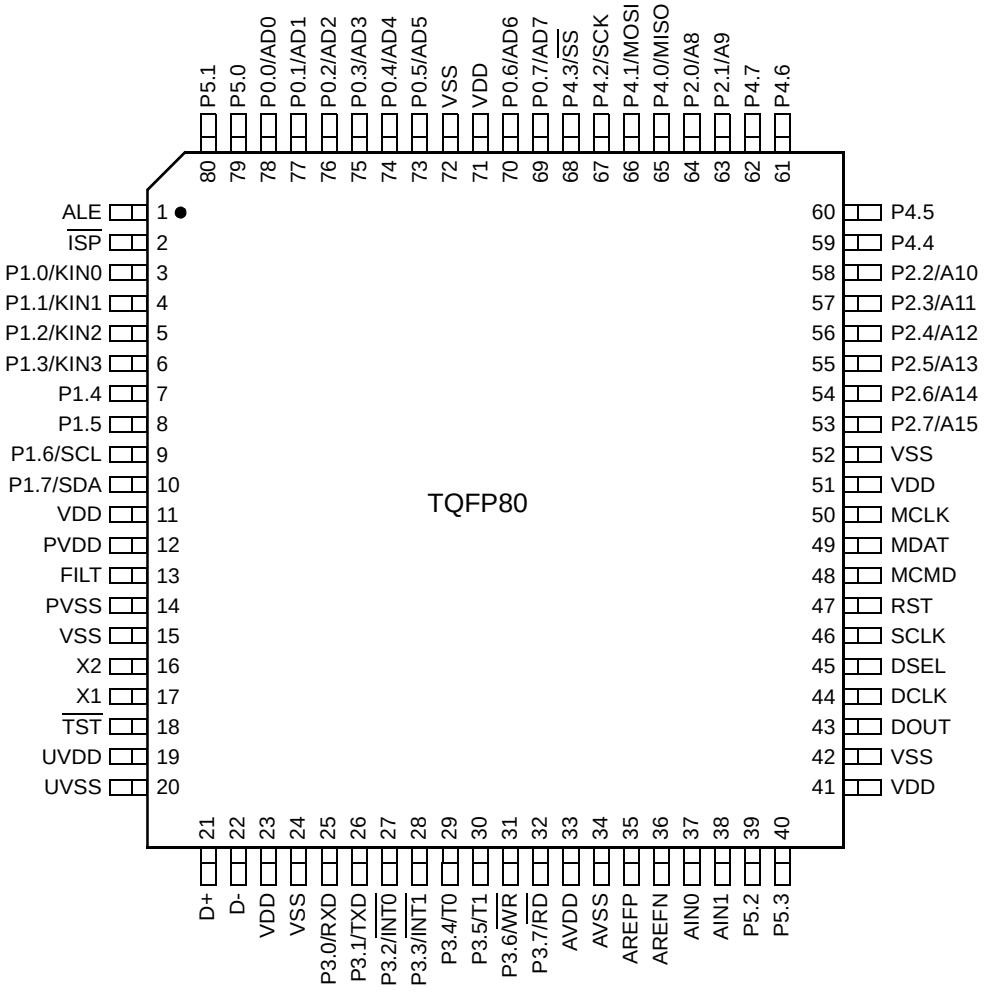
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	20MHz
Connectivity	IDE/ATAPI, I²C, Memory Card, PCM, SPI, UART/USART, USB
Peripherals	I²S, POR, WDT
Number of I/O	44
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5132-rotil

Pin Description

Figure 2. AT89C5132 80-pin TQFP Package



Signals

All the AT89C5132 signals are detailed by functionality in Table 1 to Table 15.

Table 1. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0.7:0	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.7:0	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups.	KIN3:0 SCL SDA
P2.7:0	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8
P3.7:0	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	RXD TXD $\overline{INT0}$ $\overline{INT1}$ T0 T1 $\overline{WR}$ $\overline{RD}$
P4.7:0	I/O	**Port 4** P4 is an 8-bit bidirectional I/O port with internal pull-ups.	MISO MOSI SCK $\overline{SS}$
P5.3:0	I/O	**Port 5** P5 is a 4-bit bidirectional I/O port with internal pull-ups.	-

Table 2. Clock Signal Description

Signal Name	Type	Description	Alternate Function
X1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. X1 is the clock source for internal timing.	-
X2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave X2 unconnected.	-
FILT	I	**PLL Low Pass Filter input** FILT receives the RC network of the PLL low pass filter.	-

Table 11. A/D Converter Signal Description

Signal Name	Type	Description	Alternate Function
AIN1:0	I	**A/D Converter Analog Inputs**	-
AREFP	I	**Analog Positive Voltage Reference Input**	-
AREFN	I	**Analog Negative Voltage Reference Input** This pin is internally connected to AVSS.	-

Table 12. Keypad Interface Signal Description

Signal Name	Type	Description	Alternate Function
KIN3:0	I	**Keypad Input Lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt.	P1.3:0

Table 13. External Access Signal Description

Signal Name	Type	Description	Alternate Function
A15:8	I/O	**Address Lines** Upper address lines for the external bus. Multiplexed higher address and data lines for the IDE interface.	P2.7:0
AD7:0	I/O	**Address/Data Lines** Multiplexed lower address and data lines for the external memory or the IDE interface.	P0.7:0
ALE	O	**Address Latch Enable Output** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A7:0. An external latch is used to demultiplex the address from address/data bus.	-
$\overline{\text{ISP}}$	I/O	**ISP Enable Input** This signal must be held to GND through a pull-down resistor at the falling reset to force execution of the internal bootloader.	-
$\overline{\text{RD}}$	O	**Read Signal** Read signal asserted during external data memory read operation.	P3.7
$\overline{\text{WR}}$	O	**Write Signal** Write signal asserted during external data memory write operation.	P3.6

Table 14. System Signal Description

Signal Name	Type	Description	Alternate Function
RST	I	**Reset Input** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and V_{DD}. Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation.	-
$\overline{TST}$	I	**Test Input** Test mode entry signal. This pin must be set to V_{DD}.	-

Table 15. Power Signal Description

Signal Name	Type	Description	Alternate Function
VDD	PWR	**Digital Supply Voltage** Connect these pins to +3V supply voltage.	-
VSS	GND	**Circuit Ground** Connect these pins to ground.	-
AVDD	PWR	**Analog Supply Voltage** Connect this pin to +3V supply voltage.	-
AVSS	GND	**Analog Ground** Connect this pin to ground.	-
PVDD	PWR	**PLL Supply voltage** Connect this pin to +3V supply voltage.	-
PVSS	GND	**PLL Circuit Ground** Connect this pin to ground.	-
UVDD	PWR	**USB Supply Voltage** Connect this pin to +3V supply voltage.	-
UVSS	GND	**USB Ground** Connect this pin to ground.	-

Address Spaces

The AT8xC5132 derivatives implement four different address spaces:

- Program/Code Memory
- Boot Memory
- Data Memory
- Special Function Registers (SFRs)

Code Memory

The AT89C5132 implements 64K Bytes of on-chip program/code memory in Flash technology.

The Flash memory increases ROM functionality by enabling in-circuit electrical erasure and programming. Thanks to the internal charge pump, the high voltage needed for programming or erasing Flash cells is generated on-chip using the standard V_{DD} voltage. Thus, the AT89C5132 can be programmed using only one voltage and allows in application software programming commonly known as IAP. Hardware programming mode is also available using specific programming tools.

Boot Memory

The AT89C5132 implements 4K Bytes of on-chip boot memory provided in Flash technology. This boot memory is delivered programmed with a standard bootloader software allowing in system programming commonly known as ISP. It also contains some Application Programming Interfaces routines commonly known as API allowing user to develop his own bootloader.

Data Memory

The AT89C5132 derivatives implement 2304 bytes of on-chip data RAM. This memory is divided in two separate areas:

- 256 bytes of on-chip RAM memory (standard C51 memory).
- 2048 bytes of on-chip expanded RAM memory (ERAM accessible via MOVX instructions).

Peripherals

The AT8xC5132 peripherals are briefly described in the following sections. For further details on how to interface (hardware and software) to these peripherals, please refer to the AT8xC5132 complete datasheet.

Clock Generator System

The AT8xC5132 internal clocks are extracted from an on-chip PLL fed by an on-chip oscillator. Four clocks are generated respectively for the C51 core, the audio interface, and the other peripherals. The C51 and peripheral clocks are derived from the oscillator clock. The audio interface sample rates are also obtained by dividing the PLL output clock.

Ports

The AT8xC5132 implement five 8-bit ports (P0 to P4) and one 4-bit port (P5). In addition to performing general-purpose I/Os, some ports are capable of external data memory operations; others allow for alternate functions. All I/O Ports are bidirectional. Each Port contains a latch, an output driver and an input buffer. Port 0 and Port 2 output drivers and input buffers facilitate external memory operations. Some Port 1, Port 3 and Port 4 pins serve for both general-purpose I/Os and alternate functions.

Timers/Counters

The AT8xC5132 implement the two general-purpose, 16-bit Timers/Counters of a standard C51. They are identified as Timer 0, Timer 1, and can independently be configured each to operate in a variety of modes as a Timer or as an event Counter. When operating as a Timer, a Timer/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

Watchdog Timer

The AT8xC5132 implement a hardware Watchdog Timer that automatically resets the chip if it is allowed to time out. The WDT provides a means of recovering from routines that do not complete successfully due to software or hardware malfunctions.

Audio Output Interface

The AT8xC5132 implements an audio output interface allowing the decoded audio bitstream to be output in various formats. They are compatible with right and left justification PCM and I^2S formats and the on-chip PLL allows connection of almost all commercial audio DAC families available on the market.

Universal Serial Bus Interface

The AT8xC5132 implements a full-speed Universal Serial Bus Interface. The USB interface can be used for the following purposes:

- Download of files by supporting the USB mass storage class.
- In-System Programming by supporting the USB firmware upgrade class.

MultiMedia Card Interface

The AT8xC5132 implements a MultiMedia Card (MMC) interface compliant to the V2.2 specification in MultiMedia Card mode. The MMC allows storage of files in removable Flash memory cards that can be easily plugged or removed from the application. It can also be used for In-System Programming.

IDE/ATAPI Interface

The AT8xC5132 provide an IDE/ATAPI interface allowing connection of devices such as CD-ROM reader, CompactFlash™ cards, Hard Disk Drive, etc. It consists of a 16-bit bidirectional bus part of the low-level ANSI ATA/ATAPI specification. It is provided for mass storage interface but could be used for In-System Programming using CD-ROM.

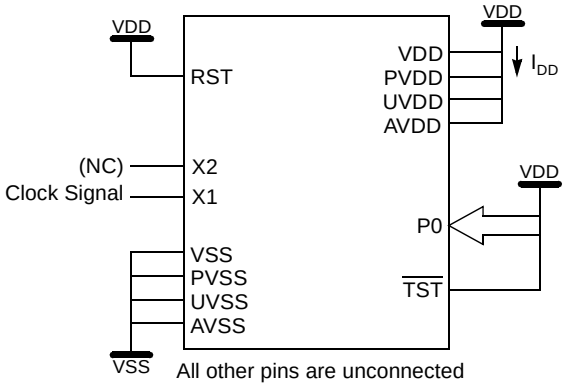
Table 1. Digital DC Characteristics
V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
I_{LI}	Input Leakage Current (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			10	µA	0.45< V_{IN}< V_{DD}
I_{TL}	Logical 1 to 0 Transition Current (P1, P2, P3, P4 and P5)			-650	µA	Vin = 2.0 V
R_{RST}	Pull-Down Resistor	50	90	200	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A= 25°C
V_{RET}	V_{DD} Data Retention Limit			1.8	V	
I_{DD}	Operating Current		(3)	X1 / X2 mode 6.5 / 10.5 8 / 13.5 9.5 / 17	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
I_{DL}	Idle Mode Current		(3)	X1 / X2 mode 5.3 / 8.1 6.4 / 10.3 7.5 / 13	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
I_{PD}	Power-Down Mode Current		20	500	µA	V_{RET} < V_{DD} < 3.3 V

Notes:
1. Typical values are obtained using V_{DD}= 3 V and T_A= 25°C. They are not tested and there is no guarantee on these values.
2. Flash retention is guaranteed with the same formula for V_{DD} min down to 0V.
3. See Table 154 for typical consumption in player mode.

I_{DD}, I_{DL} and I_{PD} Test Conditions

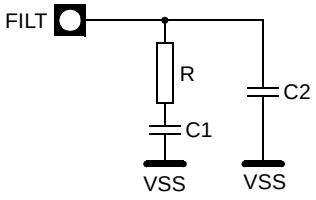
Figure 1. I_{DD} Test Condition, Active Mode



Phase Lock Loop

Schematic

Figure 5. PLL Filter Connection



Parameters

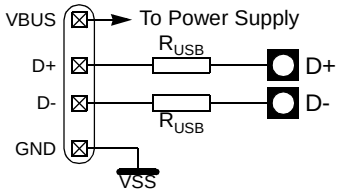
Table 4. PLL Filter Characteristics
V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R	Filter Resistor		100		Ω
C1	Filter Capacitance 1		10		nF
C2	Filter Capacitance 2		2.2		nF

USB Connection

Schematic

Figure 6. USB Connection



Parameters

Table 1. USB Termination Characteristics

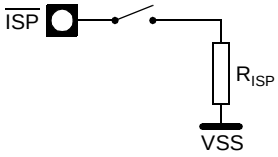
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R_{USB}	USB Termination Resistor		27		Ω

In-system Programming

Schematic

Figure 7. ISP Pull-down Connection



Parameters

Table 5. ISP Pull-Down Characteristics
V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R_{ISP}	ISP Pull-Down Resistor		2.2		kΩ

AC Characteristics

External 8-bit Bus Cycles

Definition of Symbols

Table 1. External 8-bit Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	$\overline{RD}$
W	$\overline{WR}$

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

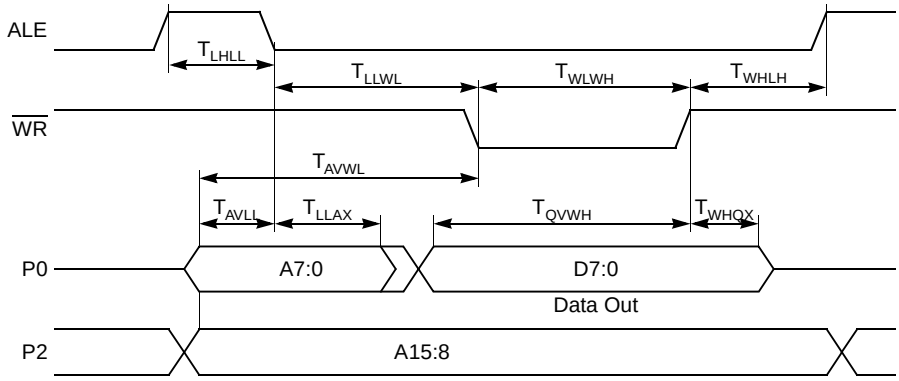
Timings

Test conditions: capacitive load on all pins = 50 pF.

Table 2. External 8-bit Bus Cycle – Data Read AC Timings
V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}-15$		$T_{CLCL}-15$		ns
T_{AVLL}	Address Valid to ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLAX}	Address hold after ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLRL}	ALE Low to $\overline{RD}$ Low	$3 \cdot T_{CLCL}-30$		$1.5 \cdot T_{CLCL}-30$		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	$6 \cdot T_{CLCL}-25$		$3 \cdot T_{CLCL}-25$		ns
T_{RHLH}	$\overline{RD}$ high to ALE High	$T_{CLCL}-20$	$T_{CLCL}+20$	$0.5 \cdot T_{CLCL}-20$	$0.5 \cdot T_{CLCL}+20$	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}-65$		$4.5 \cdot T_{CLCL}-65$	ns
T_{AVRL}	Address Valid to $\overline{RD}$ Low	$4 \cdot T_{CLCL}-30$		$2 \cdot T_{CLCL}-30$		ns
T_{RLDV}	$\overline{RD}$ Low to Valid Data		$5 \cdot T_{CLCL}-30$		$2.5 \cdot T_{CLCL}-30$	ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
T_{RHDX}	Data Hold After $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Instruction Float After $\overline{RD}$ High		$2 \cdot T_{CLCL}-25$		$T_{CLCL}-25$	ns

Figure 2. External 8-bit Bus Cycle – Data Write Waveforms



External IDE 16-bit Bus Cycles

Definition of Symbols

Table 4. External IDE 16-bit Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	$\overline{RD}$
W	$\overline{WR}$

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

Test conditions: capacitive load on all pins = 50 pF.

Table 5. External IDE 16-bit Bus Cycle – Data Read AC Timings
V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

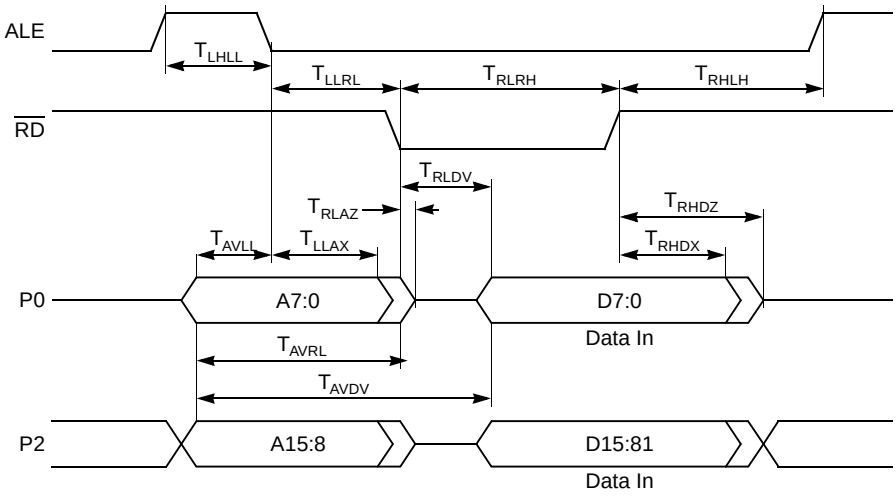
Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLRL}	ALE Low to $\overline{RD}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{RHLH}	$\overline{RD}$ high to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}$-65		$4.5 \cdot T_{CLCL}$-65	ns
T_{AVRL}	Address Valid to $\overline{RD}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{RLDV}	$\overline{RD}$ Low to Valid Data		$5 \cdot T_{CLCL}$-30		$2.5 \cdot T_{CLCL}$-30	ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
T_{RHDX}	Data Hold After $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Instruction Float After $\overline{RD}$ High		$2 \cdot T_{CLCL}$-25		T_{CLCL}-25	ns

Table 6. External IDE 16-bit Bus Cycle – Data Write AC Timings
V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLWL}	ALE Low to $\overline{WR}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{WHLH}	$\overline{WR}$ High to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	$7 \cdot T_{CLCL}$-20		$3.5 \cdot T_{CLCL}$-20		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{CLCL}-15		$0.5 \cdot T_{CLCL}$-15		ns

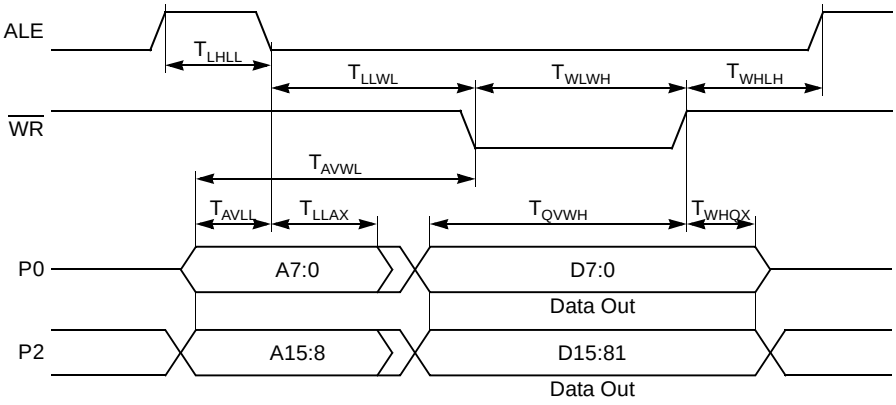
Waveforms

Figure 3. External IDE 16-bit Bus Cycle – Data Read Waveforms



Note: D15:8 is written in DAT16H SFR.

Figure 4. External IDE 16-bit Bus Cycle – Data Write Waveforms



Note: D15:8 is the content of DAT16H SFR.

SPI Interface

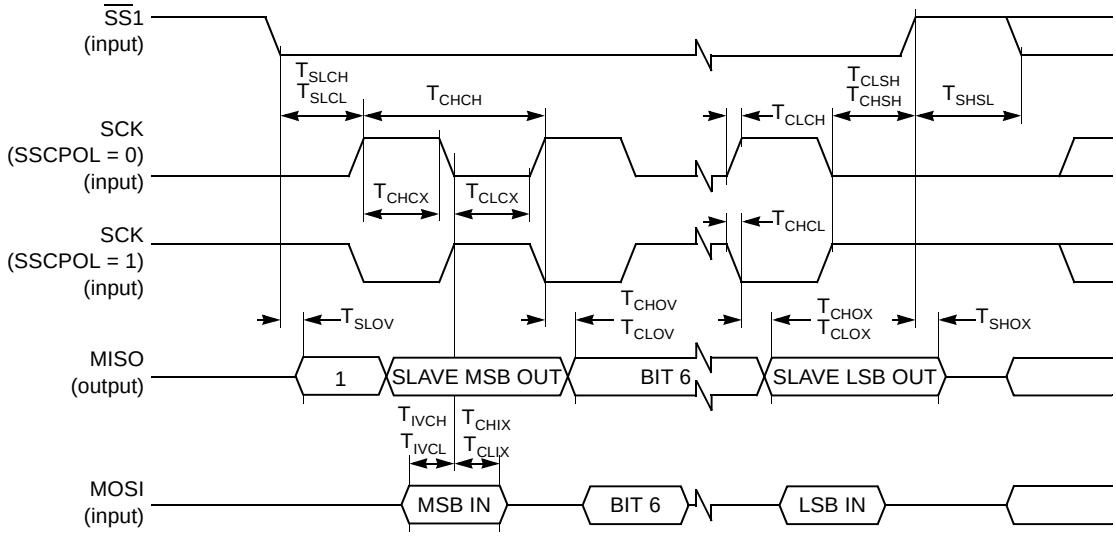
Definition of Symbols

Table 7. SPI Interface Timing Symbol Definitions

Signals	
C	Clock
I	Data In
O	Data Out

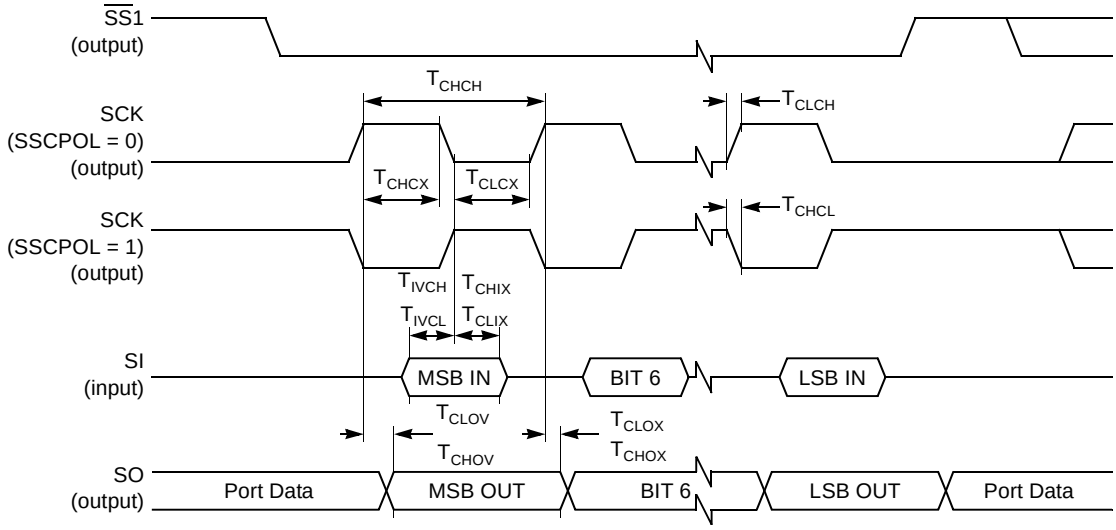
Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Figure 7. SPI Master Waveforms (SSCPHA = 0)



Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

Figure 8. SPI Master Waveforms (SSCPHA = 1)



Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

Two-wire Interface

Timings

Table 1. TWI Interface AC Timing

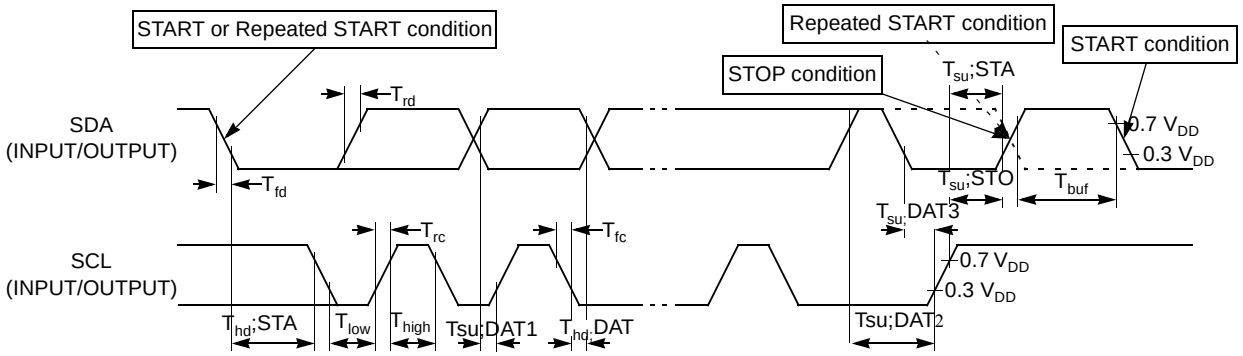
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	INPUT Min Max	OUTPUT Min Max
T_{HD}; STA	Start condition hold time	$14 \cdot T_{CLCL}$(4)	4.0 µs(1)
T_{LOW}	SCL low time	$16 \cdot T_{CLCL}$(4)	4.7 µs(1)
T_{HIGH}	SCL high time	$14 \cdot T_{CLCL}$(4)	4.0 µs(1)
T_{RC}	SCL rise time	1 µs	-(2)
T_{FC}	SCL fall time	0.3 µs	0.3 µs(3)
T_{SU}; DAT1	Data set-up time	250 ns	$20 \cdot T_{CLCL}$(4)- T_{RD}
T_{SU}; DAT2	SDA set-up time (before repeated START condition)	250 ns	1 µs(1)
T_{SU}; DAT3	SDA set-up time (before STOP condition)	250 ns	$8 \cdot T_{CLCL}$(4)
T_{HD}; DAT	Data hold time	0 ns	$8 \cdot T_{CLCL}$(4) - T_{FC}
T_{SU}; STA	Repeated START set-up time	$14 \cdot T_{CLCL}$(4)	4.7 µs(1)
T_{SU}; STO	STOP condition set-up time	$14 \cdot T_{CLCL}$(4)	4.0 µs(1)
T_{BUF}	Bus free time	$14 \cdot T_{CLCL}$(4)	4.7 µs(1)
T_{RD}	SDA rise time	1 µs	-(2)
T_{FD}	SDA fall time	0.3 µs	0.3 µs(3)

Notes:
1. At 100 kbit/s. At other bit-rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-up resistor, this must be < 1 µs.
3. Spikes on the SDA and SCL lines with a duration of less than $3 \cdot T_{CLCL}$ will be filtered out. Maximum capacitance on bus-lines SDA and SCL= 400 pF.
4. T_{CLCL}= T_{OSC}= one oscillator clock period.

Waveforms

Figure 9. Two Wire Waveforms



MMC Interface

Definition of Symbols

Table 9. MMC Interface Timing Symbol Definitions

Signals	
C	Clock
D	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

Timings

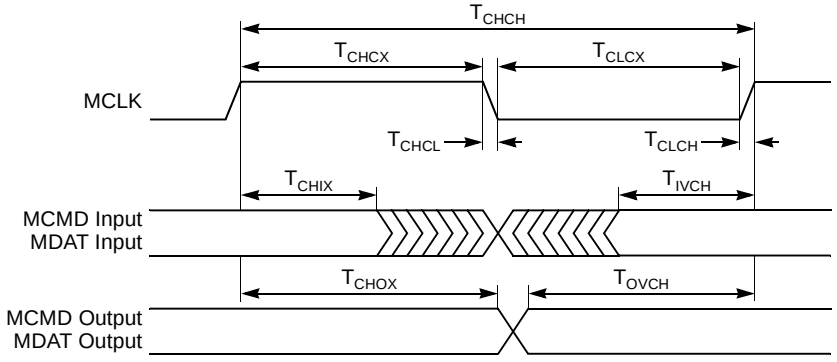
Table 10. MMC Interface AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C, CL ≤ 100pF (10 cards)

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period	50		ns
T_{CHCX}	Clock High Time	10		ns
T_{CLCX}	Clock Low Time	10		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{DVCH}	Input Data Valid to Clock High	3		ns
T_{CHDX}	Input Data Hold after Clock High	3		ns
T_{CHOX}	Output Data Hold after Clock High	5		ns
T_{OVCH}	Output Data Valid to Clock High	5		ns

Waveforms

Figure 10. MMC Input Output Waveforms



Audio Interface

Definition of Symbols

Table 11. Audio Interface Timing Symbol Definitions

Signals	
C	Clock
O	Data Out
S	Data Select

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

Timings

Table 12. Audio Interface AC timings

V_{DD} = 2.7 to 3.3V, T_A = -40 to +85°C, CL ≤ 30pF

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period		325.5(1)	ns
T_{CHCX}	Clock High Time	30		ns
T_{CLCX}	Clock Low Time	30		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{CLSV}	Clock Low to Select Valid		10	ns
T_{CLOV}	Clock Low to Data Valid		10	ns

Note: 32-bit format with Fs = 48 kHz.

Waveforms

Figure 11. Audio Interface Waveforms

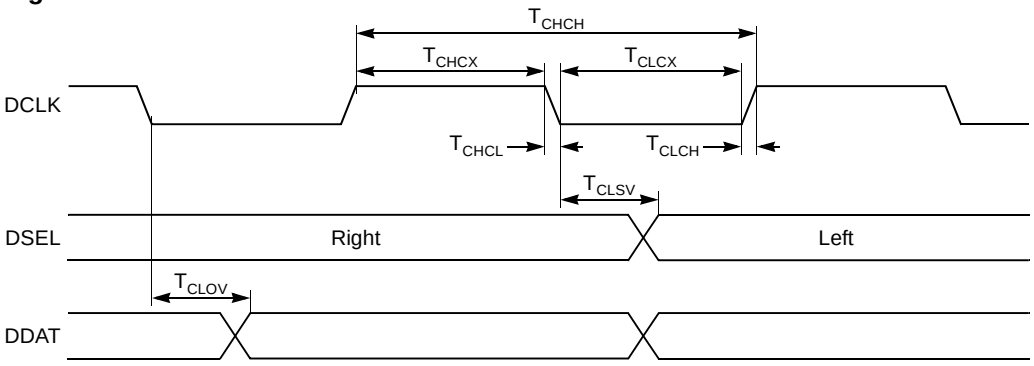
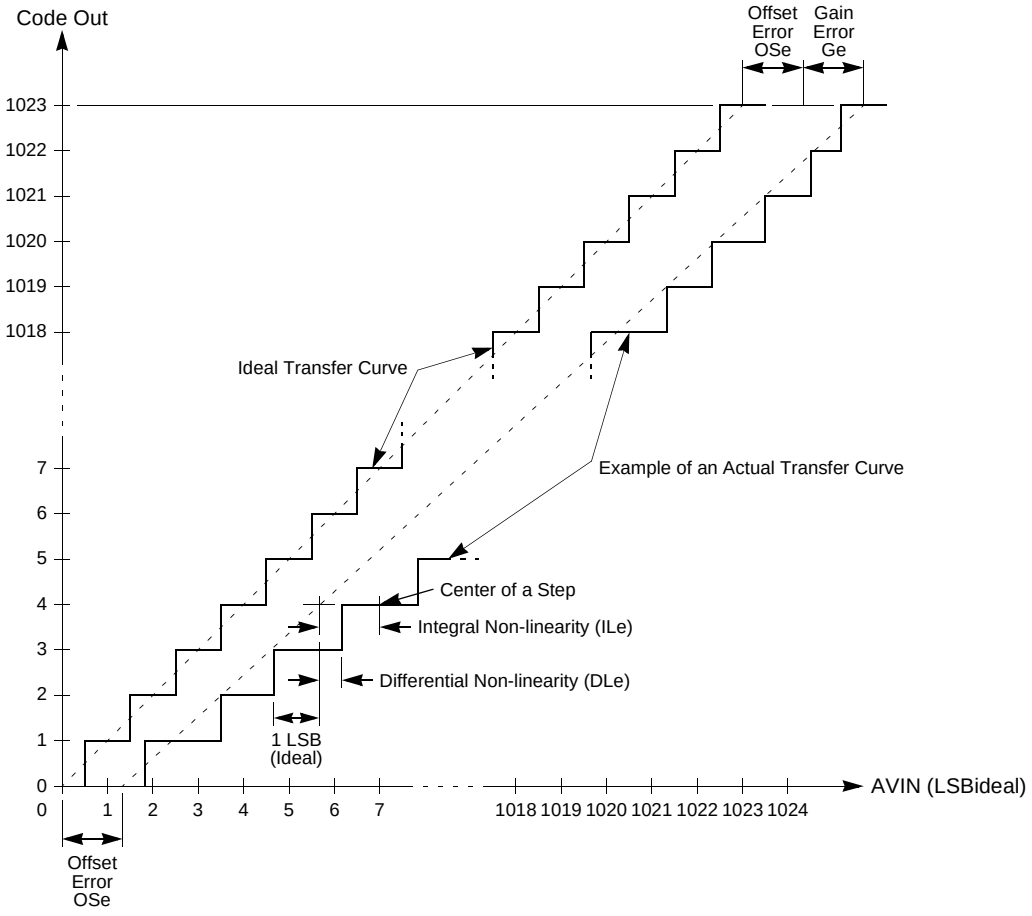


Figure 13. Analog-to-Digital Converter Characteristics



Flash Memory

Definition of Symbols

Table 14. Flash Memory Timing Symbol Definitions

Signals	
S	$\overline{ISP}$
R	RST
B	FBUSY flag

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

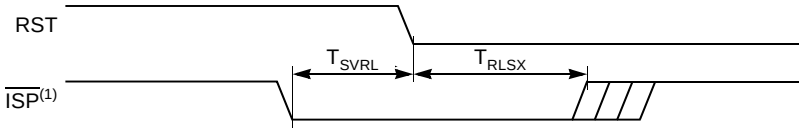
Table 15. Flash Memory AC Timing

V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
T_{SVRL}	Input $\overline{ISP}$ Valid to RST Edge	50			ns
T_{RLSX}	Input $\overline{ISP}$ Hold after RST Edge	50			ns
T_{BHBL}	FLASH Internal Busy (Programming) Time		10		ms
N_{FCY}	Number of Flash Write Cycles	100K			Cycle
T_{FDR}	Flash Data Retention Time	10			Year

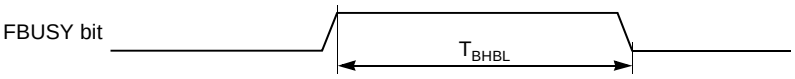
Waveforms

Figure 14. Flash Memory – ISP Waveforms



Note: 1. $\overline{ISP}$ must be driven through a pull-down resistor (see Section “In-system Programming”, page 22).

Figure 15. Flash Memory – Internal Busy Waveforms



External Clock Drive and Logic Level References

Definition of Symbols

Table 16. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

Timings

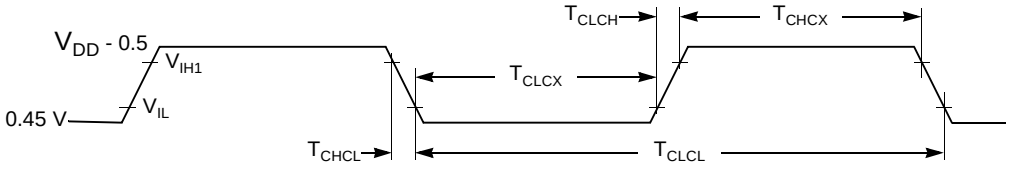
Table 17. External Clock AC Timings

V_{DD} = 2.7 to 3.3V, T_A= -40 to +85°C

Symbol	Parameter	Min	Max	Unit
T_{CLCL}	Clock Period	50		ns
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns
T_{CR}	Cyclic Ratio in X2 Mode	40	60	%

Waveforms

Figure 16. External Clock Waveform



Datasheet Change Log for AT89C5132

Changes from 4173A-08/02 to 4173B-03/04

1. Supression of ROM product version.
2. Supression of TQFP64 package.

Changes from 4173B-03/04 - 4173C - 07/04

1. Add USB connection schematic in USB section.
2. Add USB termination characteristics in DC Characteristics section.
3. Page access mode clarification in Data Memory section.

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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