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What is "Embedded - Microcontrollers"?

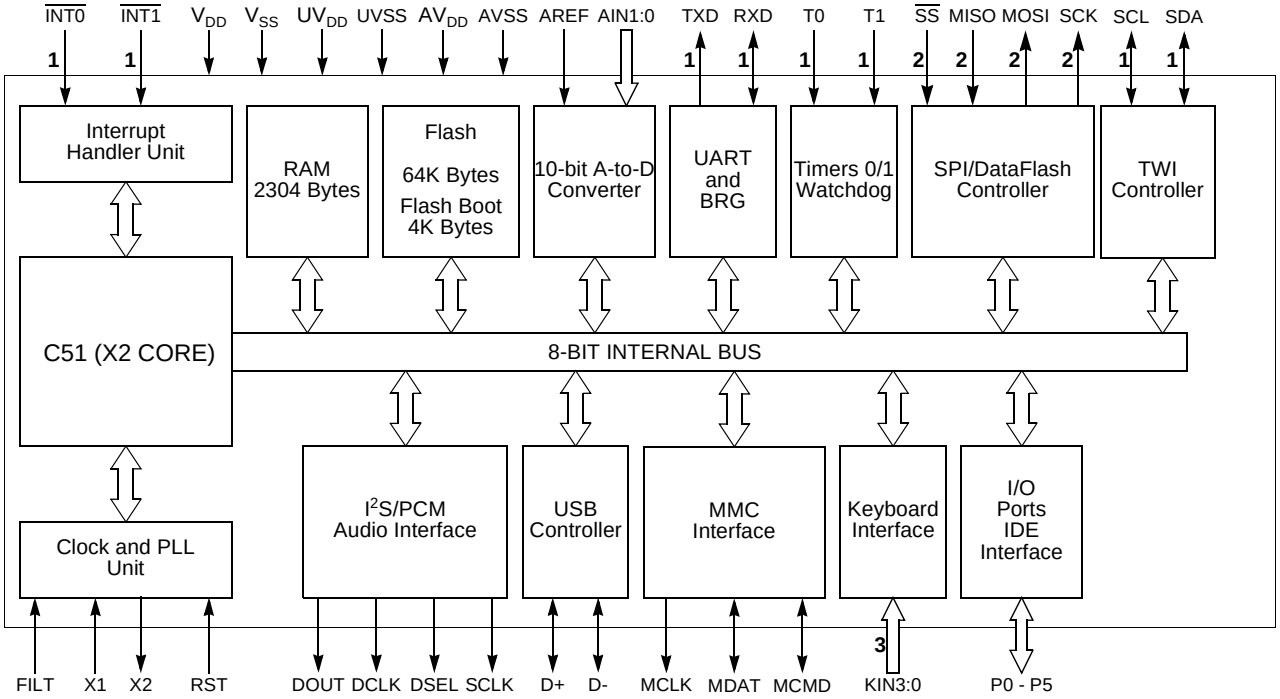
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	20MHz
Connectivity	IDE/ATAPI, I²C, Memory Card, PCM, SPI, UART/USART, USB
Peripherals	I²S, POR, WDT
Number of I/O	44
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5132-rotul

Block Diagram

Figure 1. AT89C5132 Block Diagram



Notes: 1. Alternate function of Port 3
2. Alternate function of Port 4
3. Alternate function of Port 1

Signals

All the AT89C5132 signals are detailed by functionality in Table 1 to Table 15.

Table 1. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0.7:0	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.7:0	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups.	KIN3:0 SCL SDA
P2.7:0	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8
P3.7:0	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	RXD TXD $\overline{INT0}$ $\overline{INT1}$ T0 T1 $\overline{WR}$ $\overline{RD}$
P4.7:0	I/O	**Port 4** P4 is an 8-bit bidirectional I/O port with internal pull-ups.	MISO MOSI SCK $\overline{SS}$
P5.3:0	I/O	**Port 5** P5 is a 4-bit bidirectional I/O port with internal pull-ups.	-

Table 2. Clock Signal Description

Signal Name	Type	Description	Alternate Function
X1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. X1 is the clock source for internal timing.	-
X2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave X2 unconnected.	-
FILT	I	**PLL Low Pass Filter input** FILT receives the RC network of the PLL low pass filter.	-

Table 11. A/D Converter Signal Description

Signal Name	Type	Description	Alternate Function
AIN1:0	I	**A/D Converter Analog Inputs**	-
AREFP	I	**Analog Positive Voltage Reference Input**	-
AREFN	I	**Analog Negative Voltage Reference Input** This pin is internally connected to AVSS.	-

Table 12. Keypad Interface Signal Description

Signal Name	Type	Description	Alternate Function
KIN3:0	I	**Keypad Input Lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt.	P1.3:0

Table 13. External Access Signal Description

Signal Name	Type	Description	Alternate Function
A15:8	I/O	**Address Lines** Upper address lines for the external bus. Multiplexed higher address and data lines for the IDE interface.	P2.7:0
AD7:0	I/O	**Address/Data Lines** Multiplexed lower address and data lines for the external memory or the IDE interface.	P0.7:0
ALE	O	**Address Latch Enable Output** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A7:0. An external latch is used to demultiplex the address from address/data bus.	-
$\overline{\text{ISP}}$	I/O	**ISP Enable Input** This signal must be held to GND through a pull-down resistor at the falling reset to force execution of the internal bootloader.	-
$\overline{\text{RD}}$	O	**Read Signal** Read signal asserted during external data memory read operation.	P3.7
$\overline{\text{WR}}$	O	**Write Signal** Write signal asserted during external data memory write operation.	P3.6

Table 14. System Signal Description

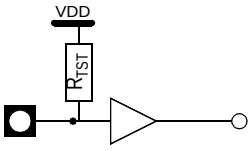
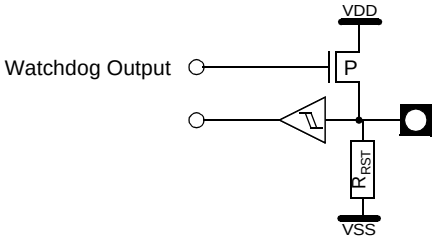
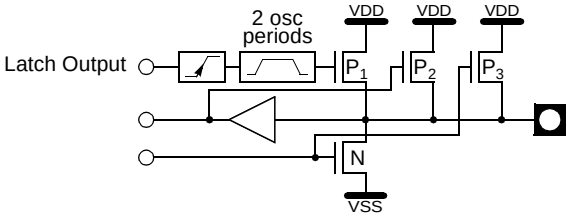
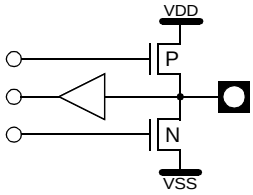
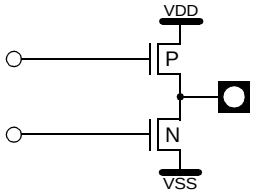
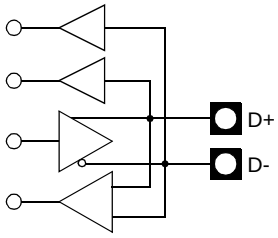
Signal Name	Type	Description	Alternate Function
RST	I	**Reset Input** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and V_{DD}. Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation.	-
$\overline{TST}$	I	**Test Input** Test mode entry signal. This pin must be set to V_{DD}.	-

Table 15. Power Signal Description

Signal Name	Type	Description	Alternate Function
VDD	PWR	**Digital Supply Voltage** Connect these pins to +3V supply voltage.	-
VSS	GND	**Circuit Ground** Connect these pins to ground.	-
AVDD	PWR	**Analog Supply Voltage** Connect this pin to +3V supply voltage.	-
AVSS	GND	**Analog Ground** Connect this pin to ground.	-
PVDD	PWR	**PLL Supply voltage** Connect this pin to +3V supply voltage.	-
PVSS	GND	**PLL Circuit Ground** Connect this pin to ground.	-
UVDD	PWR	**USB Supply Voltage** Connect this pin to +3V supply voltage.	-
UVSS	GND	**USB Ground** Connect this pin to ground.	-

Internal Pin Structure

Table 16. Detailed Internal Pin Structure

Circuit[1]	Type	Pins
	Input	$\overline{TST}$
	Input/Output	RST
	Input/Output	P1[2] P2[3] P3 P4 P53:0
	Input/Output	P0 MCMD MDAT $\overline{ISP}$ $\overline{PSEN}$
	Output	ALE SCLK DCLK DOUT DSEL MCLK
	Input/Output	D+ D-

Notes:
1. For information on resistors value, input/output levels, and drive capability, refer to the Section “DC Characteristics”, page 183.
2. When the Two Wire controller is enabled, P_1, P_2, and P_3 transistors are disabled allowing pseudo open-drain structure.
3. In Port 2, P_1 transistor is continuously driven when outputting a high level bit address (A15:8).

Peripherals

The AT8xC5132 peripherals are briefly described in the following sections. For further details on how to interface (hardware and software) to these peripherals, please refer to the AT8xC5132 complete datasheet.

Clock Generator System

The AT8xC5132 internal clocks are extracted from an on-chip PLL fed by an on-chip oscillator. Four clocks are generated respectively for the C51 core, the audio interface, and the other peripherals. The C51 and peripheral clocks are derived from the oscillator clock. The audio interface sample rates are also obtained by dividing the PLL output clock.

Ports

The AT8xC5132 implement five 8-bit ports (P0 to P4) and one 4-bit port (P5). In addition to performing general-purpose I/Os, some ports are capable of external data memory operations; others allow for alternate functions. All I/O Ports are bidirectional. Each Port contains a latch, an output driver and an input buffer. Port 0 and Port 2 output drivers and input buffers facilitate external memory operations. Some Port 1, Port 3 and Port 4 pins serve for both general-purpose I/Os and alternate functions.

Timers/Counters

The AT8xC5132 implement the two general-purpose, 16-bit Timers/Counters of a standard C51. They are identified as Timer 0, Timer 1, and can independently be configured each to operate in a variety of modes as a Timer or as an event Counter. When operating as a Timer, a Timer/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

Watchdog Timer

The AT8xC5132 implement a hardware Watchdog Timer that automatically resets the chip if it is allowed to time out. The WDT provides a means of recovering from routines that do not complete successfully due to software or hardware malfunctions.

Audio Output Interface

The AT8xC5132 implements an audio output interface allowing the decoded audio bitstream to be output in various formats. They are compatible with right and left justification PCM and I^2S formats and the on-chip PLL allows connection of almost all commercial audio DAC families available on the market.

Universal Serial Bus Interface

The AT8xC5132 implements a full-speed Universal Serial Bus Interface. The USB interface can be used for the following purposes:

- Download of files by supporting the USB mass storage class.
- In-System Programming by supporting the USB firmware upgrade class.

MultiMedia Card Interface

The AT8xC5132 implements a MultiMedia Card (MMC) interface compliant to the V2.2 specification in MultiMedia Card mode. The MMC allows storage of files in removable Flash memory cards that can be easily plugged or removed from the application. It can also be used for In-System Programming.

IDE/ATAPI Interface

The AT8xC5132 provide an IDE/ATAPI interface allowing connection of devices such as CD-ROM reader, CompactFlash™ cards, Hard Disk Drive, etc. It consists of a 16-bit bidirectional bus part of the low-level ANSI ATA/ATAPI specification. It is provided for mass storage interface but could be used for In-System Programming using CD-ROM.

Electrical Characteristics

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Voltage on any other Pin to V_{SS}	-0.3 to +4.0V
I_{OL} per I/O Pin	5 mA
Power Dissipation	1 W
Ambient Temperature Under Bias	-40°C to +85°C
V_{DD}	2.7V to 3.3V

NOTE: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

DC Characteristics

Digital Logic

Table 1. Digital DC Characteristics

V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ[1]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IH1}	Input High Voltage (except RST, X1)	$0.2 \cdot V_{DD}$ + 1.1		V_{DD}	V	
V_{IH2}	Input High Voltage (RST, X1)	$0.7 \cdot V_{DD}$[2]		V_{DD} + 0.5	V	
V_{OL1}	Output Low Voltage (except P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			0.45	V	I_{OL}= 1.6 mA
V_{OL2}	Output Low Voltage (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			0.45	V	I_{OL}= 3.2 mA
V_{OH1}	Output High Voltage (P1, P2, P3, P4 and P5)	V_{DD} - 0.7			V	I_{OH}= -30 µA
V_{OH2}	Output High Voltage (P0, P2 address mode, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT, D+, D-)	V_{DD} - 0.7			V	I_{OH}= -3.2 mA
I_{IL}	Logical 0 Input Current (P1, P2, P3, P4 and P5)			-50	µA	Vin = 0.45 V

Table 1. Digital DC Characteristics
V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
I_{LI}	Input Leakage Current (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			10	µA	0.45< V_{IN}< V_{DD}
I_{TL}	Logical 1 to 0 Transition Current (P1, P2, P3, P4 and P5)			-650	µA	Vin = 2.0 V
R_{RST}	Pull-Down Resistor	50	90	200	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A= 25°C
V_{RET}	V_{DD} Data Retention Limit			1.8	V	
I_{DD}	Operating Current		(3)	X1 / X2 mode 6.5 / 10.5 8 / 13.5 9.5 / 17	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
I_{DL}	Idle Mode Current		(3)	X1 / X2 mode 5.3 / 8.1 6.4 / 10.3 7.5 / 13	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
I_{PD}	Power-Down Mode Current		20	500	µA	V_{RET} < V_{DD} < 3.3 V

Notes:
1. Typical values are obtained using V_{DD}= 3 V and T_A= 25°C. They are not tested and there is no guarantee on these values.
2. Flash retention is guaranteed with the same formula for V_{DD} min down to 0V.
3. See Table 154 for typical consumption in player mode.

I_{DD}, I_{DL} and I_{PD} Test Conditions

Figure 1. I_{DD} Test Condition, Active Mode

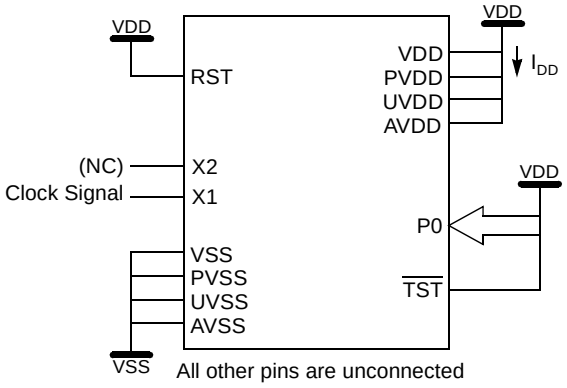


Figure 2. I_{DL} Test Condition, Idle Mode

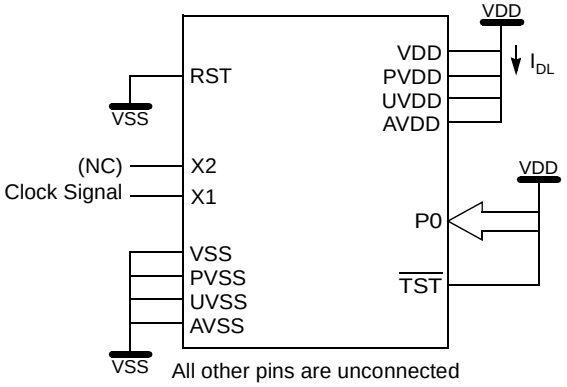
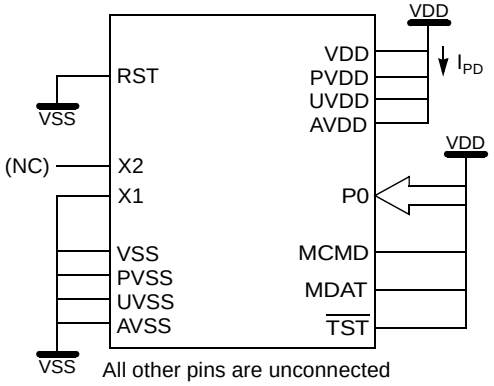


Figure 3. I_{PD} Test Condition, Power-Down Mode



A-to-D Converter

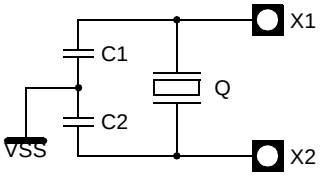
Table 2. A-to-D Converter DC Characteristics
V_{DD} = 2.7 to 3.3V , T_A = -40°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
AV_{DD}	Analog Supply Voltage	2.7		3.3	V	
AI_{DD}	Analog Operating Supply Current			600	µA	AV_{DD} = 3.3V AIN1:0 = 0 to AV_{DD}
AI_{PD}	Analog Standby Current			2	µA	AV_{DD} = 3.3V ADEN = 0 or PD = 1
AV_{IN}	Analog Input Voltage	AV_{SS}		AV_{DD}	V	
AV_{REF}	Reference Voltage A_{REFN} A_{REFP}	 AV_{SS} 2.4		 AV_{DD}	 V V	
R_{REF}	AREF Input Resistance	10		30	kΩ	T_A = 25°C
C_{IA}	Analog Input capacitance			10	pF	T_A = 25°C

Oscillator and Crystal

Schematic

Figure 4. Crystal Connection



Note: For operation with most standard crystals, no external components are needed on X1 and X2. It may be necessary to add external capacitors on X1 and X2 to ground in special cases (max 10 pF). X1 and X2 may not be used to drive other circuits.

Parameters

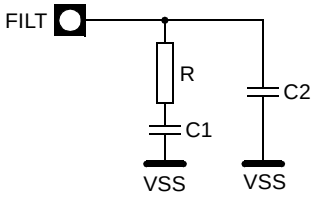
Table 3. Oscillator and Crystal Characteristics
V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
C_{X1}	Internal Capacitance (X1 - V_{SS})		10		pF
C_{X2}	Internal Capacitance (X2 - V_{SS})		10		pF
C_L	Equivalent Load Capacitance (X1 - X2)		5		pF
DL	Drive Level			50	µW
F	Crystal Frequency			20	MHz
RS	Crystal Series Resistance			40	Ω
CS	Crystal Shunt Capacitance			6	pF

Phase Lock Loop

Schematic

Figure 5. PLL Filter Connection



Parameters

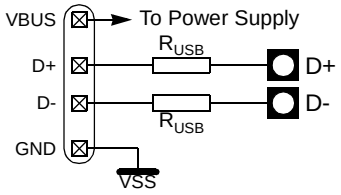
Table 4. PLL Filter Characteristics
V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R	Filter Resistor		100		Ω
C1	Filter Capacitance 1		10		nF
C2	Filter Capacitance 2		2.2		nF

USB Connection

Schematic

Figure 6. USB Connection



Parameters

Table 1. USB Termination Characteristics

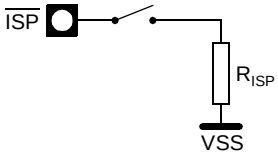
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R_{USB}	USB Termination Resistor		27		Ω

In-system Programming

Schematic

Figure 7. ISP Pull-down Connection



Parameters

Table 5. ISP Pull-Down Characteristics
V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

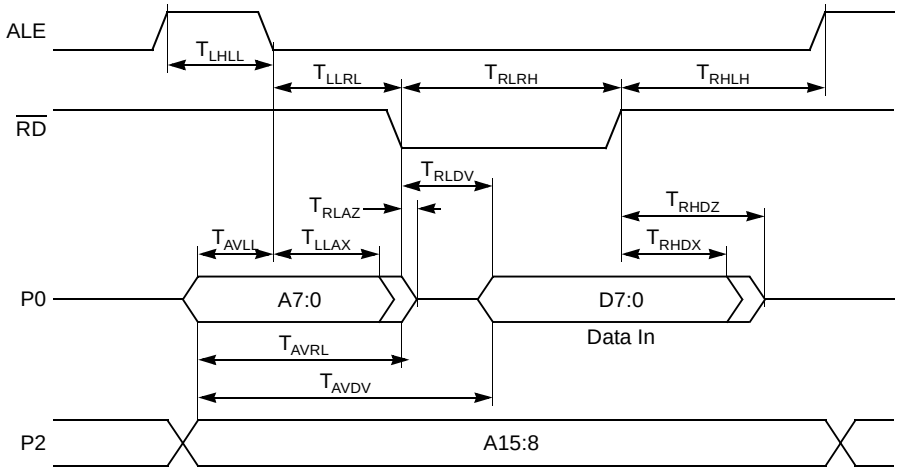
Symbol	Parameter	Min	Typ	Max	Unit
R_{ISP}	ISP Pull-Down Resistor		2.2		kΩ

Table 3. External 8-bit Bus Cycle – Data Write AC Timings
V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLWL}	ALE Low to $\overline{WR}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{WHLH}	$\overline{WR}$ High to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	$7 \cdot T_{CLCL}$-20		$3.5 \cdot T_{CLCL}$-20		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{CLCL}-15		$0.5 \cdot T_{CLCL}$-15		ns

Waveforms

Figure 1. External 8-bit Bus Cycle – Data Read Waveforms



Timings

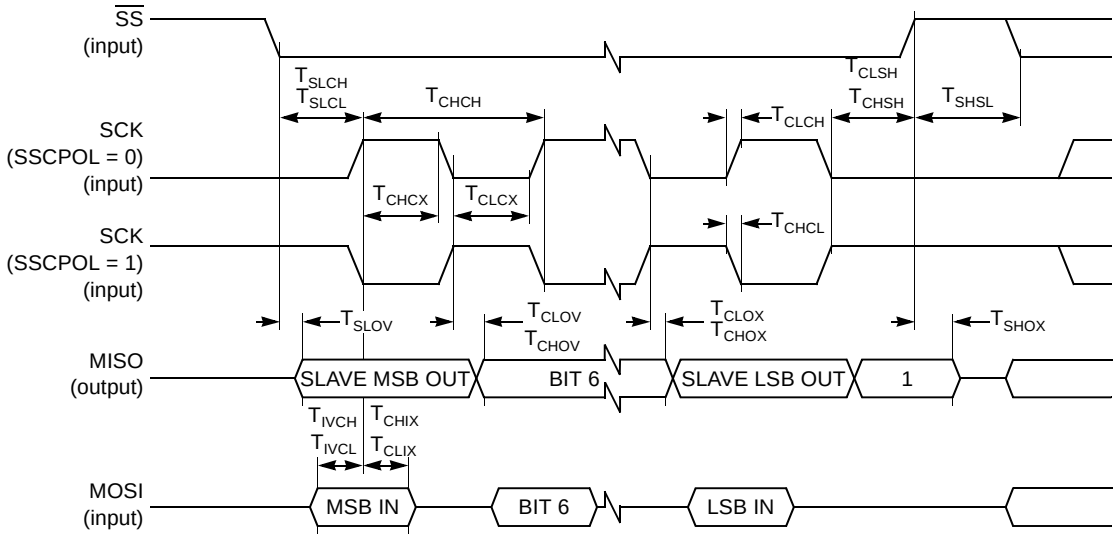
Table 8. SPI Interface Master AC Timing
V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Min	Max	Unit
Slave Mode				
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	$\overline{SS}$ Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	$\overline{SS}$ High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	$\overline{SS}$ Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after $\overline{SS}$ High		130	ns
T_{SHSL}	$\overline{SS}$ High to $\overline{SS}$ Low	(1)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise Time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master Mode				
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise Time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

Notes: 1. Value of this parameter depends on software.
2. Test conditions: capacitive load on all pins = 100 pF

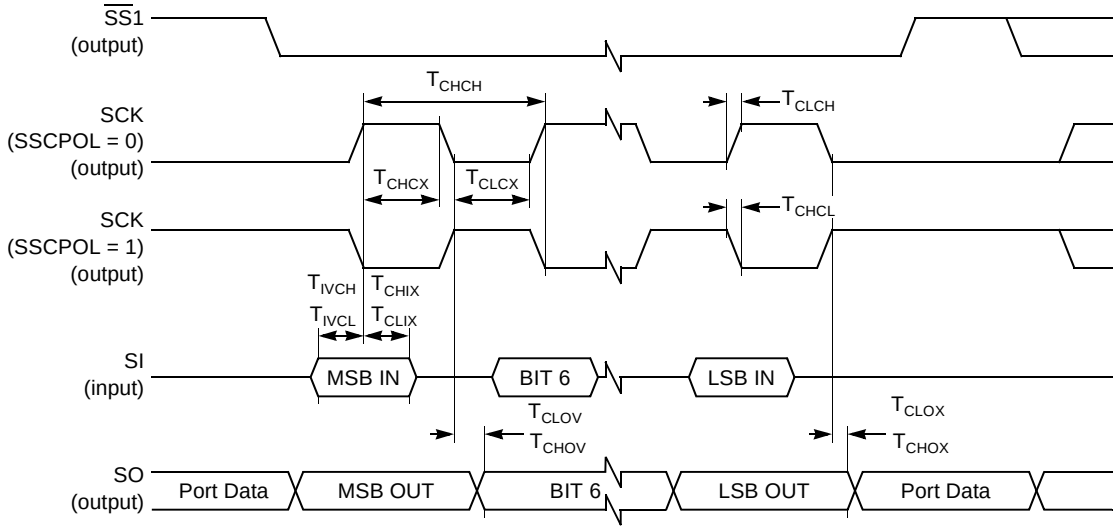
Waveforms

Figure 5. SPI Slave Waveforms (SSCPHA = 0)



Note: 1. Not Defined but generally the MSB of the character which has just been received.

Figure 6. SPI Slave Waveforms (SSCPHA = 1)



Note: 1. Not Defined but generally the LSB of the character which has just been received.

MMC Interface

Definition of Symbols

Table 9. MMC Interface Timing Symbol Definitions

Signals	
C	Clock
D	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

Timings

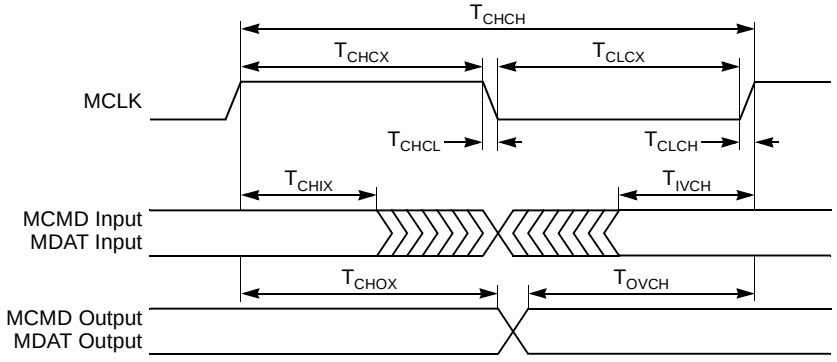
Table 10. MMC Interface AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C, CL ≤ 100pF (10 cards)

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period	50		ns
T_{CHCX}	Clock High Time	10		ns
T_{CLCX}	Clock Low Time	10		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{DVCH}	Input Data Valid to Clock High	3		ns
T_{CHDX}	Input Data Hold after Clock High	3		ns
T_{CHOX}	Output Data Hold after Clock High	5		ns
T_{OVCH}	Output Data Valid to Clock High	5		ns

Waveforms

Figure 10. MMC Input Output Waveforms



Audio Interface

Definition of Symbols

Table 11. Audio Interface Timing Symbol Definitions

Signals	
C	Clock
O	Data Out
S	Data Select

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

Timings

Table 12. Audio Interface AC timings

V_{DD} = 2.7 to 3.3V, T_A = -40 to +85°C, CL ≤ 30pF

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period		325.5(1)	ns
T_{CHCX}	Clock High Time	30		ns
T_{CLCX}	Clock Low Time	30		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{CLSV}	Clock Low to Select Valid		10	ns
T_{CLOV}	Clock Low to Data Valid		10	ns

Note: 32-bit format with Fs = 48 kHz.

Waveforms

Figure 11. Audio Interface Waveforms

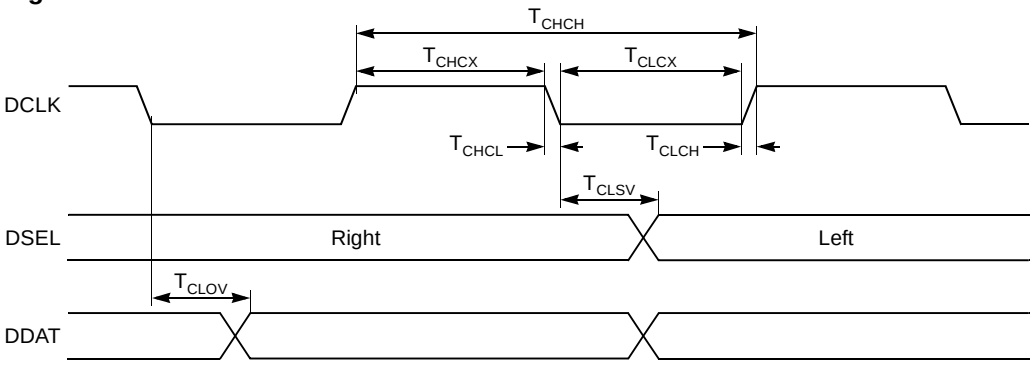
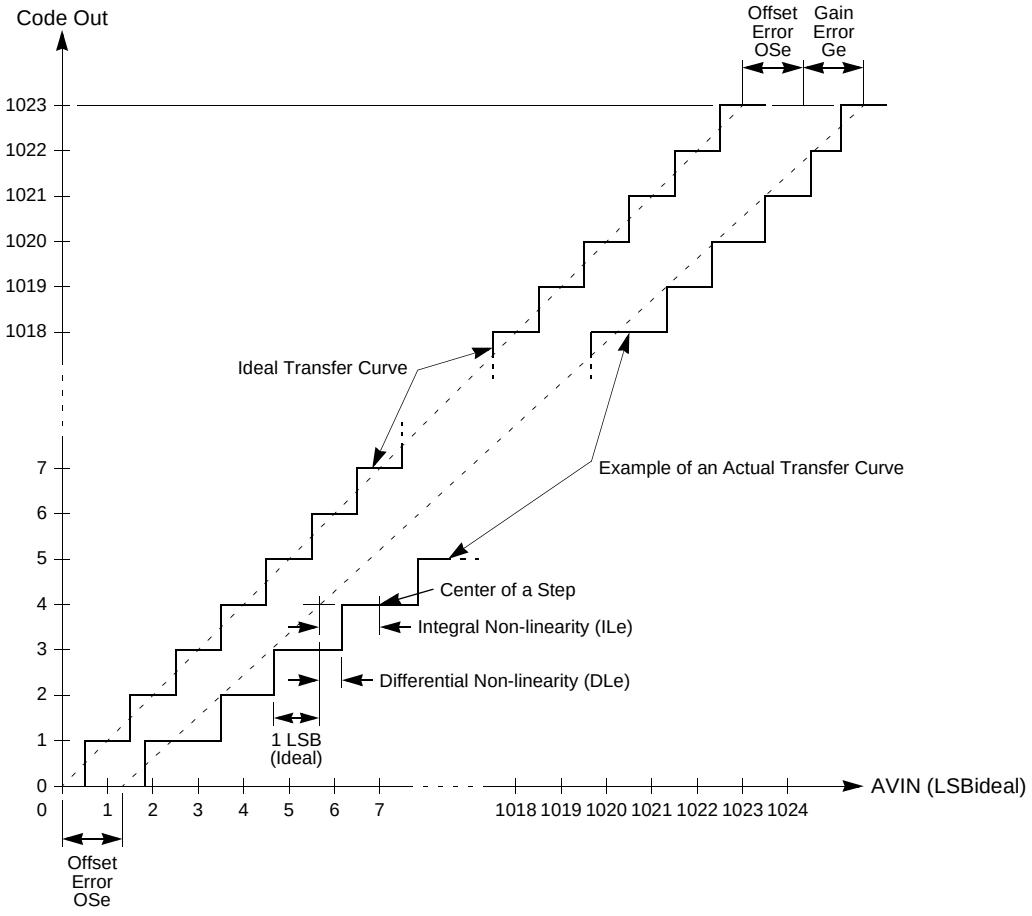


Figure 13. Analog-to-Digital Converter Characteristics



Flash Memory

Definition of Symbols

Table 14. Flash Memory Timing Symbol Definitions

Signals	
S	$\overline{ISP}$
R	RST
B	FBUSY flag

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

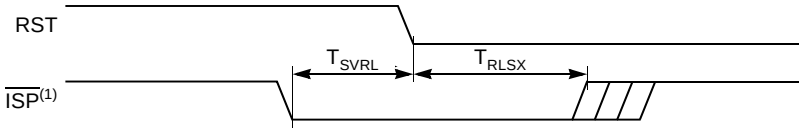
Table 15. Flash Memory AC Timing

V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
T_{SVRL}	Input $\overline{ISP}$ Valid to RST Edge	50			ns
T_{RLSX}	Input $\overline{ISP}$ Hold after RST Edge	50			ns
T_{BHBL}	FLASH Internal Busy (Programming) Time		10		ms
N_{FCY}	Number of Flash Write Cycles	100K			Cycle
T_{FDR}	Flash Data Retention Time	10			Year

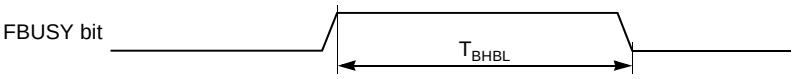
Waveforms

Figure 14. Flash Memory – ISP Waveforms



Note: 1. $\overline{ISP}$ must be driven through a pull-down resistor (see Section “In-system Programming”, page 22).

Figure 15. Flash Memory – Internal Busy Waveforms



External Clock Drive and Logic Level References

Definition of Symbols

Table 16. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

Timings

Table 17. External Clock AC Timings

V_{DD} = 2.7 to 3.3V, T_A= -40 to +85°C

Symbol	Parameter	Min	Max	Unit
T_{CLCL}	Clock Period	50		ns
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns
T_{CR}	Cyclic Ratio in X2 Mode	40	60	%

Waveforms

Figure 16. External Clock Waveform

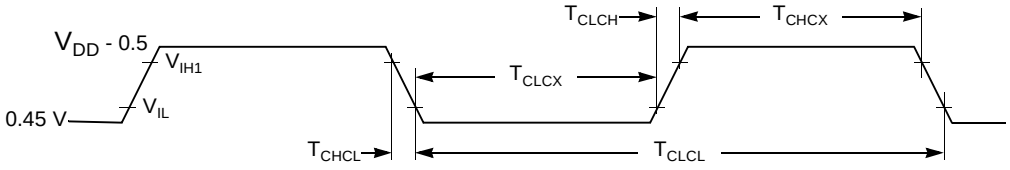
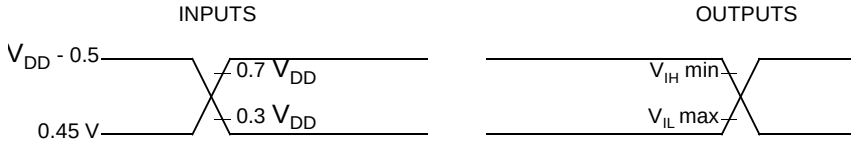
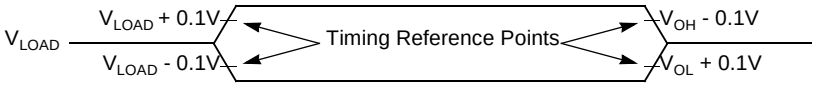


Figure 17. AC Testing Input/Output Waveforms



Notes: 1. During AC testing, all inputs are driven at V_{DD} -0.5V for a logic 1 and 0.45V for a logic 0.
2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Figure 18. Float Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} = \pm 20$ mA.

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