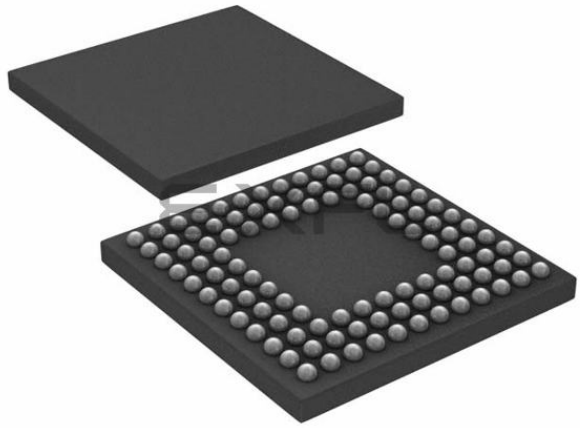

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 11x12b; D/A 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	108-LFBGA, CSPBGA
Supplier Device Package	108-CSPBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7120bbcz-rl

ABSOLUTE MAXIMUM RATINGS

AGND = 0 V, T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
AVDD to IOVDD	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOVDD to IOGND, AVDD to AGND	−0.3 V to +6 V
Digital Input Voltage to IOGND	−0.3 V to +5.3 V
Digital Output Voltage to IOGND	−0.3 V to IOV_{DD} + 0.3 V
V_{REF}_2.5 and V_{REF}_1.2 to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Outputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environments. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CSP_BGA[1]	40	12	°C/W

[1] Test Condition 1: Thermal impendance simulated values are based on JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

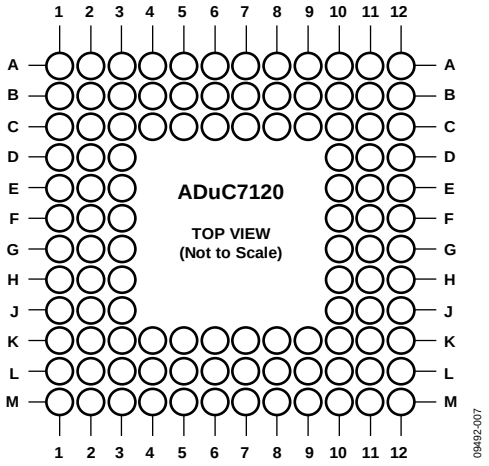

Figure 7. ADuC7020 Pin Configuration

Table 10. ADuC7120 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	IDAC1	AO	IDAC1 Output. The output for this pin is 200 mA.
A2	PVDD_IDAC1	S	Power for IDAC1.
A3	PVDD_IDAC1	S	Power for IDAC1.
A4	IDAC1	AO	IDAC1 Output. The output for this pin is 200 mA.
A5	IDAC3	AO	IDAC3 Output. The output for this pin is 80 mA.
A6	C_{DAMP}_IDAC4	AI	Damping Capacitor Pin for IDAC4.
A7	PVDD_IDAC2	S	2.0 V Power for IDAC2.
A8	IDAC2	AO	IDAC2 Output. The output for this pin is 45 mA.
A9	IDAC0	AO	IDAC0 Output. The output for this pin is 250 mA.
A10	PVDD_IDAC0	S	Power for IDAC0.
A11	PVDD_IDAC0	S	Power for IDAC0.
A12	IDAC0	AO	IDAC0 Output. The output for this pin is 250 mA.
B1	C_{DAMP}_IDAC1	AI	Damping Capacitor for IDAC1.
B2	P1.7/PLAO[4]	I/O	General-Purpose Input and Output (GPIO) Port 1.7 (P1.7). Programmable Logic Array for Output Element 4 (PLAO[4]).
B3	P1.6/PLAO[5]	I/O	General-Purpose Input and Output Port 1.6 (P1.6). Programmable Logic Array for Output Element 5 (PLAO[5]).
B4	C_{DAMP}_IDAC3	AI	Damping Capacitor for IDAC3.
B5	IDAC4	AO	IDAC4 Output. The output for this pin is 20 mA.
B6	AGND	S	Analog Ground.
B7	AVDD_IDAC	S	Output of 2.5 V LDO Regulator for Internal IDACs. Connect a 470 nF capacitor to AGND to this pin.
B8	I_{REF}	AI/O	Generates Reference Current for IDACs. Set by the external resistor, R_{EXT}.
B9	PGND	S	Power Ground.
B10	PGND	S	Power Ground.
B11	IDAC_TST	AI/O	IDAC Test Purposes.
B12	C_{DAMP}_IDAC0	AI	Damping Capacitor Pin for IDAC0.
C1	P2.6/IRQ3/PLAI[15]	I/O	General-Purpose Input and Output Port 2.6 (P2.6). External Interrupt Request 3, Active High (IRQ3). Programmable Logic Array for Input Element 15 (PLAI[15]).

Pin No.	Mnemonic	Type[1]	Description
E3	P0.4/MOSI/PLAI[11]/TRIP	I/O	General-Purpose Input and Output Port 0.4 (P0.4). SPI Master Out Slave In (MOSI). Programmable Logic Array for Input Element 11 (PLAI[11]). PWM Trip Interrupt (TRIP). The TRIP function of Pin E3 is the input that allows the PWM trip interrupt to be triggered.
E10	TMS	DI	JTAG Test Port Input, Test Mode Select. Debug and download access.
E11	P0.1/SDA0/PLAI[4]	I/O	General-Purpose Input and Output Port 0.1 (P0.1). I^2C Interface Serial Data for I^2C0 (SDA0). Programmable Logic Array for Input Element 4 (PLAI[4]).
E12	P3.7/$\overline{BM}$/PLAO[11]	I/O	General-Purpose Input and Output Port 3.7 (P3.7). Boot Mode ($\overline{BM}$). Programmable Logic Array for Output Element 11 (PLAO[11]).
F1	DGND	S	Digital Ground.
F2	P3.5/PLAO[9]	I/O	General-Purpose Input and Output Port 3.5 (P3.5). Programmable Logic Array for Output Element 9 (PLAO[9]).
F3	P0.5/$\overline{CS}$/PLAI[10]/ADC$_{\overline{CONVST}}$	I/O	General-Purpose Input and Output Port 0.5 (P0.5). SPI Slave Select Input ($\overline{CS}$). Programmable Logic Array for Input Element 10 (PLAI[10]). ADC Conversions (ADC$_{\overline{CONVST}}$). The ADC$_{\overline{CONVST}}$ function of Pin F3 initiates the ADC conversions using the PLA or the timer output.
F10	TCK	DI	JTAG Test Port Input, Test Clock. Debug and download access.
F11	P2.0/IRQ0/PLAI[13]	I/O	General-Purpose Input and Output Port 2.0 (P2.0). External Interrupt Request 0, Active High (IRQ0). Programmable Logic Array for Input Element 13 (PLAI[13]).
F12	DGND	S	Digital Ground.
G1	DVDD	S	Output of 2.6 V On-Chip LDO Regulator. Connect a 470 nF capacitor to DGND to this pin.
G2	XTALO	DO	Crystal Oscillator Inverter Output. If an external crystal is not used, this pin can remain unconnected.
G3	P0.6/$\overline{MRST}$/PLAI[2]	I/O	General-Purpose Input and Output Port 0.6 (P0.6). Power On Reset Output ($\overline{MRST}$). Programmable Logic Array for Input Element 2 (PLAI[2]).
G10	P0.7/$\overline{TRST}$/PLAI[3]	I/O	General-Purpose Input and Output Port 0.7 (P0.7). JTAG Test Port Input, Test Reset ($\overline{TRST}$). Debug and download access. Programmable Logic Array for Input Element 3 (PLAI[3]).
G11	P2.1/IRQ1/PLAI[12]	I/O	General-Purpose Input and Output Port 2.1 (P2.1) External Interrupt Request 1, Active High (IRQ1). Programmable Logic Array for Input Element 12 (PLAI[12]).
G12	DVDD	S	Output of 2.6 V On-Chip LDO Regulator. Connect a 470 nF capacitor to DGND to this pin.
H1	IOVDD	S	3.3 V GPIO Supply.
H2	XTALI	DI	Crystal Oscillator Inverter Input and Internal Clock Generator Circuits Input. If an external crystal is not used, connect this pin to the DGND system ground.
H3	P1.4/PWM1/ECLK/XCLK/PLAI[8]	I/O	General-Purpose Input and Output Port 1.4 (P1.4). Pulse-Width Modulator 1 Output (PWM1). Base System Clock Output (ECLK). Base System Clock Input (XCLK). Programmable Logic Array for Input Element 8 (PLAI[8]).
H10	P2.4/PWM5/PLAO[7]	I/O	General-Purpose Input and Output Port 2.4 (P2.4). Pulse-Width Modulator 5 Output (PWM5). Programmable Logic Array for Output Element 7 (PLAO[7]).
H11	P2.2/PLAI[1]	I/O	General-Purpose Input and Output Port 2.2 (P2.2). Programmable Logic Array for Input Element 1 (PLAI[1]).
H12	IOVDD	S	3.3 V GPIO Supply.

OVERVIEW OF THE ARM7TDMI CORE

The ARM7™ core is a 32-bit reduced instruction set computer (RISC). It uses a single 32-bit bus for instruction and data. The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 32 bits.

The ARM7TDMI® is an ARM7 core with four additional features, as follows:

- T support for the thumb (16-bit) instruction set
- D support for debug
- M support for long multiplications
- I includes the EmbeddedICE™ module to support embedded system debugging

THUMB (T) MODE

An ARM® instruction is 32 bits long. The ARM7TDMI processor supports a second instruction set that has been compressed into 16 bits, the Thumb® instruction set. Faster execution from 16-bit memory and greater code density can usually be achieved by using the Thumb instruction set instead of the ARM instruction set, which makes the ARM7TDMI core suitable for embedded applications.

However, the Thumb mode has the following two limitations:

- Thumb code typically requires more instructions for the same job. As a result, ARM code is usually best for maximizing the performance of time critical code.
- The Thumb instruction set does not include some of the instructions needed for exception handling, which automatically switches the core to ARM code for exception handling.

See the ADuC7XXX Microconverter™ Get Started Guide for details on the core architecture, the programming model, and both the ARM and ARM Thumb instruction sets.

LONG MULTIPLY (M)

The ARM7TDMI instruction set includes four extra instructions that perform 32-bit by 32-bit multiplication with a 64-bit result, and 32-bit by 32-bit multiplication accumulation (MAC) with a 64-bit result. These results are achieved in fewer cycles than required on a standard ARM7 core.

EmbeddedICE (I)

EmbeddedICE provides integrated on-chip support for the core. The EmbeddedICE module contains the breakpoint and watchpoint registers that halts code for debugging purposes. These registers are controlled through the JTAG test port.

When a breakpoint or watchpoint is encountered, the processor halts and enters a debug state. When in a debug state, the breakpoint and watchpoint registers can be inspected, as well as the Flash/EE, static random access memory (SRAM), and memory mapped registers.

EXCEPTIONS

ARM supports five types of exceptions and a privileged processing mode for each type. The five exception types include the following:

- Normal interrupt (IRQ) can service general-purpose interrupt handling of internal and external events.
- Fast interrupt (FIQ) can service data transfers or communication channels with low latency.; FIQ has priority over IRQ.
- Memory abort.
- Attempted execution of an undefined instruction.
- Software interrupt instruction (SWI) can make a call to an operating system.

Typically, the programmer defines interrupt as IRQ, but for higher priority interrupt, that is, faster response time, the programmer can define interrupt as FIQ.

Address	Name	Byte	Access Type	Cycle
0x0940	I2C1ID1	1	R/W	2
0x0944	I2C1ID2	1	R/W	2
0x0948	I2C1ID3	1	R/W	2
0x094C	I2C1FSTA	1	R/W	2

Table 24. SPI Base Address = 0xFFFF0A00

Address	Name	Byte	Access Type	Cycle
0x0A00	SPISTA	2	R	2
0x0A04	SPIRX	1	R	2
0x0A08	SPITX	1	W	2
0x0A0C	SPIDIV	1	R/W	2
0x0A10	SPICON	2	R/W	2

Table 25. PLA Base Address = 0xFFFF0B00

Address	Name	Byte	Access Type	Cycle
0x0B00	PLAELM0	2	R/W	2
0x0B04	PLAELM1	2	R/W	2
0x0B08	PLAELM2	2	R/W	2
0x0B0C	PLAELM3	2	R/W	2
0x0B10	PLAELM4	2	R/W	2
0x0B14	PLAELM5	2	R/W	2
0x0B18	PLAELM6	2	R/W	2
0x0B1C	PLAELM7	2	R/W	2
0x0B20	PLAELM8	2	R/W	2
0x0B24	PLAELM9	2	R/W	2
0x0B28	PLAELM10	2	R/W	2
0x0B2C	PLAELM11	2	R/W	2
0x0B30	PLAELM12	2	R/W	2
0x0B34	PLAELM13	2	R/W	2
0x0B38	PLAELM14	2	R/W	2
0x0B3C	PLAELM15	2	R/W	2
0x0B40	PLACLK	1	R/W	2
0x0B44	PLAIRQ	2	R/W	2
0x0B48	PLAADC	4	R/W	2
0x0B4C	PLADIN	4	R/W	2
0x0B50	PLADOUT	4	R	2
0x0B54	PLALCK	1	W	2

Table 26. GPIO Base Address = 0xFFFF0D00

Address	Name	Byte	Access Type	Cycle
0x0D00	GP0CON	4	R/W	1
0x0D04	GP1CON	4	R/W	1
0x0D08	GP2CON	4	R/W	1
0x0D0C	GP3CON	4	R/W	1
0x0D20	GP0DAT	4	R/W	1
0x0D24	GP0SET	1	W	1
0x0D28	GP0CLR	1	W	1
0x0D2C	GP0PAR	4	R/W	1
0x0D30	GP1DAT	4	R/W	1
0x0D34	GP1SET	1	W	1
0x0D38	GP1CLR	1	W	1
0x0D3C	GP1PAR	4	R/W	1
0x0D40	GP2DAT	4	R/W	1
0x0D44	GP2SET	1	W	1
0x0D48	GP2CLR	1	W	1
0x0D4C	GP2PAR	4	R/W	1
0x0D50	GP3DAT	4	R/W	1
0x0D54	GP3SET	1	W	1
0x0D58	GP3CLR	1	W	1
0x0D5C	GP3PAR	4	R/W	1

Table 27. Flash/EE Block 0 Base Address = 0xFFFF0E00

Address	Name	Byte	Access Type	Cycle
0x0E00	FEE0STA	1	R	1
0x0E04	FEE0MOD	1	R/W	1
0x0E08	FEE0CON	1	R/W	1
0x0E0C	FEE0DAT	2	R/W	1
0x0E10	FEE0ADR	2	R/W	1
0x0E18	FEE0SGN	3	R	1
0x0E1C	FEE0PRO	4	R/W	1
0x0E20	FEE0HID	4	R/W	1

Table 28. Flash/EE Block 1 Base Address = 0xFFFF0E80

Address	Name	Byte	Access Type	Cycle
0x0E80	FEE1STA	1	R	1
0x0E84	FEE1MOD	1	R/W	1
0x0E88	FEE1CON	1	R/W	1
0x0E8C	FEE1DAT	2	R/W	1
0x0E90	FEE1ADR	2	R/W	1
0x0E98	FEE1SGN	3	R	1
0x0E9C	FEE1PRO	4	R/W	1
0x0EA0	FEE1HID	4	R/W	1

Table 29. PWM Base Address= 0xFFFF0F80

Address	Name	Byte	Access Type	Cycle
0x0F80	PWMCON1	2	R/W	2
0x0F84	PWM1COM1	2	R/W	2
0x0F88	PWM1COM2	2	R/W	2
0x0F8C	PWM1COM3	2	R/W	2
0x0F90	PWM1LEN	2	R/W	2
0x0F94	PWM2COM1	2	R/W	2
0x0F98	PWM2COM2	2	R/W	2
0x0F9C	PWM2COM3	2	R/W	2
0x0FA0	PWM2LEN	2	R/W	2
0x0FA4	PWM3COM1	2	R/W	2
0x0FA8	PWM3COM2	2	R/W	2
0x0FAC	PWM3COM3	2	R/W	2
0x0FB0	PWM3LEN	2	R/W	2
0x0FB4	PWMCON2	2	R/W	2
0x0FB8	PWMICLR	2	W	2

POWER SUPPLY MONITOR (PSM)

The PSM on the ADuC7120/ADuC7121 indicates when the IOVDD supply pin drops below one of two supply trip points. The monitor function is controlled via the PSMCON register. If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit clears immediately after the CMP bit goes high. If the interrupt generated is exited before CMP goes high (IOVDD supply voltage is above the trip point), no further interrupts are generated until CMP returns high. The user must ensure that the code execution remains within the interrupt service routine (ISR) until CMP returns high.

This monitor function allows the user to save working registers to avoid possible data loss due to low supply or brownout conditions. It also ensures that normal code execution does not resume until a safe supply level is established.

The PSM does not operate correctly when using JTAG debug; therefore, disable PSM while in JTAG debug mode.

Table 44. PSMCON MMR Bit Designations (Address = 0xFFFF0440, Default Value = 0x0008)

Bit(s)	Name	Description
[15:4]	Reserved	These bits are reserved.
3	CMP	Comparator bit. This is a read only bit that directly reflects the state of the comparator. Read 1 indicates that the IOVDD supply is above its selected trip point or the PSM is in power-down mode. Read 0 indicates the IOVDD supply is below its selected trip point. Set this bit before leaving the interrupt service routine.
2	TP	Trip point selection bit. 0 = 2.79 V. 1 = 3.07 V.
1	PSMEN	Power supply monitor enable bit. Set to 1 to enable the power supply monitor circuit. Cleared to 0 to disable the power supply monitor circuit.
0	PSMI	Power supply monitor interrupt bit. This bit is set high by the MicroConverter if the CMP bit is low, indicating low input/output supply. The PSMI bit can interrupt the processor. When the CMP bit returns high, the PSMI bit can be cleared by writing a 1 to this location. Writing a 0 to this location has no effect. There is no timeout delay. PSMI can be cleared immediately after the CMP bit goes high.

Bit(s)	Description
1	Command fail. Set automatically when a command completes unsuccessfully. Cleared automatically when reading FEExSTA register.
0	Command complete. Set by MicroConverter when a command is complete. Cleared automatically when reading FEExSTA register.

FEE0MOD Register

Name: FEE0MOD

Address: 0xFFFF0E04

Default value: 0x80

Access: Read and write

FEE1MOD Register

Name: FEE1MOD

Address: 0xFFFF0E84

Default value: 0x80

Access: Read and write

Table 48. FEExMOD MMR Bit Designations

Bit(s)	Description
[7:5]	Reserved. These bits are always set to 0 except when writing keys. See the Sequence to Write the Key to Protection Registers section for details.
4	Flash/EE interrupt enable. Set by the user to enable the Flash/EE interrupt. The interrupt occurs when a command is complete. Cleared by the user to disable the Flash/EE interrupt.
3	Erase/write command protection. Set by the user to enable the erase and write commands. Cleared to protect the Flash/EE memory against erase/write command.
2	Reserved. The user must set this bit to 0.
[1:0]	Flash/EE wait states. Both Flash/EE blocks must have the same wait state value for any change to take effect.

FEE0CON Register

Name: FEE0CON

Address: 0xFFFF0E08

Default value: 0x00

Access: Read and write

FEE1CON Register

Name: FEE1CON

Address: 0xFFFF0E88

Default value: 0x00

Access: Read and write

Table 49. Command Codes in FEExCON

Code	Command	Description
0x00[1]	Null	Idle state.
0x01[1]	Single read	Load FEExDAT with the 16-bit data indexed by FEExADR.
0x02[1]	Single write	Write FEExDAT at the address pointed by FEExADR. This operation takes 50 µs.
0x03[1]	Erase/write	Erase the page indexed by FEExADR and write FEExDAT at the location pointed by FEExADR. This operation takes 20 ms.
0x04[1]	Single verify	Compare the contents of the location pointed by FEExADR to the data in FEExDAT. The result of the comparison is returned in FEExSTA Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEExADR.
0x06[1]	Mass erase	Erase user space. The 2 kB of kernel are protected in Block 0. This operation takes 2.48 sec. To prevent accidental execution, a command sequence is required to execute this instruction.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	Gives a signature of the 64 kB of Flash/EE in the 24-bit FEExSIGN MMR. This operation takes 32,778 clock cycles.
0x0C	Protect	This command can run only once. The value of FEExPRO is saved and can be removed only with a mass erase (0x06) or with the key.
0x0D	Reserved	Reserved.
0x0E	Reserved	Reserved.
0x0F	Ping	No operation, interrupt generated.

[1] The FEExCON register always reads 0x07 immediately after execution of any of these commands.

IDAC MMRS

Table 61. IDAC Control Registers (Read and Write Access)

Name	Address (Hex)	Default Value
IDAC0CON	0xFFFF0700	0x0010
IDAC1CON	0xFFFF070C	0x0010
IDAC2CON	0xFFFF0718	0x0010
IDAC3CON	0xFFFF0724	0x0010
IDAC4CON	0xFFFF0730	0x0010
TDSCON	0xFFFF073C	0x00
IDAC0PULLDOWN	0xFFFF0744	0x00

Table 62. IDACxCON MMR Bit Designations

Bit(s)	Name	Setting	Description
[15:9]			These bits are reserved.
[8:7]	SFHMODE		Bit shuffling is a method of increasing the ac precision of an IDAC. Do not use in applications where dc performance is important.
		00	Shuffle one increment at a time.
		01	Shuffle based on an internal counter.
		10	Shuffle based on the input data.
		11	Reserved.
6	MSBSHFEN	0	MSB shuffle enable. Set by the user to 1 to enable MSB shuffling. Set by the user to 0 to disable MSB shuffling.
5	LSBSHFEN	0	LSB shuffle enable. Set by the user to 1 to enable LSB shuffling. Set by the user to 0 to disable LSB shuffling.
4	IDACPD	1	IDAC power-down bit. Set by the user to 1 to power down the IDAC. IDAC output is high impedance. Set by the user to 0 to power up the IDAC.
3	IDACCLK	0	IDAC update rate. Set by the user to update the IDAC using Timer1. Cleared by the user to update the IDAC using HCLK (core clock).
2	IDACCLR	0	IDAC clear bit. Set by the user to enable normal IDAC operation. Cleared by the user to reset data register of the IDAC to 0.
1	Mode	0	Mode bit. This bit must always be cleared.
0	Reserved	0	Set this bit to 0.

Table 63. TDSCON MMR Bit Designations

Bit(s)	Name	Setting	Description
[7:3]	Reserved		The user sets these bits to 0.
2	Reserved		The user must set this to 1.
1	DISINT	0	Disable thermal trigger interrupt. Set by the user to 0 to generate an interrupt if the temperature passes the thermal shutdown point.
0	DISSD	0	Set by the user to 0 to disable the output current DACs when the temperature passes a trip point.

Table 64. IDAC0PULLDOWN MMR Bit Designations

Bit(s)	Name	Setting	Description
[7:6]	Reserved		These bits are set to 0 by the user.
5	Pulldown	0	IDAC0 pull-down. Set to 1 by the user to pull down the IDAC0 pin as well as power down IDAC0. Set to 0 by the user to disable the pull-down.
4	PLA_PD_EN	0	PLA output trigger enable. Set to 1 by the user to enable the PLA output to trigger the IDAC0 pull-down. Set to 0 by the user to disable this feature.
3:0	PLA Source		PLA output source for PLA output trigger enable. Can select the output of any element, 0 to 15, by programming these bits with the corresponding binary value.

Table 65. IDAC Data Registers (Default Value = 0x00000000, Read and Write Access)

Name	Address (Hex)
IDAC0DAT	0xFFFF0704
IDAC1DAT	0xFFFF0710
IDAC2DAT	0xFFFF071C
IDAC3DAT	0xFFFF0728
IDAC4DAT	0xFFFF0734

Table 66. IDACxDAT MMR Bit Designations

Bit(s)	Name	Setting	Description
[31:28]	Reserved		These bits are reserved.
[27:17]	Data		Data from IDACx.
[16:0]	Reserved	000	These bits are reserved.

In case of crystal loss, use the watchdog timer. During initialization, a test on the RSTSTA register can determine if the reset came from the watchdog timer.

Example Source Code for External Crystal Selection

```
     T2LD = 5;
     TCON = 0x480;


  while ((T2VAL == t2val_old) || (T2VAL > 3))
//ensures timer value loaded
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x01;
  PLLKEY2 = 0x55;


  POWKEY1 = 0x01;
  POWCON = 0x27;
// set core into nap mode
  POWKEY2 = 0xF4;
```

External Clock Selection

To switch to an external clock on P1.4 (of the P1.4/PWM1/ECLK/XCLK/PLAI[8] pin), configure P1.4 using PLLCON register. The external clock can be up to 41.78 MHz.

Example Source Code for External Clock Selection

```
     T2LD = 5;
     TCON = 0x480;
  while ((T2VAL == t2val_old) || (T2VAL > 3))
//ensures timer value loaded
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x03; //Select external clock
  PLLKEY2 = 0x55;


  POWKEY1 = 0x01;
  POWCON = 0x27; // Set Core into Nap mode
  POWKEY2 = 0xF4;
```

Power Control System

These devices offer a choice of operating modes. Table 71 describes what part of the ADuC7120/ADuC7121 is powered on in the different modes and indicates the power-up time. Table 72 gives some typical values of the total current consumption (analog + digital supply currents) in the different modes, depending on the clock divider bits. The ADC is turned off. These values also include current consumption of the regulator and other parts on the test board on which these values are measured.

Table 71. Operating Modes

Mode	Core	Peripherals	PLL	XTAL/Timer2/Timer3	External IRQ	Start-Up/Power-On Time
Active	On	On	On	On	On	66 ms at CD = 0
Pause	Off	On	On	On	On	24 ns at CD = 0; 3.06 µs at CD = 7
Nap	Off	Off	On	On	On	24 ns at CD = 0; 3.06 µs at CD = 7
Sleep	Off	Off	Off	On	On	1.58 ms
Stop	Off	Off	Off	Off	On	1.7 ms

Table 72. Typical Current Consumption at 25°C

PC Bits, Bits[2:0]	Mode	CD = 0	CD = 1	CD = 2	CD = 3	CD = 4	CD = 5	CD = 6	CD = 7
000	Active	33.1	21.2	13.8	10	8.1	7.2	6.7	6.45
001	Pause	22.7	13.3	8.5	6.1	4.9	4.3	4	3.85
010	Nap	3.8	3.8	3.8	3.8	3.8	3.8	3.8	3.8
011	Sleep	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
100	Stop	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

MMRs and Keys

To prevent accidental programming, a certain sequence must be followed when writing in the PLLCON and POWCON registers (see Table 75).

PLLKEYx Registers

Name: PLLKEY1

Address: 0xFFFF0410

Default value: 0x0000

Access: Write only

Name: PLLKEY2

Address: 0xFFFF0418

Default value: 0x0000

Access: Write only

PLLCON Register

Name: PLLCON

Address: 0xFFFF0414

Default value: 0x21

Access: Read and write

Table 73. PLLCON MMR Bit Designations

Bit(s)	Name	Setting	Description
[7:6]			Reserved.
5	OSEL		32 kHz PLL input selection.
			Set by the user to use the internal 32 kHz oscillator.
			Set by default.
			Cleared by the user to use the external 32 kHz crystal.
[4:2]			Reserved.
[1:0]	MDCLK		Clocking modes.
		00	Reserved.
		01	PLL. Default configuration.
		10	Reserved.
		11	External clock on the P1.4/PWM1/ECLK/XCLK/PLAI[8] pin.

POWKEYx Registers

Name: POWKEY1

Address: 0xFFFF0404

Default value: 0x0000

Access: Write only

Name: POWKEY2

Address: 0xFFFF040C

Default value: 0x0000

Access: Write only

POWCON Register

Name: POWCON

Address: 0xFFFF0408

Default value: 0x0003

Access: Read and write

Table 74. POWCON MMR Bit Designations

Bit(s)	Name	Setting	Description
7			Reserved.
[6:4]	PC		Operating modes.
		000	Normal mode.
		001	Pause mode.
		010	Nap mode.
		011	Sleep mode. IRQ0 to IRQ3 and Timer2 can wake up the devices.
		100	Stop mode.
		Others	Reserved.
3	RSVD		Reserved.
[2:0]	CD		CPU clock divider bits.
		000	41.779200 MHz.
		001	20.889600 MHz.
		010	10.444800 MHz.
		011	5.222400 MHz.
		100	2.611200 MHz.
		101	1.305600 MHz.
		110	654.800 kHz.
		111	326.400 kHz.

Table 75. PLLCON and POWCON Write Sequence

PLLCON	POWCON
PLLKEY1 = 0xAA	POWKEY1 = 0x01
PLLCON = 0x01	POWCON = user value
PLLKEY2 = 0x55	POWKEY2 = 0xF4

DIGITAL PERIPHERALS

PULSE-WIDTH MODULATOR (PWM) OVERVIEW

The ADuC7120/ADuC7121 integrate a 6-channel PWM interface. The PWM outputs can drive an H-bridge or can be used as standard PWM outputs. On power-up, the PWM outputs default to H-bridge mode, which ensures that the motor is turned off by default. In standard PWM mode, the outputs are arranged as three pairs of PWM pins. Users have control over the period of each pair of outputs and over the duty cycle of each individual output.

In all modes, the PWMxCOMx MMRs control the point at which the PWM outputs change state. An example of the first pair of PWM outputs (PWM1 and PWM2) timing is shown in Figure 35.

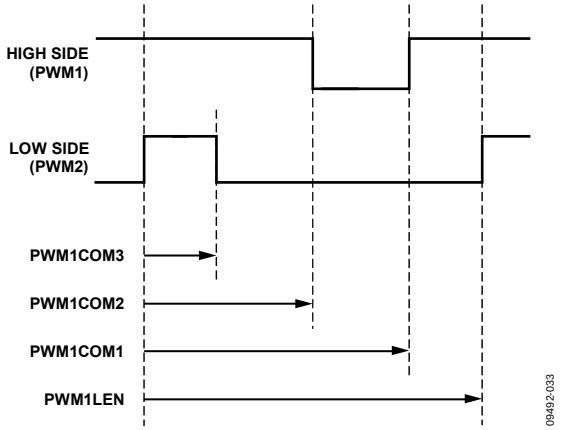

Figure 35. Example of the First Pair of PWM Outputs (PWM1 and PWM2) Timing

The PWM clock is selectable via the PWMCON1 register with one of the following values: UCLK divide by 2, divide by 4, divide by 8, divide by 16, divide by 32, divide by 64, divide by 128, or divide by 256. The length of a PWM period is defined by PWMxLEN.

The PWM waveforms are set by the count value of the 16-bit timer and the compare registers contents as shown with the PWM1 and PWM2 waveforms in Figure 35.

The low-side waveform, PWM2, goes high when the timer count reaches PWM1LEN, and it goes low when the timer count reaches the value held in PWM1COM3 or when the high-side waveform PWM1 goes low.

The high-side waveform, PWM1, goes high when the timer count reaches the value held in PWM1COM1, and it goes low when the timer count reaches the value held in PWM1COM2.

Table 76. PWM MMRs

Name	Function
PWMCON1	PWM control
PWM1COM1	Compare Register 1 for PWM Output 1 and PWM Output 2
PWM1COM2	Compare Register 2 for PWM Output 1 and PWM Output 2
PWM1COM3	Compare Register 3 for PWM Output 1 and PWM Output 2
PWM1LEN	Frequency control for PWM Output 1 and PWM Output 2
PWM2COM1	Compare Register 1 for PWM Output 3 and PWM Output 4
PWM2COM2	Compare Register 2 for PWM Output 3 and PWM Output 4
PWM2COM3	Compare Register 3 for PWM Output 3 and PWM Output 4
PWM2LEN	Frequency control for PWM Output 3 and PWM Output 4
PWM3COM1	Compare Register 1 for PWM Output 5 and PWM Output 6
PWM3COM2	Compare Register 2 for PWM Output 5 and PWM Output 6
PWM3COM3	Compare Register 3 for PWM Output 5 and PWM Output 6
PWM3LEN	Frequency control for PWM Output 5 and PWM Output 6
PWMCON2	PWM convert start control
PWMICLR	PWM interrupt clear

GENERAL-PURPOSE INPUT/OUTPUT

The ADuC7120/ADuC7121 provide 32 general-purpose, bidirectional input/output (GPIO) pins. All input/output pins are 5 V tolerant, meaning that the GPIOs support an input voltage of 5 V. In general, many of the GPIO pins have multiple functions (see Table 81). By default, the GPIO pins are configured in GPIO mode.

All GPIO pins have an internal pull-up resistor (of about 100 kΩ) and their drive capability is 1.6 mA. A maximum of 20 GPIOs can drive 1.6 mA at the same time. The 32 GPIOs are grouped into four ports: Port 0 to Port 3. Each port is controlled by four or five MMRs, with x representing the port number.

GPxCON Registers

Name: GP0CON

Address: 0xFFFF0D00

Default value: 0x11000000

Access: Read and write

Name: GP1CON

Address: 0xFFFF0D04

Default value: 0x00000000

Access: Read and write

Name: GP2CON

Address: 0xFFFF0D08

Default value: 0x00000000

Access: Read and write

Name: GP3CON

Address: 0xFFFF0D0C

Default value: 0x00000000

Access: Read and write

The input level of any GPIO can be read at any time in the GPxDAT MMR, even when the pin is configured in a mode other than GPIO. The PLA input is always active.

When the ADuC7120/ADuC7121 enter power-saving mode, the GPIO pins retain their state.

GPxCON is the Port x control register, and it selects the function of each pin of Port x, as described in Table 81.

Table 81. GPIO Pin Function Designations

		Configuration (See Table 82 for the GPxCON MMR Bit Designations)			
Port	**Pin**	**00**	**01**	**10**	**11**
0	P0.0	GPIO	SCL0		PLAI[5]
	P0.1	GPIO	SDA0	JTAG disabled	PLAI[4]
	P0.2	GPIO	SPICLK	JTAG disabled ADC_{BUSY}	PLAO[13]
	P0.3	GPIO	MISO	SYNC (PWM)	PLAO[12]
	P0.4	GPIO	MOSI	TRIP (PWM)	PLAI[11]
	P0.5	GPIO	$\overline{CS}$	$ADC_{\overline{CONVST}}$	PLAI[10]
	P0.6	GPIO	$\overline{MRST}$		PLAI[2]
	P0.7	GPIO	$\overline{TRST}$		PLAI[3]
1	P1.0	GPIO	SIN	SCL1	PLAI[7]
	P1.1	GPIO	SOUT	SDA1	PLAI[6]
	P1.2[1]	TDI (JTAG)			PLAO[15]
	P1.3[1]	TDO (JTAG)			PLAO[14]
	P1.4	GPIO	PWM1	ECLK/XCLK	PLAI[8]
	P1.5	GPIO	PWM2		PLAI[9]
	P1.6	GPIO			PLAO[5]
	P1.7	GPIO			PLAO[4]

Port	Pin	Configuration (See Table 82 for the GPxCON MMR Bit Designations)			
		00	01	10	11
2	P2.0	GPIO/IRQ0			PLAI[13]
	P2.1	GPIO/IRQ1			PLAI[12]
	P2.2	GPIO			PLAI[1]
	P2.3	GPIO/IRQ2			PLAI[14]
	P2.4	GPIO	PWM5		PLAO[7]
	P2.5	GPIO	PWM6		PLAO[6]
	P2.6	GPIO/IRQ3			PLAI[15]
	P2.7	GPIO			PLAI[0]
3	P3.0	GPIO			PLAO[0]
	P3.1	GPIO			PLAO[1]
	P3.2	GPIO/IRQ4	PWM3		PLAO[2]
	P3.3	GPIO/IRQ5	PWM4		PLAO[3]
	P3.4	GPIO			PLAO[8]
	P3.5	GPIO			PLAO[9]
	P3.6	GPIO			PLAO[10]
	P3.7	GPIO/$\overline{BM}$			PLAO[11]

[1] Reconfiguring these pins disables JTAG mode. Erase to reenable JTAG access after changing default value.

Table 82. GPxCON MMR Bit Designations

Bit(s)	Description
[31:30]	Reserved
[29:28]	Selects function of the Px.7 pin
[27:26]	Reserved
[25:24]	Selects function of the Px.6 pin
[23:22]	Reserved
[21:20]	Selects function of the Px.5 pin
[19:18]	Reserved
[17:16]	Selects function of the Px.4 pin
[15:14]	Reserved
[13:12]	Selects function of the Px.3 pin
[11:10]	Reserved
[9:8]	Selects function of the Px.2 pin
[7:6]	Reserved
[5:4]	Selects function of the Px.1 pin
[3:2]	Reserved
[1:0]	Selects function of the Px.0 pin

GPxPAR Registers

The GPxPAR registers program the parameters for Port 0, Port 1, Port 2, and Port 3. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR.

Name: GP0PAR

Address: 0xFFFF0D2C

Default value: 0x20000000

Access: Read and write

Name: GP1PAR

Address: 0xFFFF0D3C

Default value: 0x00000000

Access: Read and write

Name: GP2PAR

Address: 0xFFFF0D4C

Default value: 0x00000000

Access: Read and write

Name: GP3PAR

Address: 0xFFFF0D5C

Default value: 0x00222222

Access: Read and write

Table 83. GPxPAR MMR Bit Designations

Bit(s)	Description
[31:29]	Reserved
28	Pull-up disable Px.7 pin Set to 1 to enable the pull-up Clear to 0 to disable the pull-up
[27:25]	Reserved
24	Pull-up disable Px.6 pin
[23:21]	Reserved
20	Pull-up disable Px.5 pin
[19:17]	Reserved
16	Pull-up disable Px.4 pin

I²C Master Status Register

This 16-bit MMR is I²C status register in master mode.

Name: I2C0MSTA, I2C1MSTA

Address: 0xFFFF0884, 0xFFFF0904

Default value: 0x0000, 0x0000

Access: Read only

Table 96 I2CxMSTA MMR Bit Designations

Bit(s)	Name	Description
[15:11]		Reserved. These bits are reserved.
10	I2CBBUSY	I²C bus busy status bit. This bit is set to 1 when a start condition is detected on the I²C bus. This bit is cleared when a stop condition is detected on the I²C bus.
9	I2CMRxFO	Master receiver (Rx) FIFO overflow. This bit is set to 1 when a byte is written to the Rx FIFO when it is already full. This bit is cleared in all other conditions.
8	I2CMTC	I²C transmission complete status bit. This bit is set to 1 when a transmission is complete between the master and the slave with which it was communicating. If the I2CMCENI bit in I2CxMCTL is set, an interrupt is generated when the I2CMTC bit is set. Clear this interrupt source.
7	I2CMNA	I²C master no acknowledge data bit. This bit is set to 1 when a no acknowledge condition is received by the master in response to a data write transfer. If the I2CNACKENI bit in I2CxMCTL is set, an interrupt is generated when the I2CMNA bit is set. This bit is cleared in all other conditions.
6	I2CMBUSY	I²C master busy status bit. Set to 1 when the master is busy processing a transaction. Cleared if the master is ready or if another master device has control of the bus.
5	I2CAL	I²C arbitration lost status bit. This bit is set to 1 when the I²C master is unsuccessful in gaining control of the I²C bus. If the I2CALENI bit in I2CxMCTL is set, an interrupt is generated when the I2CAL bit is set. This bit is cleared in all other conditions.
4	I2CMNA	I²C master no acknowledge address bit. This bit is set to 1 when a no acknowledge condition is received by the master in response to an address. If the I2CNACKENI bit in I2CxMCTL is set, an interrupt is generated when the I2CMNA bit is set. This bit is cleared in all other conditions.
3	I2CMRXQ	I²C master receive request bit. This bit is set to 1 when data enters the Rx FIFO. If the I2CMRENI in I2CxMCTL is set, an interrupt is generated. This bit is cleared in all other conditions.
2	I2CMTXQ	I²C master transmit request bit. This bit goes high if the transmitter (Tx) FIFO is empty or only contains one byte and the master has transmitted an address plus write. If the I2CMTENI bit in I2CxMCTL is set, an interrupt is generated when the I2CMTXQ bit is set. This bit is cleared in all other conditions.
[1:0]	I2CMTFSTA	I²C master Tx FIFO status bits. 00 = I²C master Tx FIFO empty. 01 = one byte in master Tx FIFO. 10 = one byte in master Tx FIFO. 11 = I²C master Tx FIFO full.

INTERRUPT SYSTEM

There are 27 interrupt on the ADuC7120/ADuC7121 that are controlled by the interrupt controller. All interrupts are generated from the on-chip peripherals, except for the software interrupt (SWI), which is programmable by the user. The ARM7TDMI CPU core recognizes interrupts as one of only two types: a normal interrupt request (IRQ) and a fast interrupt request (FIQ). All the interrupts can be masked separately.

The control and configuration of the interrupt system is managed through a number of interrupt related registers. The bits in each IRQ and FIQ register represent the same interrupt source as described in Table 116.

The ADuC7120/ADuC7121 contain a vectored interrupt controller (VIC) that supports nested interrupts up to eight levels. The VIC also allows the programmer to assign priority levels to all interrupt sources. Set the ENIRQN bit in the IRQCONN register to enable interrupt nesting. When the full vectored interrupt controller is enabled, extra MMRs are used.

Upon entering the ISR, immediately save the IRQSTA and the FIQSTA registers to service all valid interrupt sources are serviced.

NORMAL INTERRUPT REQUEST (IRQ)

The normal interrupt request (IRQ) is the exception signal to enter the IRQ mode of the processor. It services general-purpose interrupt handling of internal and external events.

All 32 bits are logically OR'ed to create a single IRQ signal to the ARM7TDMI core. The four 32-bit registers dedicated to IRQ follow.

Table 116. IRQ/FIQ MMRs Bit Designations

Bit	Description	Comments
0	All interrupts OR'ed (FIQ only)	This bit is set if any FIQ is active
1	Software interrupt	User-programmable interrupt source
2	Timer0	General-Purpose Timer0
3	Timer1	General-Purpose Timer1
4	Timer2 or wake-up timer	General-Purpose Timer2 or wake-up timer
5	Timer3 or watchdog timer	General-Purpose Timer3 or watchdog timer
6	Timer4	General-Purpose Timer4
7	IDAC fault	IDAC fault IRQ
8	PSM	Power supply monitor
9	Undefined	This bit is not used
10	Flash Control 0	Flash controller for Block 0 interrupt
11	Flash Control 1	Flash controller for Block 1 interrupt
12	ADC	ADC interrupt source bit
13	UART	UART interrupt source bit
14	SPI	SPI interrupt source bit
15	I^2C0 master IRQ	I^2C Master Interrupt Source 0 bit
16	I^2C0 slave IRQ	I^2C Slave Interrupt Source 0 bit
17	I^2C1 master IRQ	I^2C Master Interrupt Source 1 bit
18	I^2C1 slave IRQ	I^2C Slave Interrupt Source 1 bit
19	XIRQ0 (GPIO IRQ0)	External Interrupt 0
20	XIRQ1 (GPIO IRQ1)	External Interrupt 1
21	XIRQ2 (GPIO IRQ2)	External Interrupt 2
22	XIRQ3 (GPIO IRQ3)	External Interrupt 3
23	PWM	PWM trip interrupt source bit
24	XIRQ4 (GPIO IRQ4)	External Interrupt 4
25	XIRQ5 (GPIO IRQ5)	External Interrupt 5
26	PLA IRQ0	PLA Block 0 IRQ bit
27	PLA IRQ1	PLA Block 1 IRQ bit

IRQP1 Register

Name: IRQP1

Address: 0xFFFF0024

Default value: 0x00000000

Access: Read and write

Table 121. IRQP1 MMR Bit Designations

Bit(s)	Name	Description
31	Reserved	Reserved bit.
[30:28]	I2C0MPI	A priority level of 0 to 7 can be set for I²C 0 master.
27	Reserved	Reserved bit.
[26:24]	SPIPI	A priority level of 0 to 7 can be set for SPI.
23	Reserved	Reserved bit.
[22:20]	UARTPI	A priority level of 0 to 7 can be set for UART.
19	Reserved	Reserved bit.
[18:16]	ADCPI	A priority level of 0 to 7 can be set for the ADC interrupt source.
15	Reserved	Reserved bit.
[14:12]	Flash1PI	A priority level of 0 to 7 can be set for the Flash Block 1 controller interrupt source.
11	Reserved	Reserved bit.
[10:8]	Flash0PI	A priority level of 0 to 7 can be set for the Flash Block 0 controller interrupt source.
[7:3]	Reserved	Reserved bits.
[2:0]	PSMPI	A priority level of 0 to 7 can be set for the power supply monitor interrupt source.

IRQP2 Register

Name: IRQP2

Address: 0xFFFF0028

Default value: 0x00000000

Access: Read and write

Table 122. IRQP2 MMR Bit Designations

Bit(s)	Name	Description
31	Reserved	Reserved bit.
[30:28]	PWMPI	A priority level of 0 to 7 can be set for PWM.
27	Reserved	Reserved bit.
[26:24]	IRQ3PI	A priority level of 0 to 7 can be set for IRQ3.
23	Reserved	Reserved bit.
[22:20]	IRQ2PI	A priority level of 0 to 7 can be set for IRQ2.
19	Reserved	Reserved bit.
[18:16]	IRQ1PI	A priority level of 0 to 7 can be set for IRQ1.
15	Reserved	Reserved bit.
[14:12]	IRQ0PI	A priority level of 0 to 7 can be set for IRQ0.
11	Reserved	Reserved bit.
[10:8]	I2C1SPI	A priority level of 0 to 7 can be set for I²C1 slave.
7	Reserved	Reserved bit.
[6:4]	I2C1MPI	A priority level of 0 to 7 can be set for I²C1 master.
3	Reserved	Reserved bit.
[2:0]	I2C0SPI	A priority level of 0 to 7 can be set for I²C0 slave.

IRQP3 Register

Name: IRQP3

Address: 0xFFFF002C

Default value: 0x00000000

Access: Read and write

IRQP3 MMR Bit Designations

Bit(s)	Name	Description
[31:15]	Reserved	Reserved bit.
[14:12]	PLA1PI	A priority level of 0 to 7 can be set for PLA0.
11	Reserved	Reserved bit.
[10:8]	PLA0PI	A priority level of 0 to 7 can be set for PLA0.
7	Reserved	Reserved bit.
[6:4]	IRQ5PI	A priority level of 0 to 7 can be set for IRQ5.
3	Reserved	Reserved bit.
[2:0]	IRQ4PI	A priority level of 0 to 7 can be set for IRQ4.

IRQCONN Register

The IRQCONN register is the IRQ and FIQ control register. It contains two active bits. The first to enable nesting and prioritization of IRQ interrupts the other to enable nesting and prioritization of FIQ interrupts.

If these bits are cleared, FIQs and IRQs can still be used, but it is not possible to nest IRQs or FIQs, nor is it possible to set an interrupt source priority level. In this default state, an FIQ does have a higher priority than an IRQ.

Name: IRQCONN

Address: 0xFFFF0030

Default value: 0x00000000

Access: Read and write

Table 123. IRQCONN MMR Bit Designations

Bit(s)	Name	Description
[31:2]	Reserved	These bits are reserved and must not be written to.
1	ENFIQN	Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.
0	ENIRQN	Setting this bit to 1 enables nesting of IRQ interrupts. Clearing this bit means no nesting or prioritization of IRQs is allowed.

Timer3 Clear Register

This 8-bit, write only MMR is written (with any value) by user code to refresh (reload) Timer3 in watchdog mode to prevent a watchdog timer reset event.

Name: T3CLRI

Address: 0xFFFF036C

Default value: 0x0000

Access: Write only

Timer3 Control Register

The 16-bit MMR configures the mode of operation of Timer3 and is described in detail in Table 138.

Name: T3CON

Address: 0xFFFF0368

Default value: 0x0000

Access: Read and write one time only

Table 138. T3CON MMR Bit Designations

Bit(s)	Setting	Description
[15:9]		These bits are reserved and should be written as 0s by user code.
8		Count up/down enable. Set by user code to configure Timer3 to count up. Cleared by user code to configure Timer3 to count down.
7		Timer3 enable. Set by user code to enable Timer3. Cleared by user code to disable Timer3.
6		Timer3 operating mode. Set by user code to configure Timer3 to operate in periodic mode. Cleared by user to configure Timer3 to operate in free running mode.
5		Watchdog timer mode enable. Set by user code to enable watchdog mode. Cleared by user code to disable watchdog mode.
4		Secure clear bit. Set by the user to use the secure clear option. Cleared by the user to disable the secure clear option by default.
[3:2]		Timer3 Clock (32.768 kHz) prescaler.
	00	Source clock divide by 1 (default).
	01	Reserved.
	10	Reserved.
	11	Reserved.
1		Watchdog timer IRQ enable. Set by user code to produce an IRQ instead of a reset when the watchdog reaches 0. Cleared by user code to disable the IRQ option.
0		Power-down off (PD_OFF). Set by user code to stop Timer3 when the peripherals are powered down via Bit 4 in the POWCON MMR. Cleared by user code to enable Timer3 when the peripherals are powered down via Bit 4 in the POWCON MMR.

TIMER4—GENERAL-PURPOSE TIMER

Timer4 is a 32-bit general-purpose timer, count down or count up, with a programmable prescaler. The prescaler source can be the 32 kHz oscillator, the core clock, or PLL undivided output. This source can be scaled by a factor of 1, 16, 256, or 32,768, which gives a minimum resolution of 42 ns when operating at CD zero, and the core operates at 41.78 MHz with a prescaler of 1 (ignoring external GPIO).

The counter can be formatted as a standard 32-bit value or as hours: minutes: seconds: hundredths.

Timer4 has a capture register (T4CAP) that can be triggered by a selected source initial assertion of the IRQ. Once triggered, the current timer value is copied to T4CAP, and the timer continues running. This feature can determine the assertion of an event with increased accuracy.

The Timer4 interface consists of the following five MMRS:

- T4LD, T4VAL, and T4CAP are 32-bit registers and hold 32-bit unsigned integers; T4VAL and T4CAP are read only.
- T4ICLR is an 8-bit register. Writing any value to this register clears the Timer1 interrupt.
- T4CON is the configuration MMR.

If the devices are in low power mode, and Timer4 is clocked from the GPIO or oscillator source, Timer4 continues to operate.

Timer4 reloads the value from T4LD either when Timer4 overflows or immediately when T4ICLR is written.

Timer4 Load Registers

T4LD is a 32-bit register that holds the 32-bit value that loads into the counter.

Name: T4LD

Address: 0xFFFF0380

Default value: 0x00000000

Access: Read and write

Timer4 Clear Register

This 8-bit, write only MMR is written (with any value) by user code to refresh (reload) Timer4.

Name: T4CLRI

Address: 0xFFFF038C

Default value: 0x00

Access: Write only

Timer4 Value Register

T4VAL is a 32-bit register that holds the current value of Timer4.

Name: T4VAL

Address: 0xFFFF0384

Default value: 0x00000000

Access: Read only

Timer4 Capture Register

This is a 32-bit register that holds the 32-bit value captured by an enabled IRQ event.

Name: T4CAP

Address: 0xFFFF0390

Default value: 0x00000000

Access: Read only

Timer4 Control Register

This 32-bit MMR configures the mode of operation of Timer4.

Name: T4CON

Address: 0xFFFF0388

Default value: 0x0000

Access: Read and write

Table 139. T4CON MMR Bit Designations

Bit(s)	Setting	Description
[31:18]		Reserved. Set by the user to 0.
17		Event select bit. Set by the user to enable time capture of an event. Cleared by the user to disable time capture of an event.
[16:12]		Event select range, 0 to 31. The events are described in the Timers section.

In these three scenarios, and in more complicated real-life applications, pay particular attention to the flow of current from the supplies and back to ground. Ensure that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. For example, do not power components on the analog side, as shown in Figure 47, with IOVDD because that forces return currents from IOVDD to flow through AGND.

In addition, avoid digital currents flowing under analog circuitry, which can occur if a noisy digital chip is placed on the left half of the board, as shown in Figure 48. If possible, avoid large discontinuities in the ground plane(s) (such as those formed by a long trace on the same layer) because they force return signals to travel a longer path. In addition, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

When connecting fast logic signals (rise or fall times < 5 ns) to any of the ADuC7120/ADuC7121 digital inputs, add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the input pins of the devices. A resistor value of 100 Ω or 200 Ω is usually sufficient enough to prevent high speed signals from coupling capacitively into the devices and affecting the accuracy of ADC conversions.

CLOCK OSCILLATOR

An internal PLL or an external clock input can generate a clock source for the ADuC7120/ADuC7121. To use the internal PLL, connect a 32.768 kHz parallel resonant crystal between XTALI and XTALO and connect a capacitor from each pin to ground (see Figure 49). This crystal allows the PLL to lock correctly to give a frequency of 41.78 MHz. If no external crystal is present, the internal oscillator typically gives a frequency of 41.78 MHz ± 3%.

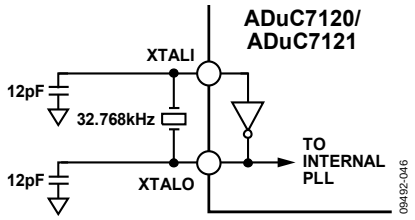

Figure 49. External Parallel Resonant Crystal Connections

To use an external clock source input instead of the PLL (see Figure 50), Bit 1 and Bit 0 of Register PLLCON must be modified. The external clock uses P1.4 and XCLK.

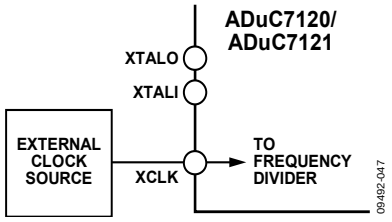

Figure 50. Connecting an External Clock Source

Using an external clock source, the ADuC7120/ADuC7121 specified operational clock speed range is 50 kHz to 41.78 MHz ± 1% to ensure correct operation of the analog peripherals and Flash/EE.

OUTLINE DIMENSIONS

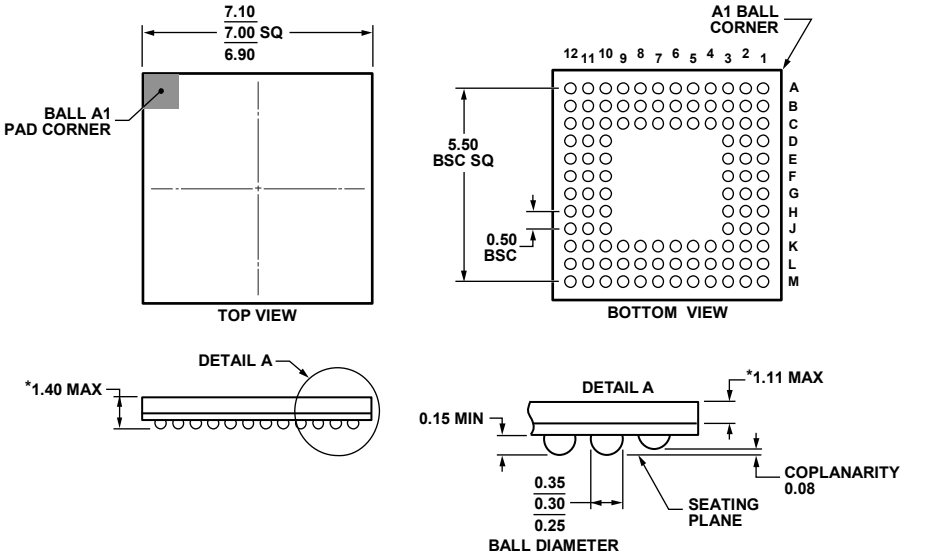

Figure 51. 108-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-108-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADuC7120BBCZ	−40°C to +105°C	108-Ball CSP_BGA	BC-108-4
ADuC7120BBCZ-RL	−40°C to +105°C	108-Ball CSP_BGA, 13″Tape and Reel	BC-108-4
ADuC7121BBCZ	−40°C to +105°C	108-Ball CSP_BGA	BC-108-4
ADuC7121BBCZ-RL	−40°C to +105°C	108-Ball CSP_BGA, 13″Tape and Reel	BC-108-4
EVAL-ADuC7120QSPZ		ADuC7120 QuickStart Development System	
EVAL-ADuC7121QSPZ		ADuC7121 QuickStart Development System	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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