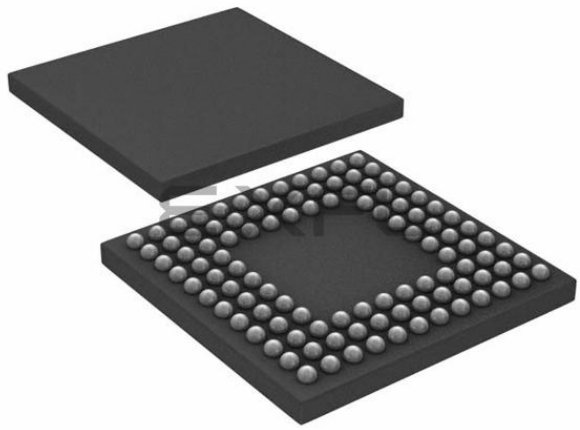

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 11x12b; D/A 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	108-LFBGA, CSPBGA
Supplier Device Package	108-CSPBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7120bbcz

SPECIFICATIONS

AVDD = IOVDD = 3.0 V to 3.6 V, PVDD_IDACx = 1.5 V to 2.1 V, reference voltage (V_{REF}) = 2.5 V internal reference, core frequency (f_{CORE}) = 41.78 MHz, ambient temperature (T_A) = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and ADC frequency (f_{ADC})/2
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity		±0.6	±2.2	LSB	
		±0.6	±2	LSB	−10°C to +95°C temperature range only
					2.5 V internal reference, not production tested for PADC0x and PADC1x channels
Differential Nonlinearity[3, 4]		±0.5	+1.4/−0.99	LSB	2.5 V internal reference, guaranteed monotonic
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[5]					Internally unbuffered channels
Offset Error					
All Channels Except IDACx Channels		±2	±5	LSB	
IDACx Channels Only		1		% of FS	
Offset Error Match		±1		LSB	
Gain Error		±2	±5.3	LSB	
		±2	±5	LSB	−10°C to +95°C temperature range only
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					Input frequency (f_{IN}) = 10 kHz sine wave, sample frequency (f_{SAMPLE}) = 1 MSPS, internally unbuffered channels
Signal-to-Noise Ratio (SNR)		69		dB	Includes distortion and noise components
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise		−75		dB	
Channel to Channel Crosstalk		−80		dB	Measured on adjacent channels
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode			V_{CM}[6] ± V_{REF}/2	V	See Table 42
Single-Ended Mode			0 to V_{REF}	V	Buffer bypassed
	0.15		AV_{DD} − 1.5	V	Buffer enabled
Leakage Current		±0.2	±1	µA	
Input Capacitance		20		pF	During ADC acquisition buffer bypassed
		20		pF	During ADC acquisition buffer enabled
PADC0x INPUT					28.3 kΩ resistor, PGA gain = 3, acquisition time = 3.2 µs, pseudo differential mode
Full-Scale Input Range	20		1000	µA	
Input Leakage at PADC0x[4]		0.15	2	nA	
Resolution	11			Bits	0.1% accuracy, 5 ppm external resistor for current to voltage
Gain Error[4]			1	%	
Gain Drift[4]			50	ppm/°C	
Offset[4]		3	6	nA	PGA offset not included
Offset Drift[4]		30	60	pA/°C	
PADC0x Compliant Range	0.1		AV_{DD} − 1.2	V	

Pin No.	Mnemonic	Type[1]	Description
C3	P0.2/SPICLK/ADC_{BUSY}/PLAO[13]	I/O	General-Purpose Input and Output Port 0.2 (P0.2). SPI Clock (SPICLK). Status of the ADC (ADC_{BUSY}). Programmable Logic Array for Output Element 13 (PLAO[13]).
C4	P3.0/PLAO[0]	I/O	General-Purpose Input and Output Port 3.0 (P3.0). Programmable Logic Array for Output Element 0 (PLAO[0]).
C5	PVDD_IDAC3	S	2.0 V Power for the IDAC3.
C6	PVDD_IDAC4	S	2.0 V Power for IDAC4.
C7	AVDD	S	Analog Supply (3.3 V).
C8	C_{DAMP}_IDAC2	AI	Damping Capacitor Pin for IDAC2.
C9	P2.7/PLAI[0]	I/O	General-Purpose Input and Output Port 2.7 (P2.7). Programmable Logic Array for Input Element 0 (PLAI[0]).
C10	P1.2/TDI/PLAO[15]	DI	General-Purpose Input and Output Port 1.2 (P1.2). JTAG Test Port Input, Test Data In (TDI). The TDI function of Pin C10 is for debug and download access. Programmable Logic Array for Output Element 15 (PLAO[15]).
C11	P3.1/PLAO[1]	I/O	General-Purpose Input and Output Port 3.1 (P3.1). Programmable Logic Array for Output Element 1 (PLAO[1]).
C12	$\overline{RST}$	I	Reset Input (Active Low).
D1	P3.2/IRQ4/PWM3/PLAO[2]	I/O	General-Purpose Input and Output Port 3.2 (P3.2). External Interrupt Request 4, Active High (IRQ4). Pulse-Width Modulator 3 Output (PWM3). Programmable Logic Array for Output Element 2 (PLAO[2]).
D2	P1.1/SOUT/SDA1/PLAI[6]	I/O	General-Purpose Input and Output Port 1.1 (P1.1). Serial Output, Transmit Data, UART (SOUT). I^2C Interface Serial Data for I^2C1 (SDA1). Programmable Logic Array for Input Element 6 (PLAI[6]).
D3	P0.3/MISO/PLAO[12]/SYNC	I/O	General-Purpose Input and Output Port 0.3 (P0.3). SPI Master In Slave Out (MISO). Programmable Logic Array for Output Element 12 (PLAO[12]). Synchronous Reset (SYNC). Input to reset synchronously the PWM counters using an external source.
D10	P1.3/TDO/PLAO[14]	DO	General-Purpose Input and Output Port 1.3 (P1.3). JTAG Test Port Output, Test Data Out (TDO). The TDO function of Pin D10 is for debug and download access. Programmable Logic Array for Output Element 14 (PLAO[14]).
D11	P0.0/SCL0/PLAI[5]	I/O	General-Purpose Input and Output Port 0.0 (P0.0). I^2C Interface Serial Clock for I^2C0 (SCL0). Programmable Logic Array for Input Element 5 (PLAI[5]).
D12	P3.6/PLAO[10]	I/O	General-Purpose Input and Output Port 3.6 (P3.6). Programmable Logic Array for Output Element 10 (PLAO[10]).
E1	P3.3/IRQ5/PWM4/PLAO[3]	I/O	General-Purpose Input and Output Port 3.3 (P3.3). External Interrupt Request 5, Active High (IRQ5). Pulse-Width Modulator 4 Output (PWM4). Programmable Logic Array for Output Element 3 (PLAO[3]).
E2	P3.4/PLAO[8]	I/O	General-Purpose Input and Output Port 3.4 (P3.4). Programmable Logic Array for Output Element 8 (PLAO[8]).
E3	P0.4/MOSI/PLAI[11]/TRIP	I/O	General-Purpose Input and Output Port 0.4 (P0.4). SPI Master Out Slave In (MOSI). Programmable Logic Array for Input Element 11 (PLAI[11]). PWM Trip Interrupt (TRIP). The TRIP function of Pin E3 is the input that allows the PWM trip interrupt to be triggered.
E10	TMS	DI	JTAG Test Port Input, Test Mode Select. Debug and download access.

ARM REGISTERS

ARM7TDMI has a total of 37 registers: 31 general-purpose registers and 6 status registers. Each operating mode has dedicated banked registers.

When writing user level programs, 15 general-purpose 32-bit registers (R0 to R14), the program counter (R15), and the current program status register (CPSR) are usable. The remaining registers are used for system level programming and exception handling only.

When an exception occurs, some of the standard registers are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (R13) and the link register (R14) as represented in Figure 9. The fast interrupt mode has more registers (R8 to R12) for fast interrupt processing, which means that interrupt processing can begin without the need to save or restore these registers, thus saving critical time in the interrupt handling process.

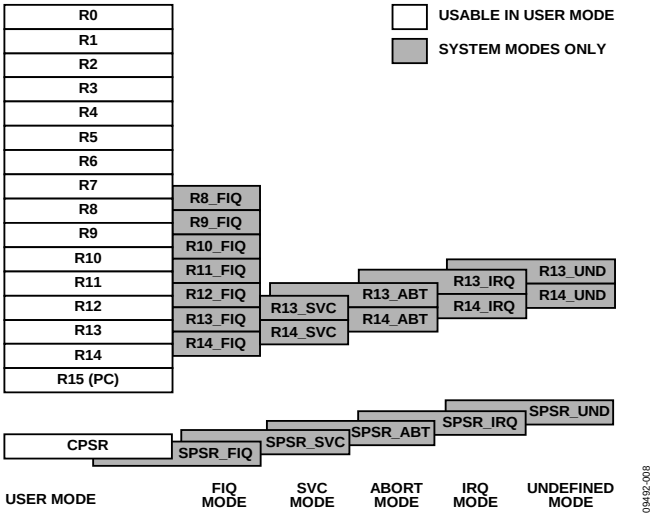

Figure 9. Register Organization

More information relative to the model of the programmer and the ARM7TDMI core architecture can be found in the following materials from ARM, Ltd.:

- ARM DDI 0029G, *ARM7TDMI Technical Reference Manual*
- ARM DDI 0100, *ARM Architecture Reference Manual*

INTERRUPT LATENCY

The worst case latency for a FIQ consists of the following:

- The longest time the request can take to pass through the synchronizer.
- The time for the longest instruction to complete (the longest instruction is a load multiple (LDM)) that loads all the registers including the PC.
- The time for the data abort entry.
- The time for FIQ entry.

At the end of this time, the ARM7TDMI executes the instruction at 0x1C (FIQ interrupt vector address). The maximum total time is 50 processor cycles, which is just under 1.2 µs in a system using a continuous 41.78 MHz processor clock.

The maximum IRQ latency calculation is similar but must allow the fact that FIQ has higher priority and can delay entry into the IRQ handling routine for an arbitrary length of time. This time can be reduced to 42 cycles if the LDM command is not used. Some compilers have an option to compile without using this command. Another option is to run the devices in thumb mode wherein the time is reduced to 22 cycles.

The minimum latency for FIQ or IRQ interrupts is five cycles, which consist of the shortest time the request can take through the synchronizer plus the time to enter the exception mode.

The ARM7TDMI always runs in ARM (32-bit) mode when in privileged modes, for example, when executing interrupt service routines.

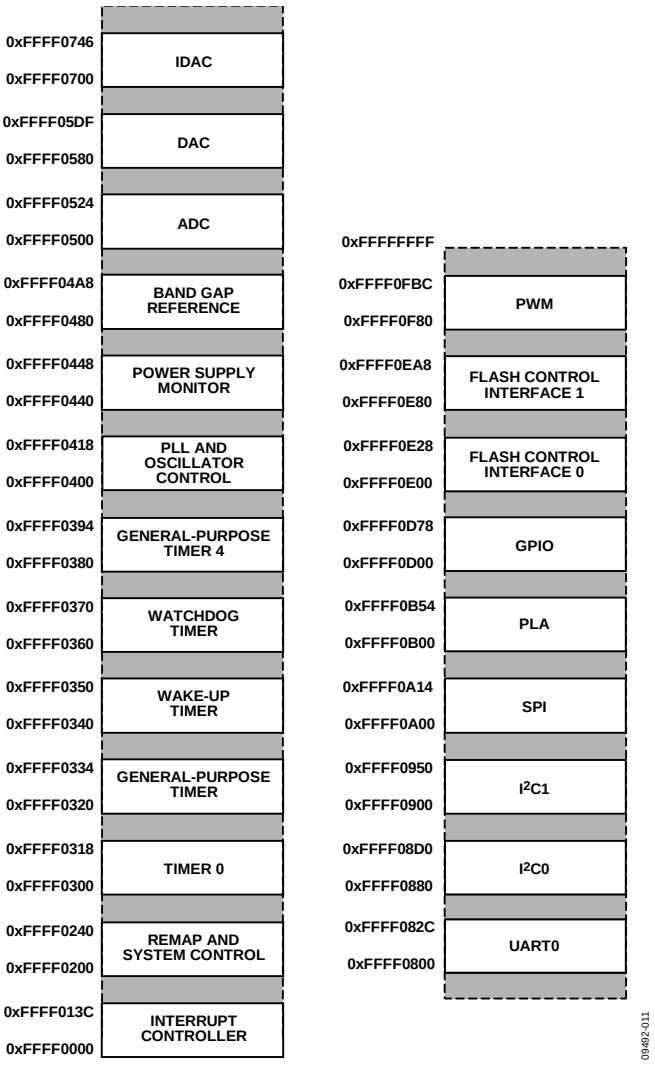

Figure 12. Memory Mapped Registers

COMPLETE MMR LISTING

The Access Type column corresponds to the access time reading or writing an MMR, where R is read, W is write, and R/W is read/write. It depends on the AMBA bus that accesses the peripheral. The processor has two AMBA buses: AHB used for system modules, and APB used for lower performance peripherals.

Table 12. IRQ Base Address = 0xFFFF0000

Address	Name	Byte	Access Type	Cycle
0x0000	IRQSTA	4	R	1
0x0004	IRQSIG	4	R	1
0x0008	IRQEN	4	R/W	1
0x000C	IRQCLR	4	W	1
0x0010	SWICFG	4	W	1
0x0014	IRQBASE	4	R/W	1
0x001C	IRQVEC	4	R/W	1
0x0020	IRQP0	4	R/W	1
0x0024	IRQP1	4	R/W	1
0x0028	IRQP2	4	R/W	1
0x002C	IRQP3	4	R/W	1
0x0030	IRQCONN	1	R/W	1
0x0034	IRQCONE	4	R/W	1
0x0038	IRQCLRE	1	W	1
0x003C	IRQSTAN	1	R/W	1
0x0100	FIQSTA	4	R	1
0x0104	FIQSIG	4	R	1
0x0108	FIQEN	4	R/W	1
0x010C	FIQCLR	4	W	1
0x011C	FIQVEC	4	R	1
0x013C	FIQSTAN	1	R/W	1

Table 13. Remap and System Control Base Address = 0xFFFF0200

Address	Name	Byte	Access Type	Cycle
0x0220	REMAP	1	R/W	1
0x0230	RSTSTA	1	R	1
0x0234	RSTCLR	1	W	1
0x0248	RSTCFGKEY0	1	W	1
0x024C	RSTCFG	1	R/W	1
0x0250	RSTCFGKEY1	1	W	1

Table 14. Timer Base Address = 0xFFFF0300

Address	Name	Byte	Access Type	Cycle
0x0300	T0LD	2	R/W	2
0x0304	T0VAL0	2	R	2
0x0308	T0VAL1	4	R	2
0x030C	T0CON	4	R/W	2
0x0310	T0CLRI	1	W	2
0x0314	T0CAP	2	R	2
0x0320	T1LD	4	R/W	2
0x0324	T1VAL	4	R	2
0x0328	T1CON	4	R/W	2
0x032C	T1CLRI	1	W	2
0x0330	T1CAP	4	R	2
0x0340	T2LD	4	R/W	2
0x0344	T2VAL	4	R	2
0x0348	T2CON	4	R/W	2
0x034C	T2CLRI	1	W	2
0x0360	T3LD	2	R/W	2
0x0364	T3VAL	2	R	2
0x0368	T3CON	2	R/W one time only	2
0x036C	T3CLRI	1	W	2
0x0380	T4LD	4	R/W	2
0x0384	T4VAL	4	R	2
0x0388	T4CON	4	R/W	2
0x038C	T4CLRI	1	W	2
0x0390	T4CAP	4	R	2

Table 15. PLL and Oscillator Control Base Address = 0xFFFF0400

Address	Name	Byte	Access Type	Cycle
0x0404	POWKEY1	2	W	2
0x0408	POWCON	1	R/W	2
0x040C	POWKEY2	2	W	2
0x0410	PLLKEY1	2	W	2
0x0414	PLLCON	1	R/W	2
0x0418	PLLKEY2	2	W	2

Table 16. PSM Base Address = 0xFFFF0440

Address	Name	Byte	Access Type	Cycle
0x0440	PSMCON	2	R/W	2

Table 17. Band Gap Reference Base Address = 0xFFFF0480

Address	Name	Byte	Access Type	Cycle
0x0480	REFCON	1	R/W	2

Table 18. ADC Base Address = 0xFFFF0500

Address	Name	Byte	Access Type	Cycle
0x0500	ADCCON	4	R/W	2
0x0504	ADCCP	1	R/W	2
0x0508	ADCCN	1	R/W	2
0x050C	ADCSTA	1	R	2
0x0510	ADCDAT	4	R	2
0x0514	ADCRST	1	W	2
0x0518	ADCGN	2	R/W	2
0x051C	ADCOF	2	R/W	2
0x0520	PGA_GN	2	R/W	2

Table 19. DAC Base Address = 0xFFFF0580

Address	Name	Byte	Access Type	Cycle
0x0580	DAC0CON	2	R/W	2
0x0584	DAC0DAT	4	R/W	2
0x0588	DAC1CON	2	R/W	2
0x058C	DAC1DAT	4	R/W	2
0x05B0	DAC2CON	2	R/W	2
0x05B4	DAC2DAT	4	R/W	2
0x05D8	DAC3CON	2	R/W	2
0x05DC	DAC3DAT	4	R/W	2

Table 20. IDAC Base Address = 0xFFFF0700

Address	Name	Byte	Access Type	Cycle
0x0700	IDAC0CON	2	R/W	2
0x0704	IDAC0DAT	4	R/W	2
0x0708	IDAC0BW	1	R/W	2
0x070C	IDAC1CON	2	R/W	2
0x0710	IDAC1DAT	4	R/W	2
0x0714	IDAC1BW	1	R/W	2
0x0718	IDAC2CON	2	R/W	2
0x071C	IDAC2DAT	4	R/W	2
0x0720	IDAC2BW	1	R/W	2
0x0724	IDAC3CON	2	R/W	2
0x0728	IDAC3DAT	4	R/W	2
0x072C	IDAC3BW	1	R/W	2
0x0730	IDAC4CON	2	R/W	2
0x0734	IDAC4DAT	4	R/W	2
0x0738	IDAC4BW	1	R/W	2
0x073C	TSDCON	1	R/W	2
0x0740	IDACSTA	1	R/W	2
0x0744	IDAC0PULLDOWN	1	R/W	2

Table 21. UART0 Base Address = 0xFFFF0800

Address	Name	Byte	Access Type	Cycle
0x0800	COMTX	1	W	2
	COMRX	1	R	2
	COMDIV0	1	R/W	2
0x0804	COMIEN0	1	R/W	2
	COMDIV1	1	R/W	2
0x0808	COMIID0	1	R	2
0x080C	COMCON0	1	R/W	2
0x0810	COMCON1	1	R/W	2
0x0814	COMSTA0	1	R	2
0X082C	COMDIV2	2	R/W	2

Table 22. I²C0 Base Address = 0xFFFF0880

Address	Name	Byte	Access Type	Cycle
0x0880	I2C0MCTL	2	R/W	2
0x0884	I2C0MSTA	2	R	2
0x0888	I2C0MRX	1	R	2
0x088C	I2C0MTX	2	W	2
0x0890	I2C0MCNT0	2	R/W	2
0x0894	I2C0MCNT1	1	R	2
0x0898	I2C0ADR0	1	R/W	2
0x089C	I2C0ADR1	1	R/W	2
0x08A0	I2C0SBYTE	1	R/W	2
0x08A4	I2C0DIV	2	R/W	2
0x08A8	I2C0SCTL	2	R/W	2
0x08AC	I2C0SSTA	2	R	2
0x08B0	I2C0SRX	1	R	2
0x08B4	I2C0STX	1	W	2
0x08B8	I2C0ALT	1	R/W	2
0x08BC	I2C0ID0	1	R/W	2
0x08C0	I2C0ID1	1	R/W	2
0x08C4	I2C0ID2	1	R/W	2
0x08C8	I2C0ID3	1	R/W	2
0x08CC	I2C0FSTA	1	R/W	2

Table 23. I²C1 Base Address = 0xFFFF0900

Address	Name	Byte	Access Type	Cycle
0x0900	I2C1MCTL	2	R/W	2
0x0904	I2C1MSTA	2	R	2
0x0908	I2C1MRX	1	R	2
0x090C	I2C1MTX	2	W	2
0x0910	I2C1MCNT0	2	R/W	2
0x0914	I2C1MCNT1	1	R	2
0x0918	I2C1ADR0	1	R/W	2
0x091C	I2C1ADR1	1	R/W	2
0x0920	I2C1SBYTE	1	R/W	2
0x0924	I2C1DIV	2	R/W	2
0x0928	I2C1SCTL	2	R/W	2
0x092C	I2C1SSTA	2	R	2
0x0930	I2C1SRX	1	R	2
0x0934	I2C1STX	1	W	2
0x0938	I2C1ALT	1	R/W	2
0x093C	I2C1ID0	1	R/W	2

Table 32. ADuC7120 ADCCP[1] MMR Bit Designations

Bit(s)	Setting	Description
[7:5]	Reserved	Reserved
[4:0]		Positive channel selection bits
	00000	PADC0P
	00001	PADC1P
	00010	ADC0
	00011	ADC1
	00100	ADC2
	00101	ADC3
	00110	ADC4
	00111	ADC5
	01000	ADC6
	01001	ADC7
	01010	ADC8
	01011	ADC9
	01100	ADC10/AINCM
	01101	Temperature sensor
	01110	DVDD_IDAC0
	01111	DVDD_IDAC1
	10000	DVDD_IDAC2
	10001	DVDD_IDAC3
	10010	DVDD_IDAC4
	10011	IOVDD_MON
	10100	PVDD_IDAC0
	10101	PVDD_IDAC1
	10110	V_{REF}
	10111	AGND
	Others	Reserved

[1] ADC channel availability depends on device model.

Table 33. ADuC7121 ADCCP[1] MMR Bit Designations

Bit(s)	Setting	Description
[7:5]	Reserved	Reserved
[4:0]		Positive channel selection bits
	00000	PADC0P
	00001	PADC1P
	00010	Reserved
	00011	Reserved
	00100	Reserved
	00101	Reserved
	00110	ADC4
	00111	ADC5
	01000	ADC6
	01001	ADC7
	01010	ADC8
	01011	ADC9
	01100	ADC10/AINCM
	01101	Temperature sensor
	01110	DVDD_IDAC0
	01111	DVDD_IDAC1
	10000	DVDD_IDAC2
	10001	DVDD_IDAC3
	10010	DVDD_IDAC4
	10011	IOVDD_MON
	10100	Reserved
	10101	Reserved
	10110	V_{REF}
	10111	AGND
	Others	Reserved

[1] ADC channel availability depends on device model.

Table 34. ADuC7120 ADCCN[1] MMR Bit Designations

Bit(s)	Setting	Description
[7:5]	Reserved	Reserved
[4:0]		Negative channel selection bits
	00000	PADC0N
	00001	PADC1N
	00010	ADC0
	00011	ADC1
	00100	ADC2
	00101	ADC3
	00110	ADC4
	00111	ADC5
	01000	ADC6
	01001	ADC7
	01010	ADC8
	01011	ADC9
	01100	ADC10/AINCM
	01101	V_{REF}
	01110	AGND
	01111	PGND
	10000	IOGND
	Others	Reserved

[1] ADC channel availability depends on device model.

Table 35. ADuC7121 ADCCN[1] MMR Bit Designations

Bit(s)	Setting	Description
[7:5]	Reserved	Reserved
[4:0]		Negative channel selection bits
	00000	PADC0N
	00001	PADC1N
	00010	Reserved
	00011	Reserved
	00100	Reserved
	00101	Reserved
	00110	ADC4
	00111	ADC5
	01000	ADC6
	01001	ADC7
	01010	ADC8
	01011	ADC9
	01100	ADC10/AINCM
	01101	V_{REF}
	01110	AGND
	01111	PGND
	10000	IOGND
	Others	Reserved

[1] ADC channel availability depends on device model.

Single-Ended Mode

In single-ended mode, SW2 is always connected internally to ground. The V_{IN-} input pin can be floating. The input signal range on V_{IN+} is 0 V to V_{REF}.

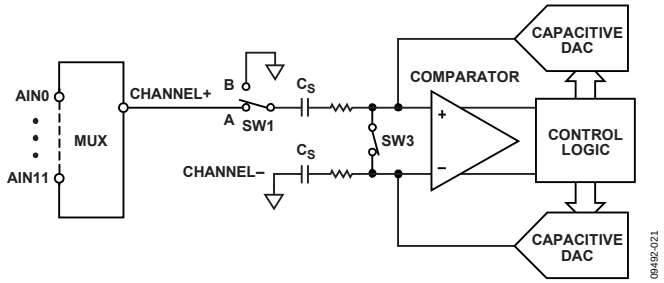

Figure 23. ADC in Single-Ended Mode

Analog Input Structure

Figure 24 shows the equivalent circuit of the analog input structure of the ADC. The four diodes provide ESD protection for the analog inputs. Ensure that the analog input signals never exceed the supply rails by more than 300 mV. Voltage in excess of 300 mV causes these diodes to become forward biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the device.

The C1 capacitors in Figure 24 are typically 4 pF and can be primarily attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors are the ADC sampling capacitors and have a capacitance of 16 pF typical.

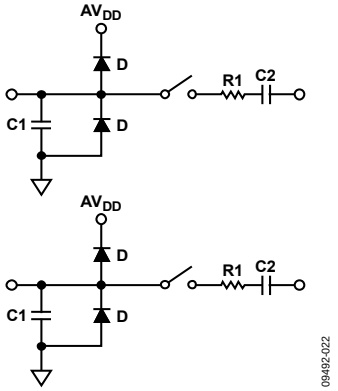

Figure 24. Equivalent Analog Input Circuit Conversion Phase: Switches Open, Track Phase: Switches Closed

For ac applications, removing high frequency components from the analog input signal is recommended with a resistor capacitor (RC) low-pass filter on the relevant analog input pins. In applications where harmonic distortion and SNR are critical, drive the analog input from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and can necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application. Figure 25 and Figure 26 give an example of an ADC front end.

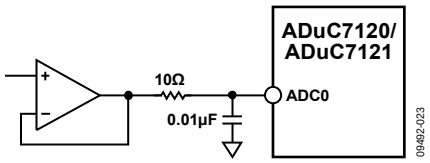

Figure 25. Buffering Single-Ended/Pseudo Differential Input

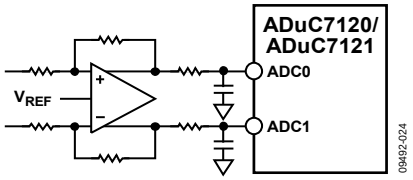

Figure 26. Buffering Differential Inputs

When no amplifier drives the analog input, limit the source impedance to values lower than 1 kΩ. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases and the performance degrades.

DRIVING THE ANALOG INPUTS

An internal or external reference can be used for the ADC. In differential mode of operation, there are restrictions on the V_{CM}. These restrictions are dependent on the reference value and supply voltage used to ensure the signal remains within the supply rails. Table 42 lists calculated V_{CM} minimum and V_{CM} maximum values.

Table 42. V_{CM} Ranges

AVDD (V)	V_{REF} (V)	V_{CM} (V)		Signal Peak-to-Peak (V)
		Min	Max	
3.3	2.5	1.25	2.05	2.5
	2.048	1.024	2.276	2.048
	1.25	0.75	2.55	1.25
3.0	2.5	1.25	1.75	2.5
	2.048	1.024	1.976	2.048
	1.25	0.75	2.25	1.25

POWER SUPPLY MONITOR (PSM)

The PSM on the ADuC7120/ADuC7121 indicates when the IOVDD supply pin drops below one of two supply trip points. The monitor function is controlled via the PSMCON register. If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit clears immediately after the CMP bit goes high. If the interrupt generated is exited before CMP goes high (IOVDD supply voltage is above the trip point), no further interrupts are generated until CMP returns high. The user must ensure that the code execution remains within the interrupt service routine (ISR) until CMP returns high.

This monitor function allows the user to save working registers to avoid possible data loss due to low supply or brownout conditions. It also ensures that normal code execution does not resume until a safe supply level is established.

The PSM does not operate correctly when using JTAG debug; therefore, disable PSM while in JTAG debug mode.

Table 44. PSMCON MMR Bit Designations (Address = 0xFFFF0440, Default Value = 0x0008)

Bit(s)	Name	Description
[15:4]	Reserved	These bits are reserved.
3	CMP	Comparator bit. This is a read only bit that directly reflects the state of the comparator. Read 1 indicates that the IOVDD supply is above its selected trip point or the PSM is in power-down mode. Read 0 indicates the IOVDD supply is below its selected trip point. Set this bit before leaving the interrupt service routine.
2	TP	Trip point selection bit. 0 = 2.79 V. 1 = 3.07 V.
1	PSMEN	Power supply monitor enable bit. Set to 1 to enable the power supply monitor circuit. Cleared to 0 to disable the power supply monitor circuit.
0	PSMI	Power supply monitor interrupt bit. This bit is set high by the MicroConverter if the CMP bit is low, indicating low input/output supply. The PSMI bit can interrupt the processor. When the CMP bit returns high, the PSMI bit can be cleared by writing a 1 to this location. Writing a 0 to this location has no effect. There is no timeout delay. PSMI can be cleared immediately after the CMP bit goes high.

NONVOLATILE FLASH/EE MEMORY

FLASH/EE MEMORY OVERVIEW

The ADuC7120/ADuC7121 incorporate Flash/EE memory technology on chip to provide the user with nonvolatile, in circuit reprogrammable memory space.

Similar to EEPROM, flash memory can be programmed in system at a byte level, although it must first be erased. The erase is performed in page blocks. As a result, flash memory is often (and more correctly) referred to as Flash/EE memory.

Overall, Flash/EE memory represents the ideal memory device that includes no volatility, in circuit programmability, high density, and low cost. Incorporated in the ADuC7120/ADuC7121, Flash/EE memory technology allows the user to update program code space in circuit, without the need to replace one time programmable (OTP) devices at remote operating nodes.

The ADuC7120/ADuC7121 contain two 64 kB arrays of Flash/EE memory. In Flash Block 0, the lower 62 kB is available to the user, and the upper 2 kB of this Flash/EE memory array program contain permanently embedded firmware, allowing in circuit serial download. The 2 kB of embedded firmware also contain a power-on configuration routine that downloads factory calibrated coefficients to the various calibrated peripherals (band gap references and so forth). This 2 kB embedded firmware is hidden from the user code. It is not possible for the user to read, write, or erase this page.

In Flash Block 1, all 64 kB of Flash/EE memory are available to the user.

The 128 kB of Flash/EE memory can be programmed in circuit using serial download mode or JTAG mode.

Flash/EE Memory Reliability

The Flash/EE memory arrays on the ADuC7120/ADuC7121 are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to cycle through many program, read, and erase cycles. A single endurance cycle is composed of four independent, sequential events, defined as follows:

1. Initial page erase sequence
2. Read and verify sequence a single Flash/EE
3. Byte program sequence memory
4. Second read and verify sequence endurance cycle

In reliability qualification, every half word (16-bit wide) location of the three pages (top, middle, and bottom) in the Flash/EE memory is cycled 10,000 times from 0x0000 to 0xFFFF.

As indicated in the Specifications section, the Flash/EE memory endurance qualification is carried out in accordance with JEDEC Retention Lifetime Specification, Method A117 over the industrial temperature range of −40°C to +105°C. The results allow the specification of a minimum endurance figure over a supply temperature of 10,000 cycles.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. The devices are qualified in accordance with the formal JEDEC Retention Lifetime Specification, Method A117 at a specific junction temperature (T_J = 85°C). As part of this qualification procedure, the Flash/EE memory is cycled to the specified endurance limit, previously described, before data retention is characterized. The Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time the Flash/EE memory is reprogrammed. Retention lifetime, based on activation energy of 0.6 eV, derates with T_J, as shown in Figure 27.

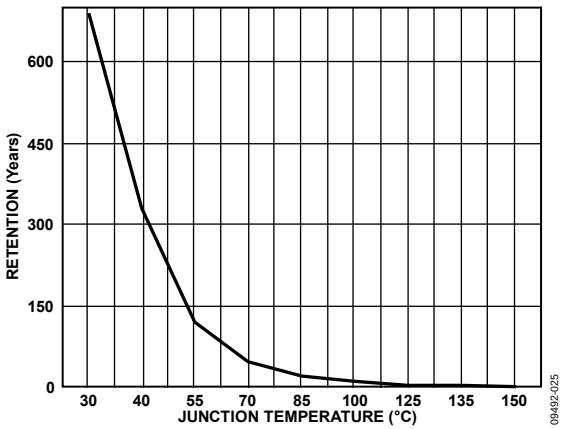

Figure 27. Flash/EE Memory Data Retention

Serial Downloading (In Circuit Programming)

The ADuC7120/ADuC7121 facilitate code download via the I²C serial port. If the $\overline{BM}$ function of the P3.7/$\overline{BM}$/PLAO[11] pin is pulled low through an external 1 kΩ resistor, the ADuC7120/ADuC7121 enter serial download mode after a reset or power cycle. In the Flash, if Address 0x0014 is 0xFFFFFFFF and $\overline{BM}$ is pulled low, the devices enter download mode; if this address contains any other value, user code is executed. When in serial download mode, the user can download code to the full 128 kB of Flash/EE memory while the devices are in circuit in their target application hardware. A PC serial download executable and hardware dongle are provided as part of the development system for serial downloads via the I²C port. The I²C maximum allowed baud rate is 100 kHz for the I²C downloader.

JTAG Access

The JTAG protocol uses the on-chip JTAG interface to facilitate code download and debug.

FLASH/EE MEMORY SECURITY

The 126 kB of Flash/EE memory available to the user can be read and write protected. Bit 31 of the FEE0PRO and FEE0HID MMRs protects it from read through by JTAG and I²C programming mode. The other 31 bits of this register protect writing to the Flash/EE memory; each bit protects four pages, that is, 2 kB. Write protection is activated for all access types. FEE1PRO and FEE1HID protect Flash Block 1. Bit 31 of the FEE1PRO and FEE1HID MMRs protects the 64 kB of Block 1 from being read through JTAG. Bit 30 protects writing to the top 8 pages of Block 1. The other 30 bits of this register protect writing to the Flash/EE memory; each bit protects four pages, that is, 2 kB.

Three Levels of Protection

Protection can be set and removed by writing directly into the FEExHID MMRs. This protection does not remain after reset.

Protection can be set by writing into the FEExPRO MMRs. It takes effect only after a save protection command (0x0C) and a reset. The FEExPRO MMRs are protected by a key to avoid direct access. The key is saved one time only and must be reentered to modify the FEExPRO. A mass erase sets the key back to 0xFFFF but also erases all user code.

The Flash/EE memory can be permanently protected by using the FEExPRO MMRs and a particular value of the 0xDEADDEAD key. Entering the key again to modify the FEExPRO register is not allowed.

Sequence to Write the Key to Protection Registers

1. Write the bit in the FEExPRO corresponding to the page to be protected.
2. Enable key protection by setting Bit 6 of FEExMOD (Bit 5 must equal 0).
3. Write a 32-bit key in FEExADR and FEExDAT.
4. Run the write key command 0x0C in FEExCON; wait for the read to be successful by monitoring FEExSTA.
5. Reset the device.

To remove or modify the protection, the same sequence is used with a modified value of FEExPRO. If the key chosen is the value 0xDEAD, the memory protection cannot be removed. Only a mass erase unprotects the device, but it also erases all user code.

The sequence to write the key is shown in the following example; this protects writing Page 4 to Page 7 of the Flash/EE memory:

```
FEE0PRO=0xFFFFFFFD;  //Protect Page 4 to Page 7
FEE0MOD=0x48;        //Write key enable
FEE0ADR=0x1234;      //16-bit key value
FEE0DAT=0x5678;      //16-bit key value
FEE0CON= 0x0C;       //Write key command
```

Follow the same sequence to permanently protect the devices with FEExADR = 0xDEAD and FEExDAT = 0xDEAD.

FLASH/EE CONTROL INTERFACE

FEE0DAT Register

FEE0DAT is a 16-bit data register.

Name: FEE0DAT

Address: 0xFFFF0E0C

Default value: 0xXXXX

Access: Read and write

FEE0ADR Register

FEE0ADR is a 16-bit address register.

Name: FEE0ADR

Address: 0xFFFF0E10

Default value: 0x0000

Access: Read and write

FEE0SGN Register

FEE0SGN is a 24-bit code signature.

Name: FEE0SGN

Address: 0xFFFF0E18

Default value: 0xFFFFFF

Access: Read only

FEE0PRO Register

FEE0PRO provides protection following subsequent reset MMR. It requires a software key (see Table 45).

Name: FEE0PRO

Address: 0xFFFF0E1C

Default value: 0x00000000

Access: Read and write

FEE0HID Register

FEE0HID provides immediate protection MMR. It does not require any software keys (see Table 45).

Name: FEE0HID

Address: 0xFFFF0E20

Default value: 0xFFFFFFFF

Access: Read and write

Bit(s)	Description
1	Command fail. Set automatically when a command completes unsuccessfully. Cleared automatically when reading FEExSTA register.
0	Command complete. Set by MicroConverter when a command is complete. Cleared automatically when reading FEExSTA register.

FEE0MOD Register

Name: FEE0MOD

Address: 0xFFFF0E04

Default value: 0x80

Access: Read and write

FEE1MOD Register

Name: FEE1MOD

Address: 0xFFFF0E84

Default value: 0x80

Access: Read and write

Table 48. FEExMOD MMR Bit Designations

Bit(s)	Description
[7:5]	Reserved. These bits are always set to 0 except when writing keys. See the Sequence to Write the Key to Protection Registers section for details.
4	Flash/EE interrupt enable. Set by the user to enable the Flash/EE interrupt. The interrupt occurs when a command is complete. Cleared by the user to disable the Flash/EE interrupt.
3	Erase/write command protection. Set by the user to enable the erase and write commands. Cleared to protect the Flash/EE memory against erase/write command.
2	Reserved. The user must set this bit to 0.
[1:0]	Flash/EE wait states. Both Flash/EE blocks must have the same wait state value for any change to take effect.

FEE0CON Register

Name: FEE0CON

Address: 0xFFFF0E08

Default value: 0x00

Access: Read and write

FEE1CON Register

Name: FEE1CON

Address: 0xFFFF0E88

Default value: 0x00

Access: Read and write

Table 49. Command Codes in FEExCON

Code	Command	Description
0x00[1]	Null	Idle state.
0x01[1]	Single read	Load FEExDAT with the 16-bit data indexed by FEExADR.
0x02[1]	Single write	Write FEExDAT at the address pointed by FEExADR. This operation takes 50 µs.
0x03[1]	Erase/write	Erase the page indexed by FEExADR and write FEExDAT at the location pointed by FEExADR. This operation takes 20 ms.
0x04[1]	Single verify	Compare the contents of the location pointed by FEExADR to the data in FEExDAT. The result of the comparison is returned in FEExSTA Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEExADR.
0x06[1]	Mass erase	Erase user space. The 2 kB of kernel are protected in Block 0. This operation takes 2.48 sec. To prevent accidental execution, a command sequence is required to execute this instruction.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	Gives a signature of the 64 kB of Flash/EE in the 24-bit FEExSIGN MMR. This operation takes 32,778 clock cycles.
0x0C	Protect	This command can run only once. The value of FEExPRO is saved and can be removed only with a mass erase (0x06) or with the key.
0x0D	Reserved	Reserved.
0x0E	Reserved	Reserved.
0x0F	Ping	No operation, interrupt generated.

[1] The FEExCON register always reads 0x07 immediately after execution of any of these commands.

GENERAL-PURPOSE INPUT/OUTPUT

The ADuC7120/ADuC7121 provide 32 general-purpose, bidirectional input/output (GPIO) pins. All input/output pins are 5 V tolerant, meaning that the GPIOs support an input voltage of 5 V. In general, many of the GPIO pins have multiple functions (see Table 81). By default, the GPIO pins are configured in GPIO mode.

All GPIO pins have an internal pull-up resistor (of about 100 kΩ) and their drive capability is 1.6 mA. A maximum of 20 GPIOs can drive 1.6 mA at the same time. The 32 GPIOs are grouped into four ports: Port 0 to Port 3. Each port is controlled by four or five MMRs, with x representing the port number.

GPxCON Registers

Name: GP0CON

Address: 0xFFFF0D00

Default value: 0x11000000

Access: Read and write

Name: GP1CON

Address: 0xFFFF0D04

Default value: 0x00000000

Access: Read and write

Name: GP2CON

Address: 0xFFFF0D08

Default value: 0x00000000

Access: Read and write

Name: GP3CON

Address: 0xFFFF0D0C

Default value: 0x00000000

Access: Read and write

The input level of any GPIO can be read at any time in the GPxDAT MMR, even when the pin is configured in a mode other than GPIO. The PLA input is always active.

When the ADuC7120/ADuC7121 enter power-saving mode, the GPIO pins retain their state.

GPxCON is the Port x control register, and it selects the function of each pin of Port x, as described in Table 81.

Table 81. GPIO Pin Function Designations

		Configuration (See Table 82 for the GPxCON MMR Bit Designations)			
Port	**Pin**	**00**	**01**	**10**	**11**
0	P0.0	GPIO	SCL0		PLAI[5]
	P0.1	GPIO	SDA0	JTAG disabled	PLAI[4]
	P0.2	GPIO	SPICLK	JTAG disabled ADC_{BUSY}	PLAO[13]
	P0.3	GPIO	MISO	SYNC (PWM)	PLAO[12]
	P0.4	GPIO	MOSI	TRIP (PWM)	PLAI[11]
	P0.5	GPIO	$\overline{CS}$	$ADC_{\overline{CONVST}}$	PLAI[10]
	P0.6	GPIO	$\overline{MRST}$		PLAI[2]
	P0.7	GPIO	$\overline{TRST}$		PLAI[3]
1	P1.0	GPIO	SIN	SCL1	PLAI[7]
	P1.1	GPIO	SOUT	SDA1	PLAI[6]
	P1.2[1]	TDI (JTAG)			PLAO[15]
	P1.3[1]	TDO (JTAG)			PLAO[14]
	P1.4	GPIO	PWM1	ECLK/XCLK	PLAI[8]
	P1.5	GPIO	PWM2		PLAI[9]
	P1.6	GPIO			PLAO[5]
	P1.7	GPIO			PLAO[4]

I²C Master Clock Control Register

This MMR controls the frequency of the I²C clock generated by the master on to the SCLx pin.

Name: I2C0DIV, I2C1DIV

Address: 0xFFFF08A4, 0xFFFF0924

Default value: 0x1F1F

Access: Read and write

Table 101. I2CxDIV MMR

Bit(s)	Name	Description
[15:8]	DIVH	These bits control the duration of the high period of SCLx.
[7:0]	DIVL	These bits control the duration of the low period of SCLx.

I²C Slave Registers

I²C Slave Control Register

This 16-bit MMR configures the I²C peripheral in slave mode.

Name: I2C0SCTL, I2C1SCTL

Address: 0xFFFF08A8, 0xFFFF0928

Default value: 0x0000

Access: Read and write

Table 102. I2CxSCTL MMR Bit Designations

Bit(s)	Name	Description
[15:11]		Reserved bits.
10	I2CSTXENI	Slave transmit interrupt enable bit. Set this bit to enable an interrupt after a slave transmits a byte. Clear this interrupt source.
9	I2CSRXENI	Slave receive interrupt enable bit. Set this bit to enable an interrupt after the slave receives data. Clear this interrupt source.
8	I2CSSENI	I²C stop condition detected interrupt enable bit. Set this bit to enable an interrupt on detecting a stop condition on the I²C bus. Clear this interrupt source.
7	I2CNACKEN	I²C no acknowledge enable bit. Set this bit to no acknowledge the next byte in the transmission sequence. Clear this bit to let the hardware control the acknowledge/no acknowledge sequence.
6		Reserved. A value of 0 should be written to this bit.
5	I2CSETEN	I²C early transmit interrupt enable bit. Setting this bit enables a transmit request interrupt just after the positive edge of SCLx during the read bit transmission. Clear this bit to enable a transmit request interrupt just after the negative edge of SCLx during the read bit transmission.
4	I2CGCCLR	I²C general call status and ID clear bit. Writing a 1 to this bit clears the general call status and ID bits in the I2CxSSTA register. Clear this bit at all other times.
3	I2CHGCEN	I²C hardware general call enable. Hardware general call enable. When this bit and Bit 2 are set, and having received a general call (Address 0x00) and a data byte, the device checks the contents of the I2CxALT register against the receive register. If the contents match, the device has received a hardware general call. This is used if a device needs urgent attention from a master device without knowing which master it needs to turn to. This is a to whom it may concern call. The ADuC7120/ADuC7121 watch for these addresses. The device that requires attention embeds its own address into the message. All masters listen, and the one that can handle the device contacts its slave and acts appropriately. The LSB of the I2CxALT register must always be written to 1, as per the I²C January 2000 Bus Specification. Set this bit and I2CGCEN to enable hardware general call recognition in slave mode. Clear to disable recognition of hardware general call commands.

SERIAL PERIPHERAL INTERFACE

The ADuC7120/ADuC7121 integrate a complete hardware serial peripheral interface (SPI) on-chip. SPI is an industry standard, synchronous serial interface that allows eight bits of data to synchronously transmit and simultaneously receive, that is, full duplex up to a maximum bit rate of 20 Mbps.

The SPI port can be configured for master or slave operation and typically consists of four pins: P0.3/MISO/PLAO[12]/SYNC, P0.4/MOSI/PLAI[11]/TRIP, P0.2/SPICLK/ADC_{BUSY}/PLAO[13], and P0.5/$\overline{CS}$/PLAI[10]/$ADC_{\overline{CONVST}}$.

SPI MASTER IN, SLAVE OUT (MISO) PIN

MISO on the P0.3/MISO/PLAO[12]/SYNC pin is configured as an input line in master mode and an output line in slave mode. Connect the MISO line on the master (data in) to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

SPI MASTER OUT, SLAVE IN (MOSI) PIN

MOSI on the P0.4/MOSI/PLAI[11]/TRIP pin is configured as an output line in master mode and an input line in slave mode. Connect the MOSI line on the master (data out) to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SERIAL CLOCK INPUT/OUTPUT (SPICLK) PIN

The master serial clock (SPICLK) synchronizes the data transmitted and received through the MOSI SPICLK period. Therefore, a byte is transmitted/received after eight SPICLK periods. The P0.2/SPICLK/ADC_{BUSY}/PLAO[13] pin is configured as an output in master mode and as an input in slave mode.

In master mode, the polarity and phase of the clock are controlled by the SPICON register, and the bit rate is defined in the SPIDIV register as follows:

$$f_{SERIAL\ CLOCK} = (f_{UCLK}/(2 \times (1 + SPIDIV))$$

The maximum speed of the SPI clock is independent on the clock divider bits.

In slave mode, the SPICON register must be configured with the phase and polarity of the expected input clock. The slave accepts data from an external master up to 10 Mbps.

In both master and slave modes, data is transmitted on one edge of the SPICLK signal and sampled on the other. Therefore, it is important that the polarity and phase are configured the same for the master and slave devices.

SPI CHIP SELECT INPUT PIN

In SPI slave mode, a transfer is initiated by the assertion of $\overline{CS}$ on the P0.5/$\overline{CS}$/PLAI[10]/$ADC_{\overline{CONVST}}$ pin. $\overline{CS}$ is an active low input signal. The SPI port then transmits and receives 8-bit data until the transfer is concluded by deassertion of $\overline{CS}$. In slave mode, $\overline{CS}$ is always an input.

In SPI master mode, $\overline{CS}$ is an active low output signal. It asserts itself automatically at the beginning of a transfer and deasserts itself upon completion.

CONFIGURING EXTERNAL PINS FOR SPI FUNCTIONALITY

The SPI pins of the ADuC7120/ADuC7121 are P0.2 to P0.5.

- P0.5/$\overline{CS}$/PLAI[10]/$ADC_{\overline{CONVST}}$ is the slave chip select pin. In slave mode, this pin is an input and must be driven low by the master. In master mode, this pin is an output and goes low at the beginning of a transfer and high at the end of a transfer.
- P0.2/SPICLK/ADC_{BUSY}/PLAO[13] is the SPICLK pin.
- P0.3/MISO/PLAO[12]/SYNC is the master in, slave out pin.
- P0.4/MOSI/PLAI[11]/TRIP is the master out, slave in pin.

To configure P0.2 to P0.5 for SPI mode, see the General-Purpose Input/Output section.

SPI REGISTERS

The following MMR registers control the SPI interface: SPISTA, SPIRX, SPITX, SPIDIV, and SPICON.

SPI Status Register

This 32-bit MMR contains the status of the SPI interface in both master and slave modes.

Name: SPISTA

Address: 0xFFFF0A00

Default value: 0x0000

Access: Read only

Table 105. SPISTA MMR Bit Designations

Bit(s)	Name	Description
[15:12]		Reserved bits.
11	SPIREX	SPI Rx FIFO excess bytes present. This bit is set when there are more bytes in the Rx FIFO than indicated in the SPIMDE bits in SPICON. This bit is cleared when the number of bytes in the FIFO is equal or less than the number in SPIMDE.

PLADOUT Register

PLADOUT is a data output MMR for PLA. This register is always updated.

Name: PLADOUT

Address: 0xFFFF0B50

Default value: 0x00000000

Access: Read only

Table 115. PLADOUT MMR Bit Descriptions

Bit(s)	Description
[31:16]	Reserved.
[15:0]	Output bit from Element 15 to Element 0.

PLALCK Register

PLALCK is a PLA lock option. Bit 0 is written only once. When set, it does not allow modifying any of the PLA MMRs, except PLADIN. A PLA tool is provided in the development system to easily configure the PLA.

Name: PLALCK

Address: 0xFFFF0B54

Default value: 0x00

Access: Write only

IRQSIG Register

IRQSIG reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits clear when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is a read only register. Do not use this register in an interrupt service routine for determining the source of an IRQ exception; use only IRQSTA for this purpose.

Name: IRQSIG

Address: 0xFFFF0004

Default value: 0x00000000

Access: Read only

IRQEN Register

IRQEN provides the value of the current enable mask. When a bit is set to 1, the corresponding source request is enabled to create an IRQ exception. When a bit is set to 0, the corresponding source request is disabled or masked, which does not create an IRQ exception. The IRQEN register cannot be used to disable an interrupt.

Name: IRQEN

Address: 0xFFFF0008

Default value: 0x00000000

Access: Read and write

IRQCLR Register

IRQCLR is a write only register that allows the IRQEN register to clear or mask an interrupt source. Each bit that is set to 1 clears the corresponding bit in the IRQEN register without affecting the remaining bits. A pair of registers, IRQEN and IRQCLR, allows independent manipulation of the enable mask without requiring an atomic read modify write.

Use this register to disable an interrupt source only when:

- The device is in the interrupt sources interrupt service routine.
- The peripheral is temporarily disabled by its own control register.

Do not use the IRQCLR to disable an IRQ source if that IRQ source has an interrupt pending or could have an interrupt pending.

Name: IRQCLR

Address: 0xFFFF000C

Default value: 0x00000000

Access: Write only

IRQSTA Register

IRQSTA is a read only register that provides the current enabled IRQ source status (effectively a logic AND of the IRQSIG and IRQEN bits). When set to 1, that source generates an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine.

Name: IRQSTA

Address: 0xFFFF0000

Default value: 0x00000000

Access: Read only

FAST INTERRUPT REQUEST (FIQ)

The fast interrupt request (FIQ) is the exception signal to enter the FIQ mode of the processor. It is provided to service data transfer or communication channel tasks with low latency. The FIQ interface is identical to the IRQ interface and provides the second level interrupt (highest priority). Four 32-bit registers are dedicated to FIQ: FIQSIG, FIQEN, FIQCLR, and FIQSTA.

Bit 31 to Bit 1 of FIQSTA are logically OR'ed to create the FIQ signal to the core and to Bit 0 of both the FIQ and IRQ registers (FIQ source).

The logic for FIQEN and FIQCLR does not allow an interrupt source to be enabled in both IRQ and FIQ masks. A bit set to 1 in FIQEN clears, as a side effect, the same bit in IRQEN. Likewise, a bit set to 1 in IRQEN clears, as a side effect, the same bit in FIQEN. An interrupt source can be disabled in both IRQEN and FIQEN masks.

FIQSIG Register

FIQSIG reflects the status of the different FIQ sources. If a peripheral generates an FIQ signal the corresponding bit in the FIQSIG is set; otherwise, it is cleared. The FIQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All FIQ sources can be masked in the FIQEN MMR. FIQSIG is read only.

Name: FIQSIG

Address: 0xFFFF0104

Default value: 0x00000000

Access: Read only

IRQP1 Register

Name: IRQP1

Address: 0xFFFF0024

Default value: 0x00000000

Access: Read and write

Table 121. IRQP1 MMR Bit Designations

Bit(s)	Name	Description
31	Reserved	Reserved bit.
[30:28]	I2C0MPI	A priority level of 0 to 7 can be set for I²C 0 master.
27	Reserved	Reserved bit.
[26:24]	SPIPI	A priority level of 0 to 7 can be set for SPI.
23	Reserved	Reserved bit.
[22:20]	UARTPI	A priority level of 0 to 7 can be set for UART.
19	Reserved	Reserved bit.
[18:16]	ADCPI	A priority level of 0 to 7 can be set for the ADC interrupt source.
15	Reserved	Reserved bit.
[14:12]	Flash1PI	A priority level of 0 to 7 can be set for the Flash Block 1 controller interrupt source.
11	Reserved	Reserved bit.
[10:8]	Flash0PI	A priority level of 0 to 7 can be set for the Flash Block 0 controller interrupt source.
[7:3]	Reserved	Reserved bits.
[2:0]	PSMPI	A priority level of 0 to 7 can be set for the power supply monitor interrupt source.

IRQP2 Register

Name: IRQP2

Address: 0xFFFF0028

Default value: 0x00000000

Access: Read and write

Table 122. IRQP2 MMR Bit Designations

Bit(s)	Name	Description
31	Reserved	Reserved bit.
[30:28]	PWMPI	A priority level of 0 to 7 can be set for PWM.
27	Reserved	Reserved bit.
[26:24]	IRQ3PI	A priority level of 0 to 7 can be set for IRQ3.
23	Reserved	Reserved bit.
[22:20]	IRQ2PI	A priority level of 0 to 7 can be set for IRQ2.
19	Reserved	Reserved bit.
[18:16]	IRQ1PI	A priority level of 0 to 7 can be set for IRQ1.
15	Reserved	Reserved bit.
[14:12]	IRQ0PI	A priority level of 0 to 7 can be set for IRQ0.
11	Reserved	Reserved bit.
[10:8]	I2C1SPI	A priority level of 0 to 7 can be set for I²C1 slave.
7	Reserved	Reserved bit.
[6:4]	I2C1MPI	A priority level of 0 to 7 can be set for I²C1 master.
3	Reserved	Reserved bit.
[2:0]	I2C0SPI	A priority level of 0 to 7 can be set for I²C0 slave.

IRQP3 Register

Name: IRQP3

Address: 0xFFFF002C

Default value: 0x00000000

Access: Read and write

IRQP3 MMR Bit Designations

Bit(s)	Name	Description
[31:15]	Reserved	Reserved bit.
[14:12]	PLA1PI	A priority level of 0 to 7 can be set for PLA0.
11	Reserved	Reserved bit.
[10:8]	PLA0PI	A priority level of 0 to 7 can be set for PLA0.
7	Reserved	Reserved bit.
[6:4]	IRQ5PI	A priority level of 0 to 7 can be set for IRQ5.
3	Reserved	Reserved bit.
[2:0]	IRQ4PI	A priority level of 0 to 7 can be set for IRQ4.

IRQCONN Register

The IRQCONN register is the IRQ and FIQ control register. It contains two active bits. The first to enable nesting and prioritization of IRQ interrupts the other to enable nesting and prioritization of FIQ interrupts.

If these bits are cleared, FIQs and IRQs can still be used, but it is not possible to nest IRQs or FIQs, nor is it possible to set an interrupt source priority level. In this default state, an FIQ does have a higher priority than an IRQ.

Name: IRQCONN

Address: 0xFFFF0030

Default value: 0x00000000

Access: Read and write

Table 123. IRQCONN MMR Bit Designations

Bit(s)	Name	Description
[31:2]	Reserved	These bits are reserved and must not be written to.
1	ENFIQN	Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.
0	ENIRQN	Setting this bit to 1 enables nesting of IRQ interrupts. Clearing this bit means no nesting or prioritization of IRQs is allowed.

Timer0 Value Registers

T0VAL0 and T0VAL1 are 16-bit and 32-bit registers that hold the 16 LSBs and 32 MSBs, respectively. T0VAL0 and T0VAL1 are read only registers. In 16-bit mode, 16-bit T0VAL0 is used. In 48-bit mode, both 16-bit T0VAL0 and 32-bit T0VAL1 are used.

Name: T0VAL0

Address: 0xFFFF0304

Default value: 0x0000

Access: Read only

Name: T0VAL1

Address: 0xFFFF0308

Default value: 0x00000000

Access: Read only

Timer0 Capture Register

This is a 16-bit register that holds the 16-bit value captured by an enabled IRQ event; available in 16-bit mode only.

Name: T0CAP

Address: 0xFFFF0314

Default value: 0x0000

Access: Read only

Timer0 Control Register

This 17-bit MMR configures the mode of operation of Timer0.

Name: T0CON

Address: 0xFFFF030C

Default value: 0x00000000

Access: Read and write

Table 132. T0CON MMR Bit Designations

Bit(s)	Setting	Description
[31:18]		Reserved.
17		Event select bit. Set by the user to enable time capture of an event. Cleared by the user to disable time capture of an event.
[16:12]		Event select range, 0 to 16. The events are described in the Timers section.
11		Reserved.
[10:9]		Clock select.
	00	Internal 32 kHz oscillator.
	01	UCLK.
	10	External 32 kHz crystal.
	11	HCLK.
8		Count up. Available in 16-bit mode only. Set by the user for Timer0 to count up. Cleared by the user for Timer0 to count down (default).
7		Timer0 enable bit. Set by the user to enable Timer0. Cleared by the user to disable Timer0 (default).
6		Timer0 mode. Set by the user to operate in periodic mode. Cleared by the user to operate in free running mode (default).
5		Reserved.
4		Timer0 mode of operation.
	0	16-bit operation (default).
	1	48-bit operation.
[3:0]		Prescaler.
	0000	Source clock divide by 1 (default).
	0100	Source clock divide by 16.
	1000	Source clock divide by 256.
	1111	Source clock divide by 32,768.

Timer0 Load Registers

T0LD is a 16-bit register that holds the 16-bit value that loads into the counter; available only in 16-bit mode.

Name: T0LD

Address: 0xFFFF0300

Default value: 0x00

Access: Read and write

Timer0 Clear Register

This 8-bit, write only MMR is written (with any value) by user code to refresh (reload) Timer0.

Name: T0CLRI

Address: 0xFFFF0310

Default value: 0x00

Access: Write only

HARDWARE DESIGN CONSIDERATIONS

POWER SUPPLIES

The ADuC7120/ADuC7121 operational power supply voltage range is 3.0 V to 3.6 V. Separate analog and digital power supply pins (AVDD and IOVDD, respectively) allow AVDD to be kept relatively free of noisy digital signals often present on the system IOVDD line. In this mode, the devices can also operate with split supplies, that is, using different voltage levels for each supply. For example, the system can operate with an IOVDD voltage level of 3.3 V while the AVDD level can be at 3 V, or vice versa. A typical split supply configuration is shown in Figure 42.

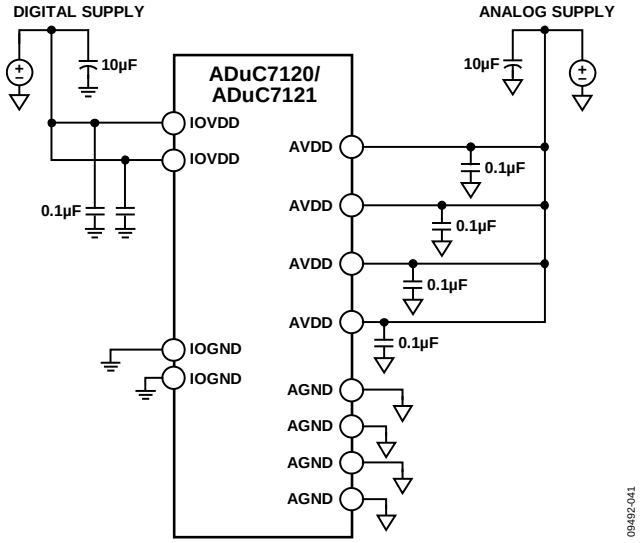

Figure 42. External Dual-Supply Connections

As an alternative to providing two separate power supplies, the user can reduce noise on AVDD by placing a small series resistor and/or ferrite bead between AVDD and IOVDD, and then decouple AVDD separately to ground. An example of this configuration is shown in Figure 43. With this configuration, other analog circuitry (such as op amps, voltage reference, and others) can be powered from the AVDD supply line as well.

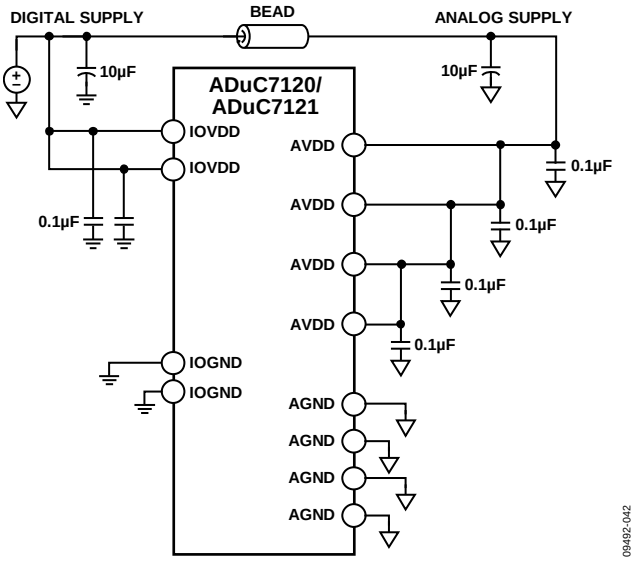

Figure 43. External Single Supply Connections

Notice that in both Figure 42 and Figure 43, a large value (10 µF) reservoir capacitor sits on IOVDD, and a separate 10 µF capacitor sits on AVDD. In addition, local small value (0.1 µF) capacitors are located at each AVDD and IOVDD pin of the chip. As per standard design practice, include all of these capacitors and ensure that the smaller capacitors are close to each AVDD pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. The analog and digital ground pins on the ADuC7120/ADuC7121 must be referenced to the same system ground reference point at all times.

IOVDD Supply Sensitivity

The IOVDD supply is sensitive to high frequency noise because it is the supply source for the internal oscillator and PLL circuits. When the internal PLL loses lock, the clock source is removed by a gating circuit from the CPU, and the ARM7TDMI core stops executing code until the PLL regains lock. This feature ensures that no flash interface timings or ARM7TDMI timings are violated.

Typically, frequency noise greater than 50 kHz and 50 mV p-p on top of the supply causes the core to stop working.

If decoupling values recommended in the Power Supplies section do not sufficiently dampen all noise sources below 50 mV on IOVDD, a filter such as the one shown in Figure 44 is recommended.

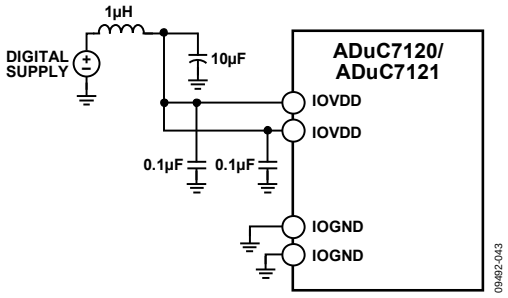

Figure 44. Recommended IOVDD Supply Filter

Linear Voltage Regulator

Each ADuC7120/ADuC7121 requires a single 3.3 V supply, but the core logic requires a 2.6 V supply. An on-chip linear regulator generates the 2.6 V from IOVDD for the core logic. The DVDD pins are the 2.6 V supply for the core logic. An external compensation capacitor of 0.47 µF must be connected between each DVDD and DGND (as close as possible to these pins) to act as a tank of charge as shown in Figure 45. The internal IDACs require a 2.5 V supply. An internal LDO provides a stable 2.5 V supply. The AVDD_IDAC pin is the 2.5 V supply for the IDACs. An external compensation capacitor of 0.47 µF must be connected between AVDD_IDAC and AGND (as close as possible to these pins) to act as a tank of charge as shown in Figure 45.

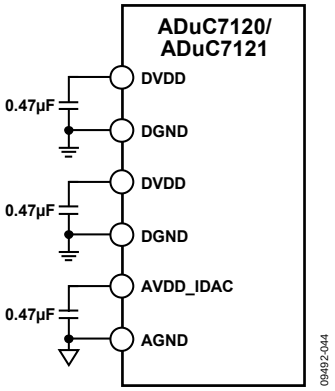

Figure 45. Voltage Regulator Connections

Do not use the DVDD pins for any other chip. It is also recommended to use excellent power supply decoupling on IOVDD to help improve line regulation performance of the on-chip voltage regulator.

GROUNDING AND BOARD LAYOUT RECOMMENDATIONS

As with all high resolution data converters, special attention must be paid to grounding and PCB layout of ADuC7120/ADuC7121-based designs to achieve optimum performance from the ADCs and DAC.

Although the devices have separate pins for analog and digital ground (AGND and IOGND), do not tie these to two separate ground planes unless the two ground planes are connected close to the device. A simplified example of this is shown in Figure 46.

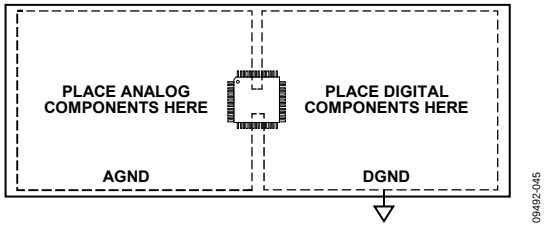

Figure 46. System Grounding Scheme Example of Two Ground Planes Connected Close to the Devices

In systems where digital and analog ground planes are connected together somewhere else (at the power supply of the system, for example), the planes can not be reconnected near the device because a ground loop can result. In these cases, tie all AGND and IOGND pins of the ADuC7120/ADuC7121 to the analog ground plane, as shown in Figure 47.

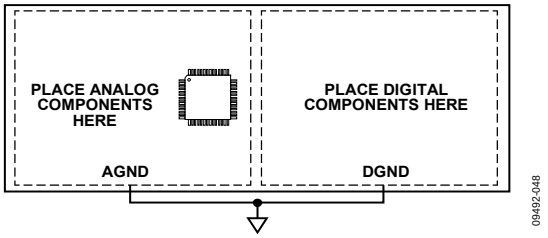

Figure 47. System Grounding Scheme Example of All AGND and IOGND Pins Tied to the Analog Ground Plane

In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board so digital return currents do not flow near analog circuitry and vice versa. The ADuC7120/ADuC7121 can then be placed between the digital and analog sections, as shown in Figure 48.

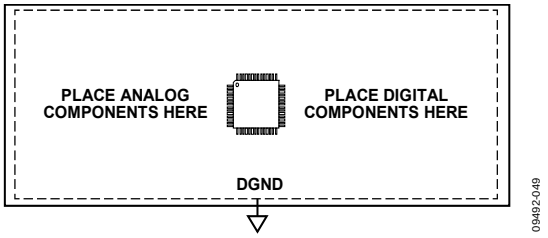

Figure 48. System Grounding Scheme Example of ADuC7120/ADuC7121 Placed Between the Digital and Analog Sections