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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	47
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3bu-au">https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3bu-au</a>

## 8. DMAC – Direct Memory Access Controller

### 8.1 Features

- Allows high speed data transfers with minimal CPU intervention
  - from data memory to data memory
  - from data memory to peripheral
  - from peripheral to data memory
  - from peripheral to peripheral
- Four DMA channels with separate
  - transfer triggers
  - interrupt vectors
  - addressing modes
- Programmable channel priority
- From 1 byte to 16MB of data in a single transaction
  - Up to 64KB block transfers with repeat
  - 1, 2, 4, or 8 byte burst transfers
- Multiple addressing modes
  - Static
  - Incremental
  - Decremental
- Optional reload of source and destination addresses at the end of each
  - Burst
  - Block
  - Transaction
- Optional interrupt on end of transaction
- Optional connection to CRC generator for CRC on DMA data

### 8.2 Overview

The four-channel direct memory access (DMA) controller can transfer data between memories and peripherals, and thus offload these tasks from the CPU. It enables high data transfer rates with minimum CPU intervention, and frees up CPU time. The four DMA channels enable up to four independent and parallel transfers.

The DMA controller can move data between SRAM and peripherals, between SRAM locations and directly between peripheral registers. With access to all peripherals, the DMA controller can handle automatic transfer of data to/from communication modules. The DMA controller can also read from memory mapped EEPROM.

Data transfers are done in continuous bursts of 1, 2, 4, or 8 bytes. They build block transfers of configurable size from 1 byte to 64KB. A repeat counter can be used to repeat each block transfer for single transactions up to 16MB. Source and destination addressing can be static, incremental or decremental. Automatic reload of source and/or destination addresses can be done after each burst or block transfer, or when a transaction is complete. Application software, peripherals, and events can trigger DMA transfers.

The four DMA channels have individual configuration and control settings. This include source, destination, transfer triggers, and transaction sizes. They have individual interrupt settings. Interrupt requests can be generated when a transaction is complete or when the DMA controller detects an error on a DMA channel.

To allow for continuous transfers, two channels can be interlinked so that the second takes over the transfer when the first is finished, and vice versa.

## 10. System Clock and Clock options

### 10.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal oscillators:
  - 32MHz run-time calibrated and tuneable oscillator
  - 2MHz run-time calibrated oscillator
  - 32.768kHz calibrated oscillator
  - 32kHz ultra low power (ULP) oscillator with 1kHz output
- External clock options
  - 0.4MHz - 16MHz crystal oscillator
  - 32.768kHz crystal oscillator
  - External clock
- PLL with 20MHz - 128MHz output frequency
  - Internal and external clock options and 1x to 31x multiplication
  - Lock detector
- Clock prescalers with 1x to 2048x division
- Fast peripheral clocks running at two and four times the CPU clock
- Automatic run-time calibration of internal oscillators
- External oscillator and PLL lock failure detection with optional non-maskable interrupt

### 10.2 Overview

Atmel AVR XMEGA A3BU devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

[Figure 10-1 on page 19](#) presents the principal clock system in the XMEGA A3BU family of devices. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in [“Power Management and Sleep Modes” on page 21](#)

## 23. TWI – Two-Wire Interface

### 23.1 Features

- Two Identical two-wire interface peripherals
- Bidirectional, two-wire communication interface
  - Phillips I<sup>2</sup>C compatible
  - System Management Bus (SMBus) compatible
- Bus master and slave operation supported
  - Slave operation
  - Single bus master operation
  - Bus master in multi-master bus environment
  - Multi-master arbitration
- Flexible slave address match functions
  - 7-bit and general call address recognition in hardware
  - 10-bit addressing supported
  - Address mask register for dual address match or address range masking
  - Optional software address recognition for unlimited number of addresses
- Slave can operate in all sleep modes, including power-down
- Slave address match can wake device from all sleep modes
- 100kHz and 400kHz bus frequency support
- Slew-rate limited output drivers
- Input filter for bus noise and spike suppression
- Support arbitration between start/repeated start and data bit (SMBus)
- Slave arbitration allows support for address resolve protocol (ARP) (SMBus)

### 23.2 Overview

The two-wire interface (TWI) is a bidirectional, two-wire communication interface. It is I<sup>2</sup>C and System Management Bus (SMBus) compatible. The only external hardware needed to implement the bus is one pull-up resistor on each bus line.

A device connected to the bus must act as a master or a slave. The master initiates a data transaction by addressing a slave on the bus and telling whether it wants to transmit or receive data. One bus can have many slaves and one or several masters that can take control of the bus. An arbitration process handles priority if more than one master tries to transmit data at the same time. Mechanisms for resolving bus contention are inherent in the protocol.

The TWI module supports master and slave functionality. The master and slave functionality are separated from each other, and can be enabled and configured separately. The master module supports multi-master bus operation and arbitration. It contains the baud rate generator. Both 100kHz and 400kHz bus frequency is supported. Quick command and smart mode can be enabled to auto-trigger operations and reduce software complexity.

The slave module implements 7-bit address match and general address call recognition in hardware. 10-bit addressing is also supported. A dedicated address mask register can act as a second address match register or as a register for address range masking. The slave continues to operate in all sleep modes, including power-down mode. This enables the slave to wake up the device from all sleep modes on TWI address match. It is possible to disable the address matching to let this be handled in software instead.

The TWI module will detect START and STOP conditions, bus collisions, and bus errors. Arbitration lost, errors, collision, and clock hold on the bus are also detected and indicated in separate status flags available in both master and slave modes.

It is possible to disable the TWI drivers in the device, and enable a four-wire digital interface for connecting to an external TWI bus driver. This can be used for applications where the device operates from a different V<sub>CC</sub> voltage than used by the TWI bus.

PORTC and PORTE each has one TWI. Notation of these peripherals are TWIC and TWIE.

## 29. ADC – 12-bit Analog to Digital Converter

### 29.1 Features

- Two Analog to Digital Converters (ADCs)
- 12-bit resolution
- Up to two million samples per second
  - Two inputs can be sampled simultaneously using ADC and 1x gain stage
  - Four inputs can be sampled within 1.5 $\mu$ s
  - Down to 2.5 $\mu$ s conversion time with 8-bit resolution
  - Down to 3.5 $\mu$ s conversion time with 12-bit resolution
- Differential and single-ended input
  - Up to 16 single-ended inputs
  - 16x4 differential inputs without gain
  - 8x4 differential input with gain
- Built-in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x gain options
- Single, continuous and scan conversion options
- Four internal inputs
  - Internal temperature sensor
  - DAC output
  - $AV_{CC}$  voltage divided by 10
  - 1.1V bandgap voltage
- Four conversion channels with individual input control and result registers
  - Enable four parallel configurations and results
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional DMA transfer of conversion results
- Optional interrupt/event on compare result

### 29.2 Overview

The ADC converts analog signals to digital values. The ADC has 12-bit resolution and is capable of converting up to two million samples per second (msps). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

This is a pipelined ADC that consists of several consecutive stages. The pipelined design allows a high sample rate at a low system clock frequency. It also means that a new input can be sampled and a new ADC conversion started while other ADC conversions are still ongoing. This removes dependencies between sample rate and propagation delay.

The ADC has four conversion channels (0-3) with individual input selection, result registers, and conversion start control. The ADC can then keep and use four parallel configurations and results, and this will ease use for applications with high data throughput or for multiple modules using the ADC independently. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The output from the DAC,  $AV_{CC}/10$  and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

## 30. DAC – 12-bit Digital to Analog Converter

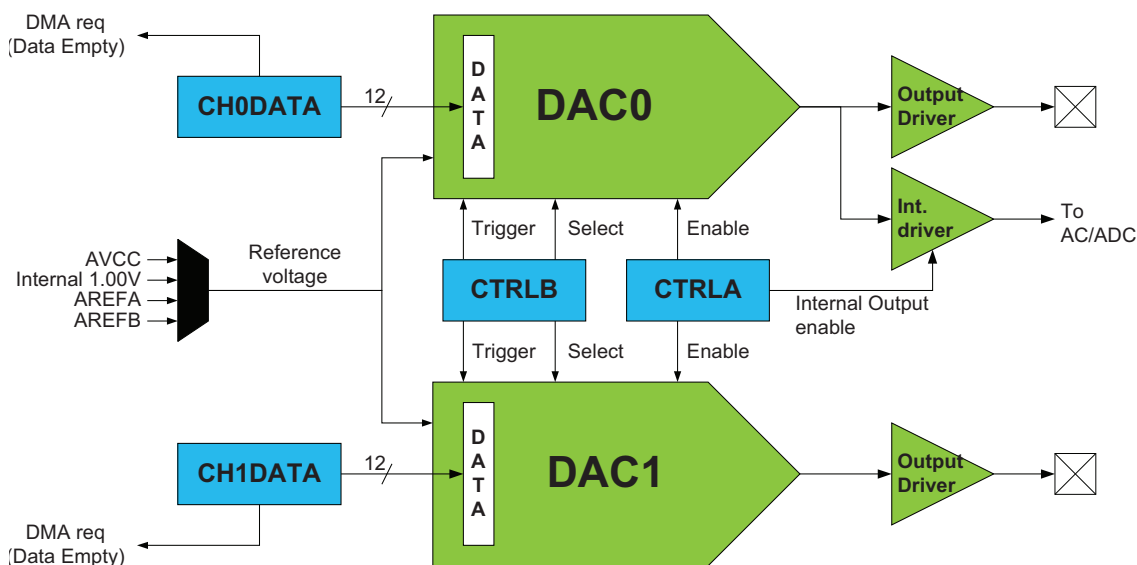
### 30.1 Features

- One Digital to Analog Converter (DAC)
- 12-bit resolution
- Two independent, continuous-drive output channels
- Up to one million samples per second conversion rate per DAC channel
- Built-in calibration that removes:
  - Offset error
  - Gain error
- Multiple conversion trigger sources
  - On new available data
  - Events from the event system
- High drive capabilities and support for
  - Resistive loads
  - Capacitive loads
  - Combined resistive and capacitive loads
- Internal and external reference options
- DAC output available as input to analog comparator and ADC
- Low-power mode, with reduced drive strength
- Optional DMA transfer of data

### 30.2 Overview

The digital-to-analog converter (DAC) converts digital values to voltages. The DAC has two channels, each with 12-bit resolution, and is capable of converting up to one million samples per second (msps) on each channel. The built-in calibration system can remove offset and gain error when loaded with calibration values from software.

Figure 30-1. DAC overview.



## 35. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	$Rd \leftarrow Rd + Rr$	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	$Rd \leftarrow Rd + 1:Rd + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	$Rd \leftarrow Rd - Rr$	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	$Rd \leftarrow Rd - K$	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	$Rd \leftarrow Rd - K - C$	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	$Rd + 1:Rd \leftarrow Rd + 1:Rd - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	$Rd \leftarrow Rd \bullet Rr$	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	$Rd \leftarrow Rd \bullet K$	Z,N,V,S	1
OR	Rd, Rr	Logical OR	$Rd \leftarrow Rd \vee Rr$	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	$Rd \leftarrow Rd \oplus Rr$	Z,N,V,S	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V,S	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (\$FFh - K)$	Z,N,V,S	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V,S	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V,S	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V,S	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
MUL	Rd,Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr (UU)$	Z,C	2
MULS	Rd,Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr (SS)$	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr (SU)$	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr << 1 (UU)$	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	$R1:R0 \leftarrow Rd \times Rr << 1 (SS)$	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr << 1 (SU)$	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 $\leftarrow$ Encrypt(R15:R0, K) else if (H = 1) then R15:R0 $\leftarrow$ Decrypt(R15:R0, K)		1/2
Branch instructions					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow 0$	None	2
EIJMP		Extended Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow EIND$	None	2
JMP	k	Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Call Subroutine	$PC \leftarrow PC + k + 1$	None	2 / 3 <sup>(1)</sup>

Mnemonics	Operands	Description	Operation	Flags	#Clocks
IN	Rd, A	In From I/O Location	$Rd \leftarrow I/O(A)$	None	1
OUT	A, Rr	Out To I/O Location	$I/O(A) \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	1 <sup>(1)</sup>
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2 <sup>(1)</sup>
XCH	Z, Rd	Exchange RAM location	$Temp \leftarrow Rd,$ $Rd \leftarrow (Z),$ $(Z) \leftarrow Temp$	None	2
LAS	Z, Rd	Load and Set RAM location	$Temp \leftarrow Rd,$ $Rd \leftarrow (Z),$ $(Z) \leftarrow Temp \vee (Z)$	None	2
LAC	Z, Rd	Load and Clear RAM location	$Temp \leftarrow Rd,$ $Rd \leftarrow (Z),$ $(Z) \leftarrow (\$FFh - Rd) \cdot (Z)$	None	2
LAT	Z, Rd	Load and Toggle RAM location	$Temp \leftarrow Rd,$ $Rd \leftarrow (Z),$ $(Z) \leftarrow Temp \oplus (Z)$	None	2
Bit and bit-test instructions					
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n),$ $Rd(0) \leftarrow 0,$ $C \leftarrow Rd(7)$	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1),$ $Rd(7) \leftarrow 0,$ $C \leftarrow Rd(0)$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C,$ $Rd(n+1) \leftarrow Rd(n),$ $C \leftarrow Rd(7)$	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C,$ $Rd(n) \leftarrow Rd(n+1),$ $C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftrightarrow Rd(7..4)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	$I/O(A, b) \leftarrow 1$	None	1
CBI	A, b	Clear Bit in I/O Register	$I/O(A, b) \leftarrow 0$	None	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1

## 37.3 Current consumption

Table 37-4. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{CC}$	Active Power consumption <sup>(1)</sup>	32kHz, Ext. Clk	$V_{CC} = 1.8V$	120		$\mu A$
			$V_{CC} = 3.0V$	270		
		1MHz, Ext. Clk	$V_{CC} = 1.8V$	350		
			$V_{CC} = 3.0V$	697		
		2MHz, Ext. Clk	$V_{CC} = 1.8V$	658	700	$mA$
			$V_{CC} = 3.0V$	1.1	1.4	
	Idle Power consumption <sup>(1)</sup>	32kHz, Ext. Clk	$V_{CC} = 1.8V$	4.3		$\mu A$
			$V_{CC} = 3.0V$	4.8		
		1MHz, Ext. Clk	$V_{CC} = 1.8V$	78		
			$V_{CC} = 3.0V$	150		
		2MHz, Ext. Clk	$V_{CC} = 1.8V$	150	350	$mA$
			$V_{CC} = 3.0V$	290	600	
	Power-down power consumption	T = 25°C	$V_{CC} = 3.0V$	0.1	1.0	$\mu A$
		T = 85°C		1.8	5.0	
		WDT and Sampled BOD enabled, T = 25°C	$V_{CC} = 3.0V$	1.3	3.0	
		WDT and Sampled BOD enabled, T = 85°C		3.1	7.0	
	Power-save power consumption <sup>(2)</sup>	RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	$V_{CC} = 1.8V$	0.6	2	
			$V_{CC} = 3.0V$	0.7	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	$V_{CC} = 1.8V$	0.8	3	
			$V_{CC} = 3.0V$	1.0	3	
	Reset power consumption	Current through $\overline{RESET}$ pin subtracted	$V_{CC} = 3.0V$	250		

- Notes:
1. All Power Reduction Registers set.
  2. Maximum limits are based on characterization, and not tested in production.

**Table 37-14. Accuracy characteristics.**

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
RES	Input Resolution					12	Bits
INL <sup>(1)</sup>	Integral non-linearity	$V_{REF} = \text{Ext } 1.0V$	$V_{CC} = 1.6V$		$\pm 2.0$	$\pm 3$	lsb
			$V_{CC} = 3.6V$		$\pm 1.5$	$\pm 2.5$	
		$V_{REF} = AV_{CC}$	$V_{CC} = 1.6V$		$\pm 2.0$	$\pm 4$	
			$V_{CC} = 3.6V$		$\pm 1.5$	$\pm 4$	
		$V_{REF} = \text{INT}1V$	$V_{CC} = 1.6V$		$\pm 5.0$		
			$V_{CC} = 3.6V$		$\pm 5.0$		
DNL <sup>(1)</sup>	Differential non-linearity	$V_{REF} = \text{Ext } 1.0V$	$V_{CC} = 1.6V$		$\pm 1.5$	3	
			$V_{CC} = 3.6V$		$\pm 0.6$	1.5	
		$V_{REF} = AV_{CC}$	$V_{CC} = 1.6V$		$\pm 1.0$	3.5	
			$V_{CC} = 3.6V$		$\pm 0.6$	1.5	
		$V_{REF} = \text{INT}1V$	$V_{CC} = 1.6V$		$\pm 4.5$		
			$V_{CC} = 3.6V$		$\pm 4.5$		
	Gain error	After calibration			<4		
	Gain calibration step size				4		
	Gain calibration drift	$V_{REF} = \text{Ext } 1.0V$			<0.2		mV/K
	Offset error	After calibration			<1		lsb
	Offset calibration step size				1		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

## 37.8 Analog Comparator Characteristics

**Table 37-15. Analog Comparator characteristics.**

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
$V_{off}$	Input offset voltage				$< \pm 10$		mV
$I_{lk}$	Input leakage current				<1		nA
	Input voltage range			-0.1		$AV_{CC}$	V
	AC startup time				100		$\mu s$
$V_{hys1}$	Hysteresis, None				0		mV
$V_{hys2}$	Hysteresis, Small	mode = High Speed (HS)			13		
		mode = Low Power (LP)			30		
$V_{hys3}$	Hysteresis, Large	mode = HS			30		
		mode = LP			60		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
$t_{\text{delay}}$	Propagation delay	$V_{\text{CC}} = 3.0\text{V}$ , $T = 85^{\circ}\text{C}$	mode = HS		30	90	ns
		mode = HS			30		
		$V_{\text{CC}} = 3.0\text{V}$ , $T = 85^{\circ}\text{C}$	mode = LP		130	500	
		mode = LP			130		
	Current source calibration range	Single mode		2		8	$\mu\text{s}$
		Double mode		4		16	
	64-Level Voltage Scaler	Integral non-linearity (INL)			0.3	0.5	lsb

## 37.9 Bandgap and Internal 1.0V Reference Characteristics

Table 37-16. Bandgap and Internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC or DAC	$1 \text{ Clk}_{\text{PER}} + 2.5\mu\text{s}$			$\mu\text{s}$
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	$T = 85^{\circ}\text{C}$ , after calibration	0.99	1	1.01	
	Variation over voltage and temperature	Relative to $T = 85^{\circ}\text{C}$ , $V_{\text{CC}} = 3.0\text{V}$		$\pm 1.0$		%

## 37.10 Brownout Detection Characteristics

Table 37-17. Brownout detection characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{\text{BOT}}$	BOD level 0 falling $V_{\text{CC}}$		1.60	1.62	1.72	V
	BOD level 1 falling $V_{\text{CC}}$			1.8		
	BOD level 2 falling $V_{\text{CC}}$			2.0		
	BOD level 3 falling $V_{\text{CC}}$			2.2		
	BOD level 4 falling $V_{\text{CC}}$			2.4		
	BOD level 5 falling $V_{\text{CC}}$			2.6		
	BOD level 6 falling $V_{\text{CC}}$			2.8		
	BOD level 7 falling $V_{\text{CC}}$			3.0		
$t_{\text{BOD}}$	Detection time	Continuous mode		0.4		$\mu\text{s}$
		Sampled mode		1000		
$V_{\text{HYST}}$	Hysteresis			1.6		%

### 37.15.5 Internal Phase Locked Loop (PLL) characteristics

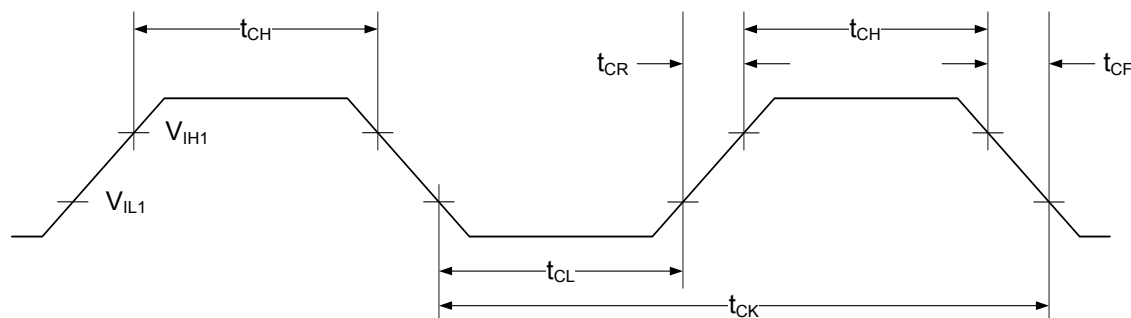
**Table 37-27. Internal PLL characteristics.**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{IN}$	Input frequency	Output frequency must be within $f_{OUT}$	0.4		64	MHz
$f_{OUT}$	Output frequency <sup>(1)</sup>	$V_{CC} = 1.6 - 1.8V$	20		48	
		$V_{CC} = 2.7 - 3.6V$	20		128	
	Start-up time			25		$\mu s$
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

### 37.15.6 External clock characteristics

**Figure 37-3. External clock drive waveform.**



**Table 37-28. External clock used as system clock without prescaling.**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency <sup>(1)</sup>	$V_{CC} = 1.6 - 1.8V$	0		12	MHz
		$V_{CC} = 2.7 - 3.6V$	0		32	
$t_{CK}$	Clock period	$V_{CC} = 1.6 - 1.8V$	83.3			ns
		$V_{CC} = 2.7 - 3.6V$	31.5			
$t_{CH}$	Clock high time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
$t_{CL}$	Clock low time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
$t_{CR}$	Rise time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
$t_{CF}$	Fall time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
$\Delta t_{CK}$	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

## 38. Typical Characteristics

### 38.1 Current consumption

#### 38.1.1 Active mode supply current

Figure 38-1. Active supply current vs. frequency.

$f_{SYS} = 0 - 1\text{MHz}$  external clock,  $T = 25^{\circ}\text{C}$ .

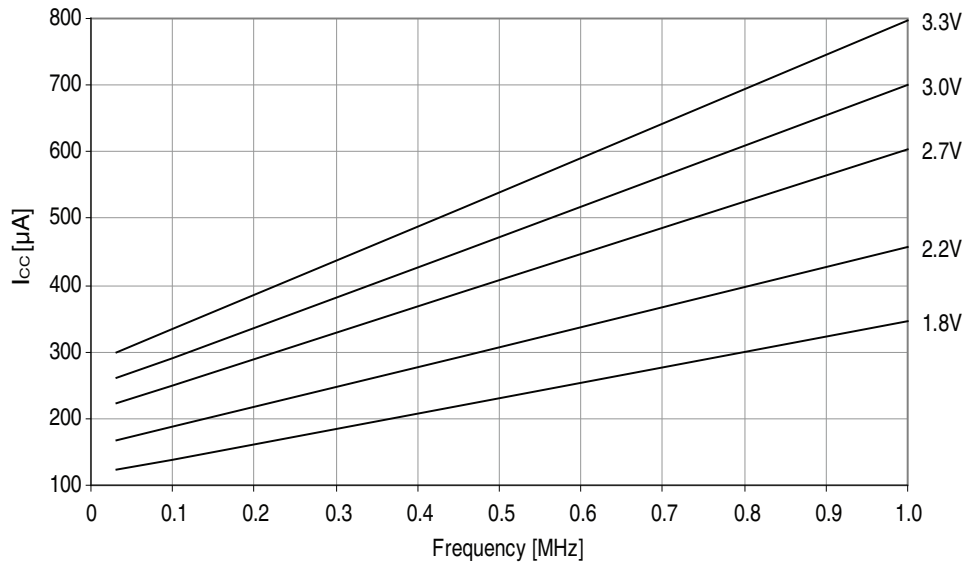
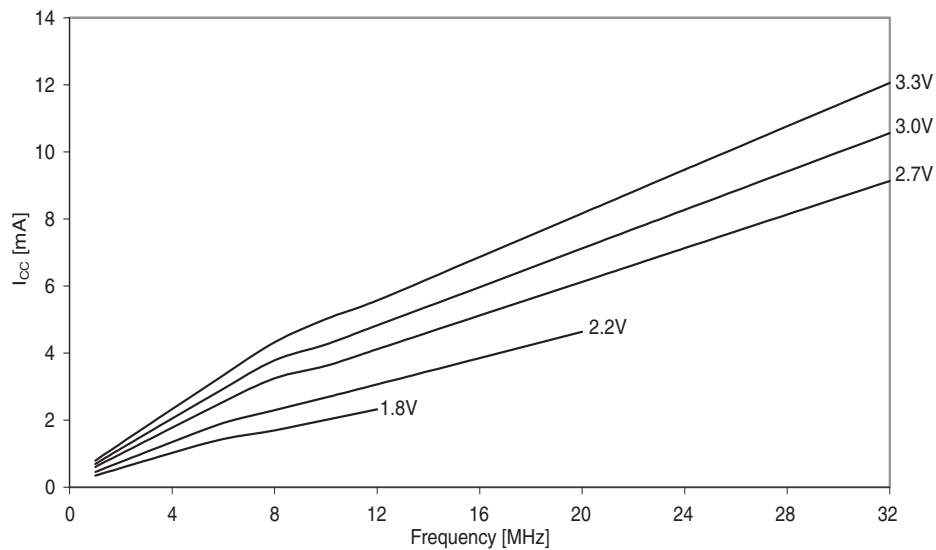


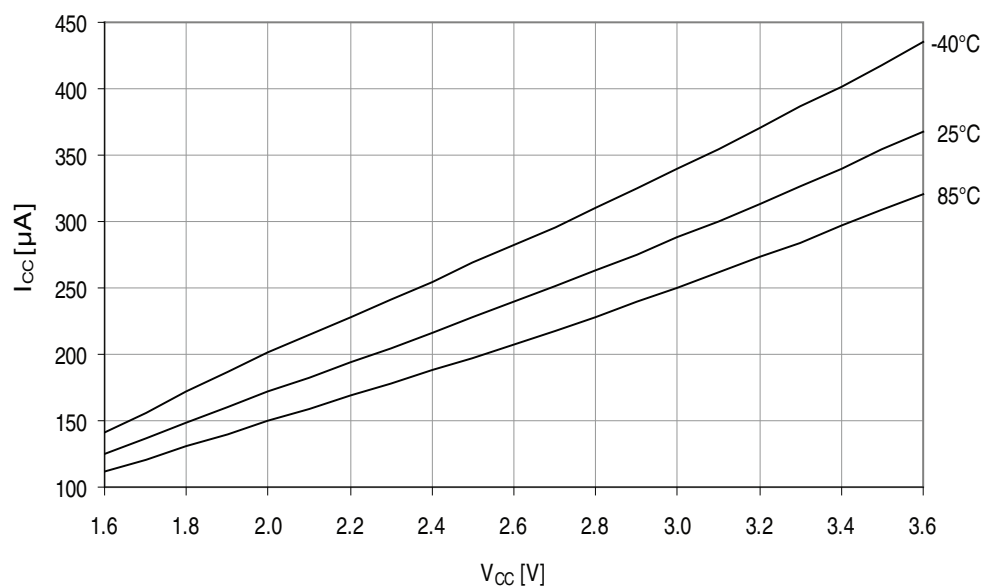
Figure 38-2. Active supply current vs. frequency.

$f_{SYS} = 1 - 32\text{MHz}$  external clock,  $T = 25^{\circ}\text{C}$ .



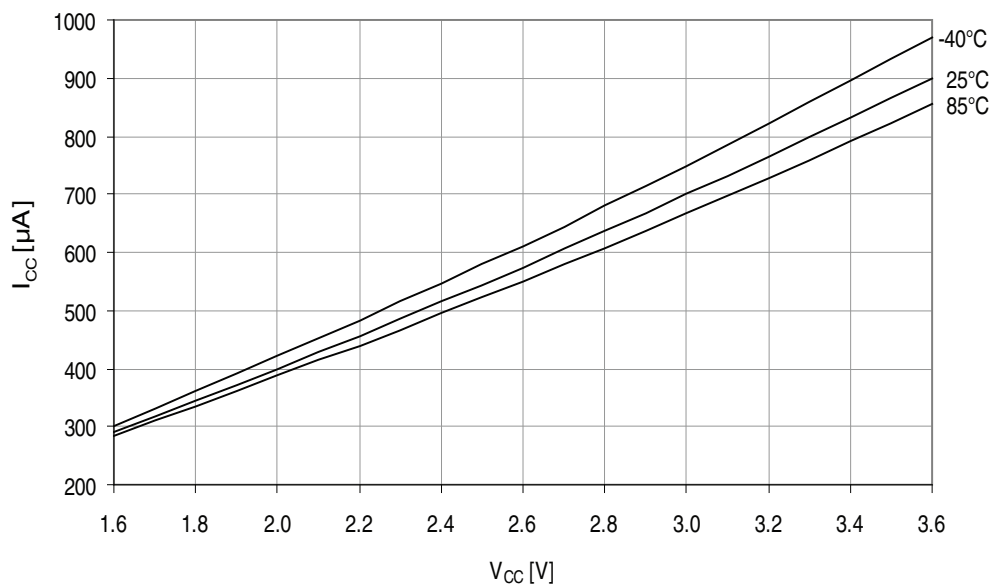
**Figure 38-3. Active mode supply current vs.  $V_{CC}$ .**

$f_{SYS} = 32.768\text{kHz}$  internal oscillator.



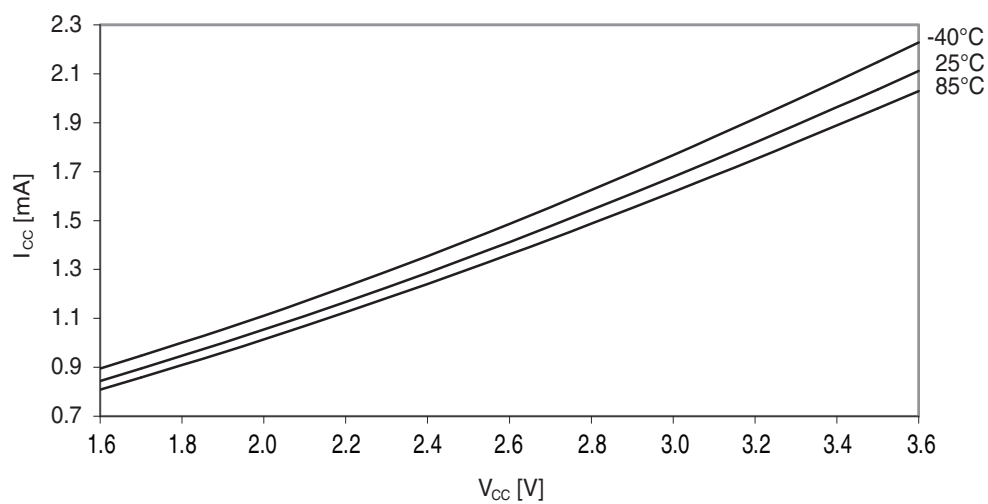
**Figure 38-4. Active mode supply current vs.  $V_{CC}$ .**

$f_{SYS} = 1\text{MHz}$  external clock.



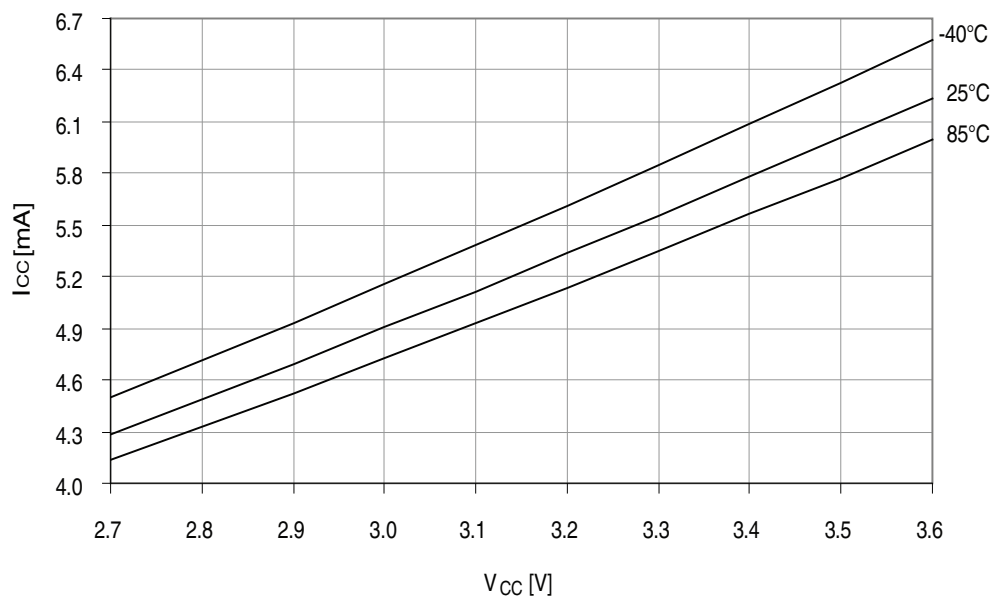
**Figure 38-13. Idle mode supply current vs.  $V_{CC}$ .**

$f_{SYS} = 32\text{MHz}$  internal oscillator prescaled to 8MHz.

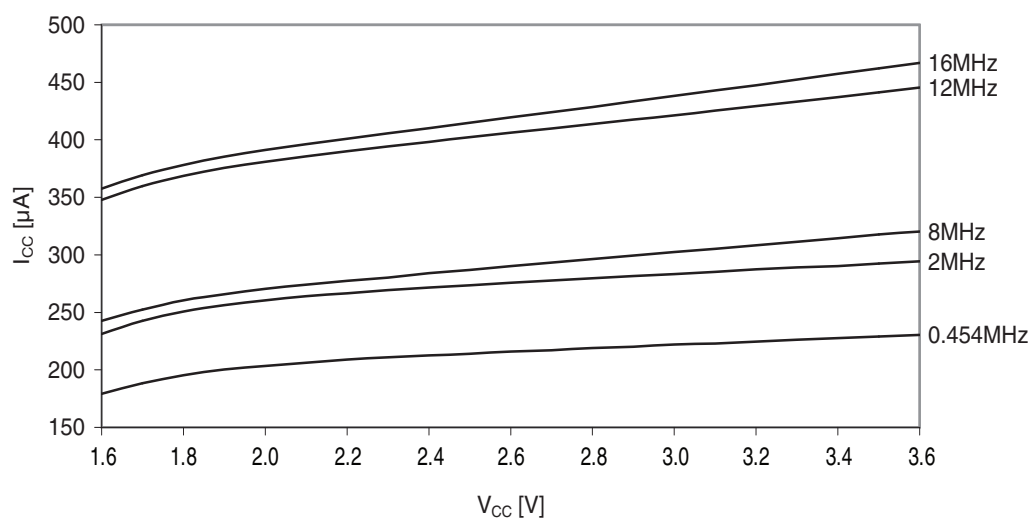


**Figure 38-14. Idle mode current vs.  $V_{CC}$ .**

$f_{SYS} = 32\text{MHz}$  internal oscillator.



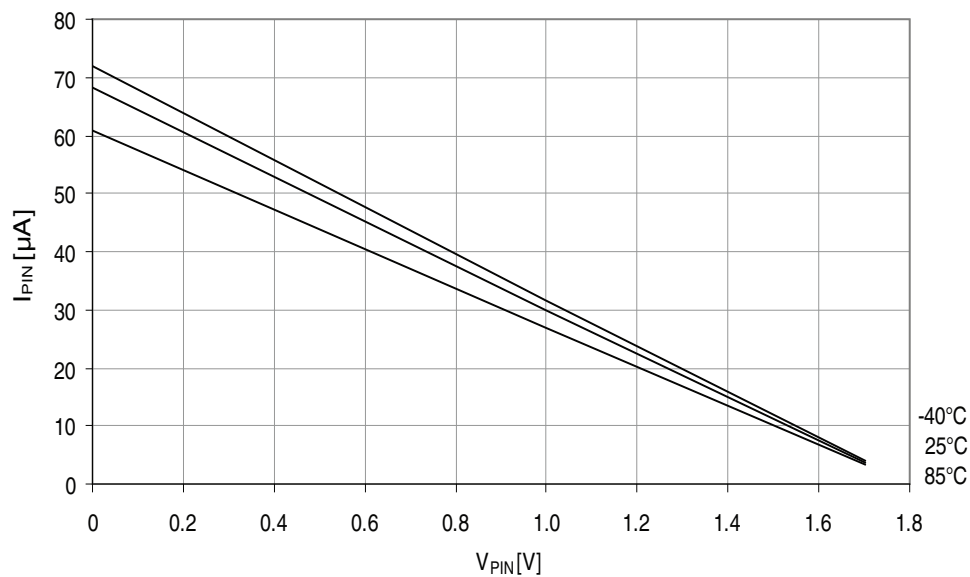
**Figure 38-19. Standby supply current vs.  $V_{CC}$ .**  
*25°C, running from different crystal oscillators.*



## 38.2 I/O Pin Characteristics

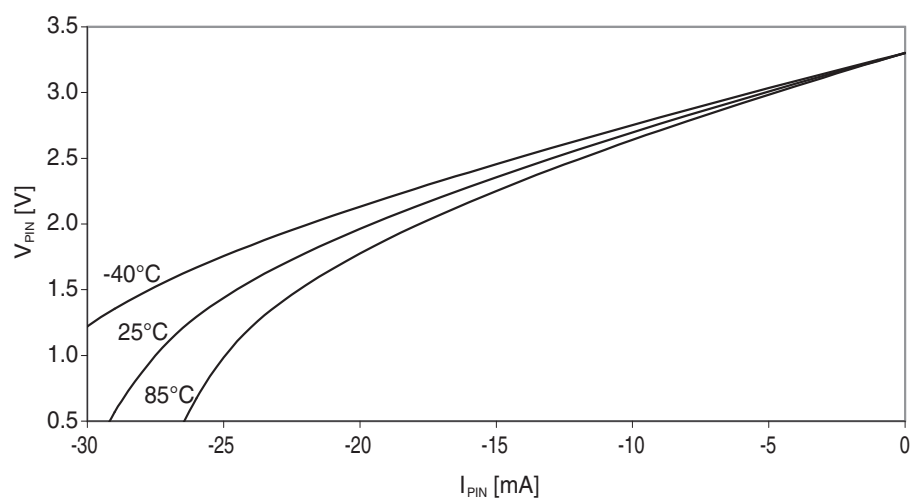
### 38.2.1 Pull-up

**Figure 38-20. I/O pin pull-up resistor current vs. input voltage.**  
 *$V_{CC} = 1.8V$ .*

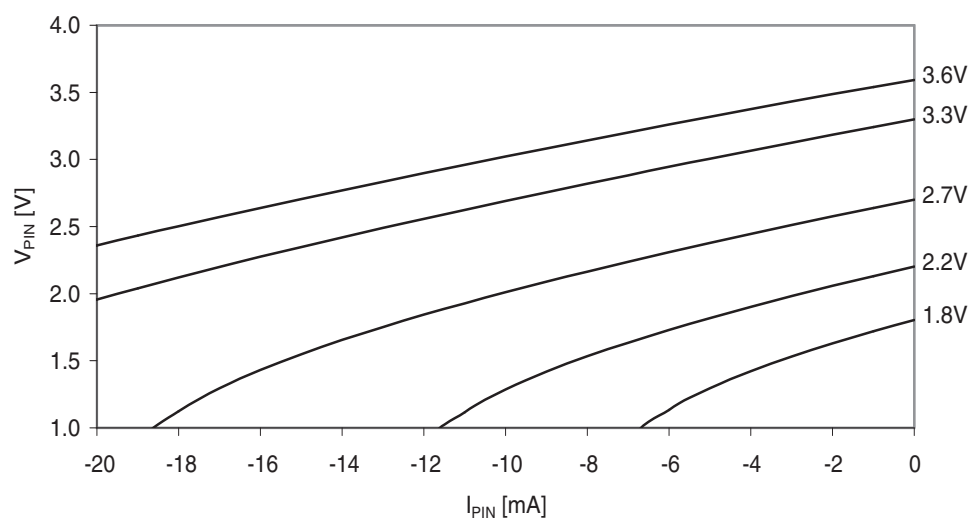


**Figure 38-25. I/O pin output voltage vs. source current.**

$V_{CC} = 3.3V$ .

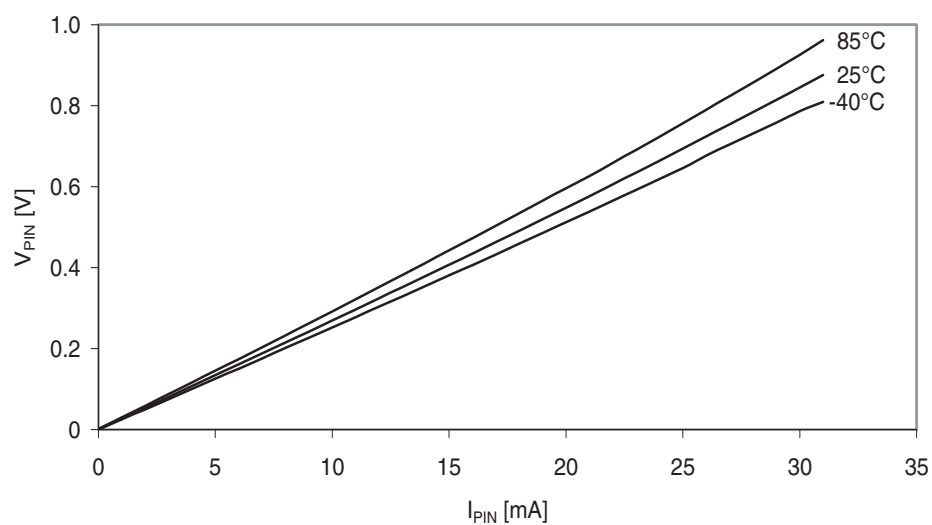


**Figure 38-26. I/O pin output voltage vs. source current.**

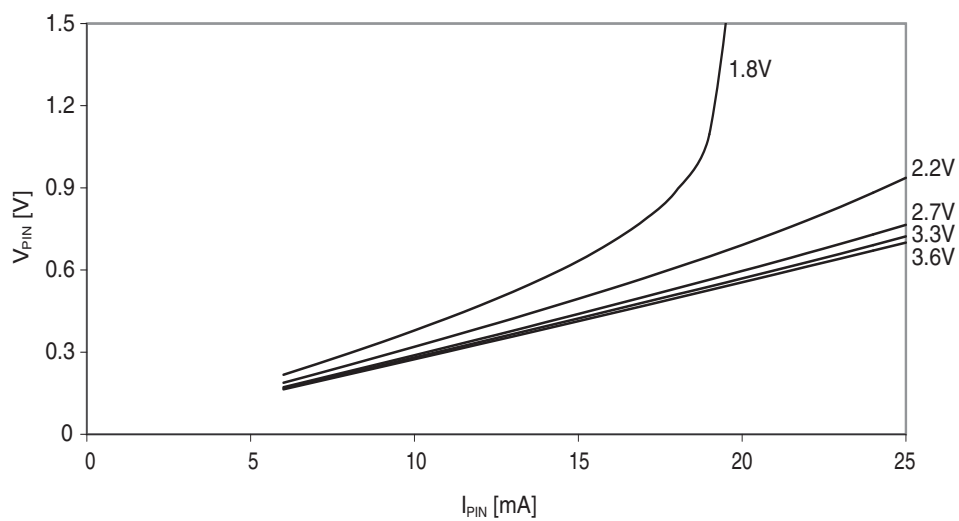


**Figure 38-29. I/O pin output voltage vs. sink current.**

$V_{CC} = 3.3V$ .

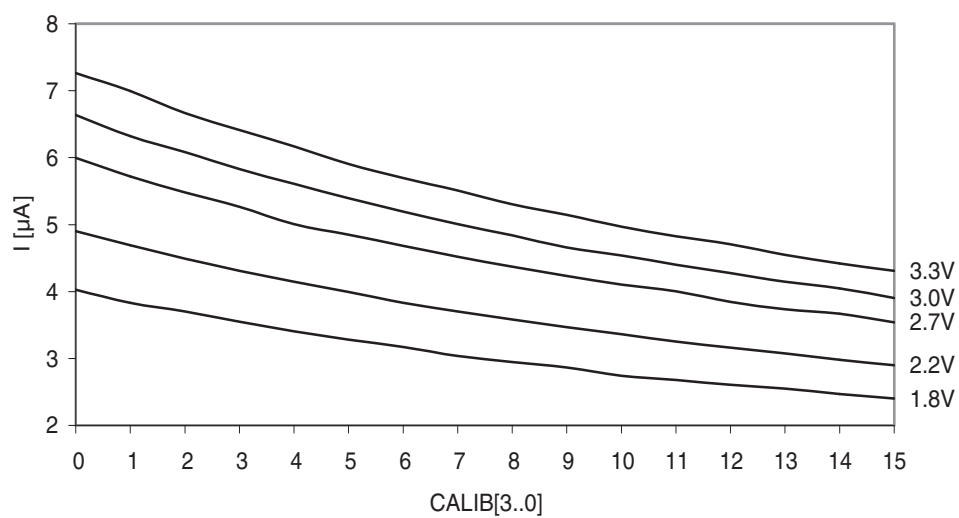


**Figure 38-30. I/O pin output voltage vs. sink current.**



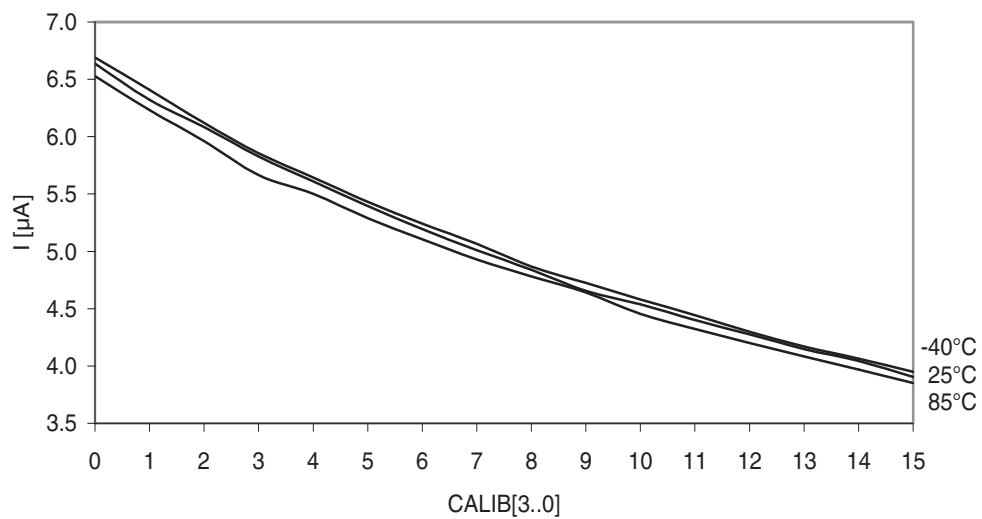
**Figure 38-55. Analog comparator current source vs. calibration value.**

*Temperature = 25°C.*

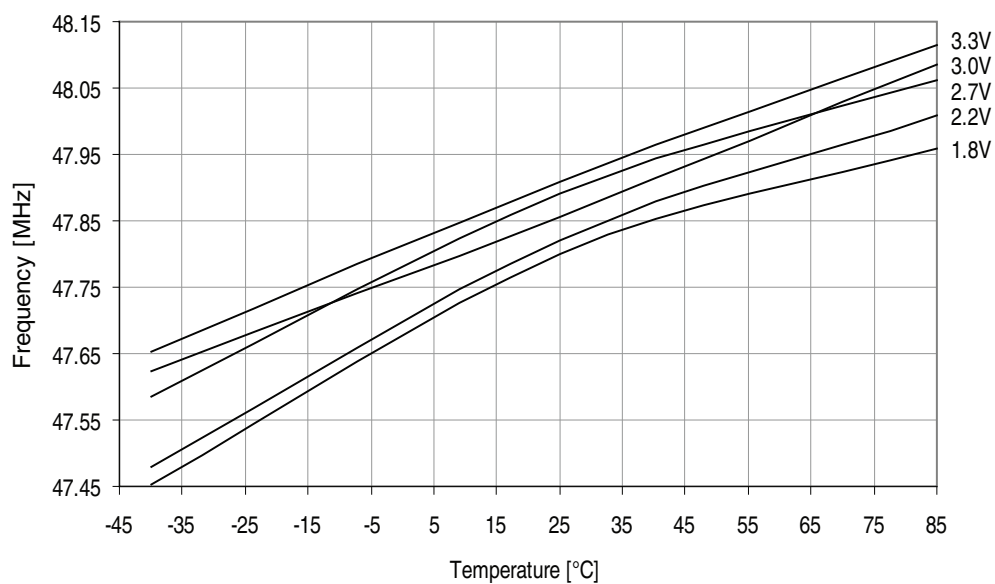


**Figure 38-56. Analog comparator current source vs. calibration value.**

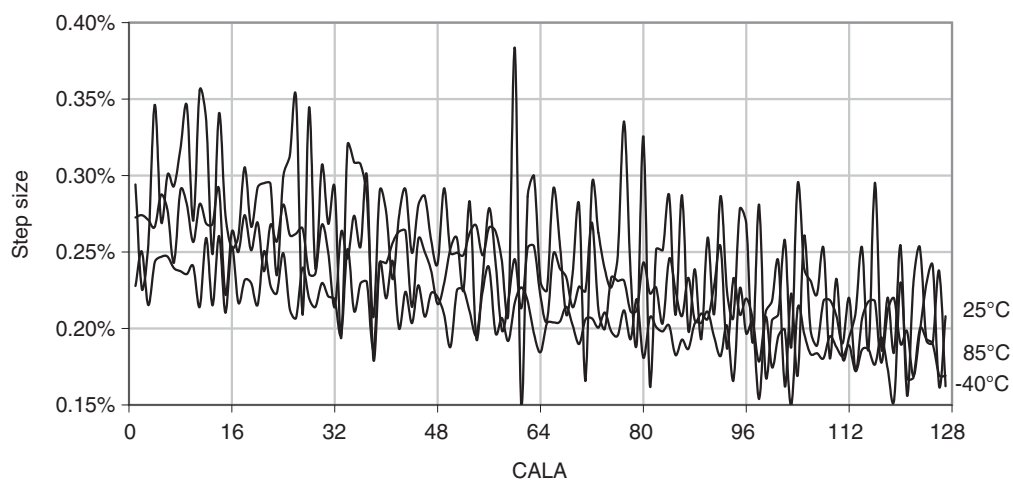
*$V_{CC} = 3.0\text{V}$ .*



**Figure 38-79. 48MHz internal oscillator frequency vs. temperature.**  
*DPLL enabled, from the 32.768kHz internal oscillator.*



**Figure 38-80. 48MHz internal oscillator CALA calibration step size.**  
 $V_{CC} = 3.0V$ .



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