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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	47
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3bu-aur">https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3bu-aur</a>

# 1. Ordering Information

Ordering code	Flash (bytes)	EEPROM (bytes)	SRAM (bytes)	Speed (MHz)	Power supply	Package <sup>(1)(2)(3)</sup>	Temp.
ATxmega256A3BU-AU	256K + 8K	4K	16K	32	1.6 - 3.6V	64A	-40°C-85°C
ATxmega256A3BU-AUR <sup>(4)</sup>							
ATxmega256A3BU-MH	256K + 8K	4K	16K	32	1.6 - 3.6V	64M2	
ATxmega256A3BU-MHR <sup>(4)</sup>							

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For packaging information, see ["Packaging information" on page 67](#).
  4. Tape and reel.

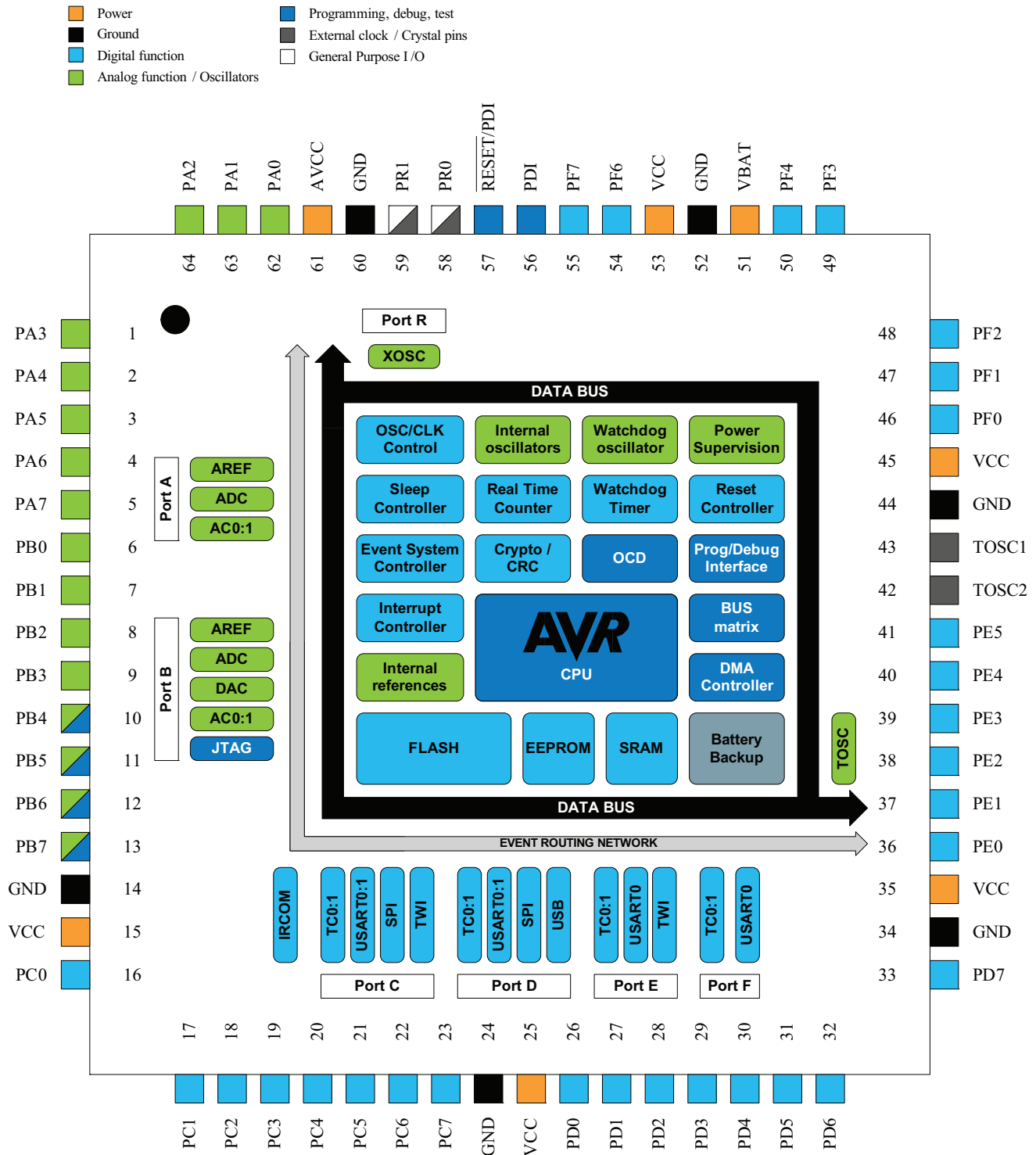
Package type	
<b>64A</b>	64-lead, 14 x 14mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
<b>64M2</b>	64-pad, 9 x 9 x 1.0mm body, lead pitch 0.50mm, 7.65mm exposed pad, quad flat no-lead package (QFN)

## Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	USB connectivity	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

## 2. Pinout/Block Diagram

Figure 2-1. Block diagram and pinout.



- Notes:
1. For full details on pinout and pin functions refer to "Pinout and Pin Functions" on page 55.
  2. The large center pad underneath the QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

### 3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA device achieves CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA A3BU devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel DMA controller; eight-channel event system and programmable multilevel interrupt controller; 47 general purpose I/O lines; 32-bit real-time counter (RTC) with battery backup system; seven flexible 16-bit Timer/Counters with compare modes and PWM; one full speed USB 2.0 interface; six USARTs; two two-wire serial interfaces (TWIs); two serial peripheral interfaces (SPIs); AES and DES cryptographic engine; two 16-channel, 12-bit ADCs with programmable gain; one 2-channel 12-bit DAC; four analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available. The devices also have an IEEE std. 1149.1 compliant JTAG interface, and this can also be used for boundary scan, on-chip debug and programming.

The XMEGA A3BU devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, DMA controller, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, USB resume, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI or JTAG interfaces. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

## 10. System Clock and Clock options

### 10.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal oscillators:
  - 32MHz run-time calibrated and tuneable oscillator
  - 2MHz run-time calibrated oscillator
  - 32.768kHz calibrated oscillator
  - 32kHz ultra low power (ULP) oscillator with 1kHz output
- External clock options
  - 0.4MHz - 16MHz crystal oscillator
  - 32.768kHz crystal oscillator
  - External clock
- PLL with 20MHz - 128MHz output frequency
  - Internal and external clock options and 1x to 31x multiplication
  - Lock detector
- Clock prescalers with 1x to 2048x division
- Fast peripheral clocks running at two and four times the CPU clock
- Automatic run-time calibration of internal oscillators
- External oscillator and PLL lock failure detection with optional non-maskable interrupt

### 10.2 Overview

Atmel AVR XMEGA A3BU devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

[Figure 10-1 on page 19](#) presents the principal clock system in the XMEGA A3BU family of devices. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in [“Power Management and Sleep Modes” on page 21](#)

## 11. Power Management and Sleep Modes

### 11.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes
  - Idle
  - Power down
  - Power save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

### 11.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

### 11.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

#### 11.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, event system and DMA controller are kept running. Any enabled interrupt will wake the device.

#### 11.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

## 13. WDT – Watchdog Timer

### 13.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

### 13.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

## 14. Battery Backup System

### 14.1 Features

- Battery Backup voltage supply from dedicated  $V_{BAT}$  power pin for:
  - One Ultra Low-power 32-bit Real Time Counter (RTC)
  - One 32.768kHz crystal oscillator with failure detection monitor
  - Two Backup Registers
- Typical power consumption of 500nA with Real Time Counter running
- Automatic switching from main power to battery backup power at:
  - Brown-Out Detection (BOD) reset
- Automatic switching from battery backup power to main power:
  - Device reset after Brown-Out Reset (BOR) is released
  - Device reset after Power-On Reset (POR) and BOR is released

### 14.2 Overview

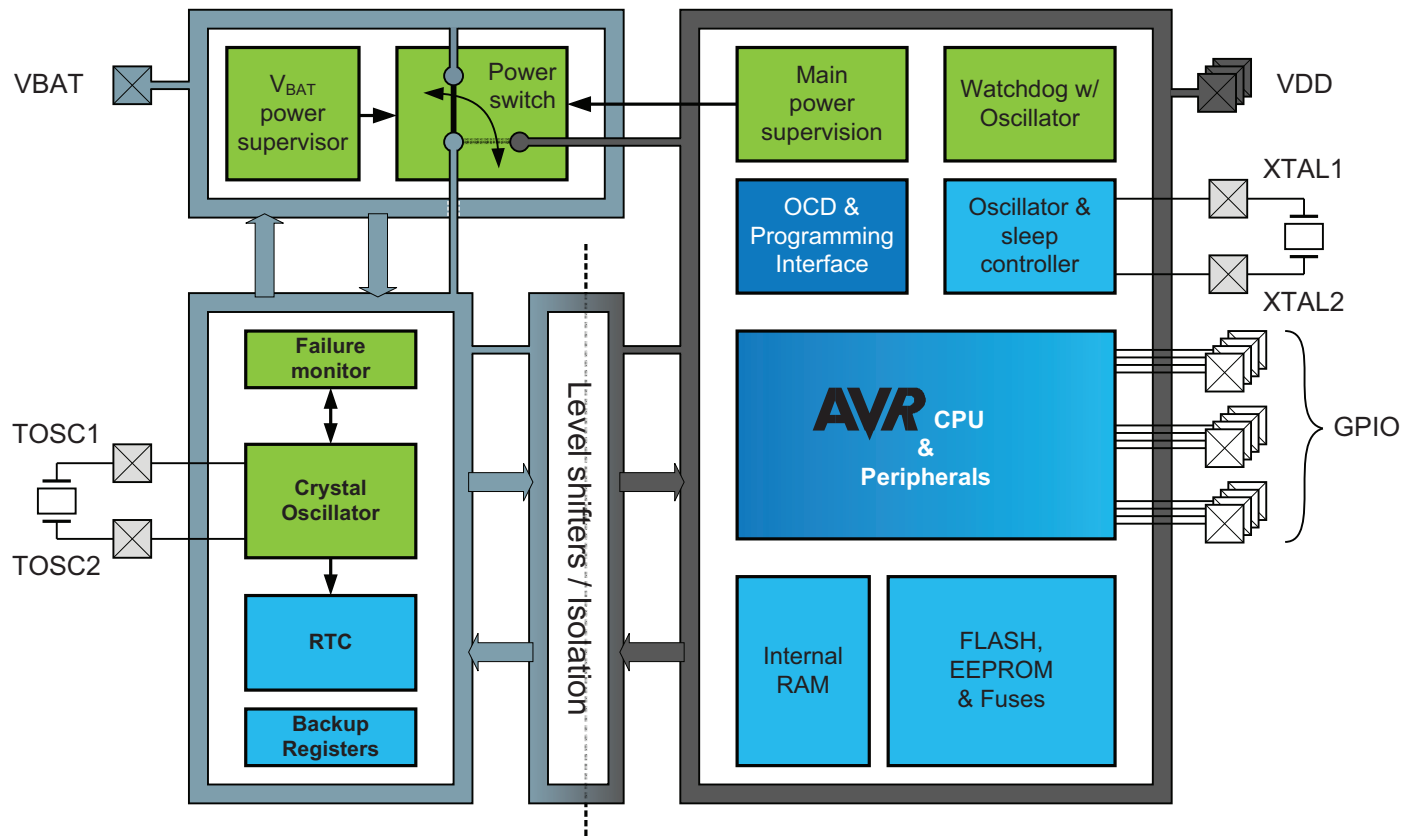
Atmel AVR XMEGA family is already running in an ultra low leakage process with power-save current consumption below 2μA with RTC, BOD and watchdog enabled. Still, for some applications where time keeping is important, the system would have one main battery or power source used for day to day tasks, and one backup battery power for the time keeping functionality. The Battery Backup System includes functionality that enable automatic power switching between main power and a battery backup power. [Figure 14-1 on page 27](#) shows an overview of the system.

The Battery Backup Module support connection of a backup battery to the dedicated  $V_{BAT}$  power pin. This will ensure power to the 32-bit Real Time Counter, a 32.768kHz crystal oscillator with failure detection monitor and two backup registers, when the main battery or power source is unavailable.

Upon main power loss the device will automatically detect this and the Battery Backup Module will switch to be powered from the  $V_{BAT}$  pin. After main power has been restored and both main POR and BOR are released, the Battery Backup Module will automatically switch back to be powered from main power again.

The 32-bit real time counter (RTC) must be clocked from the 1Hz output of a 32.768kHz crystal oscillator connected between the TOSC1 and TOSC2 pins when running from  $V_{BAT}$ . For more details on the 32-bit RTC refer to the [“RTC32 – 32-bit Real-Time Counter” on page 39](#).

Figure 14-1. Battery Backup Module and its power domain implementation.



## 20. Hi-Res – High Resolution Extension

### 20.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM, and dual-slope PWM generation
- Supports the AWeX when this is used for the same timer/counter

### 20.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock ( $\text{Clk}_{\text{PER}4}$ ). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There are four hi-res extensions that each can be enabled for each timer/counters pair on PORTC, PORTD, PORTE and PORTF. The notation of these are HIRESC, HIRESD, HIRESE and HIRESF, respectively.

## 26. IRCOM – IR Communication Module

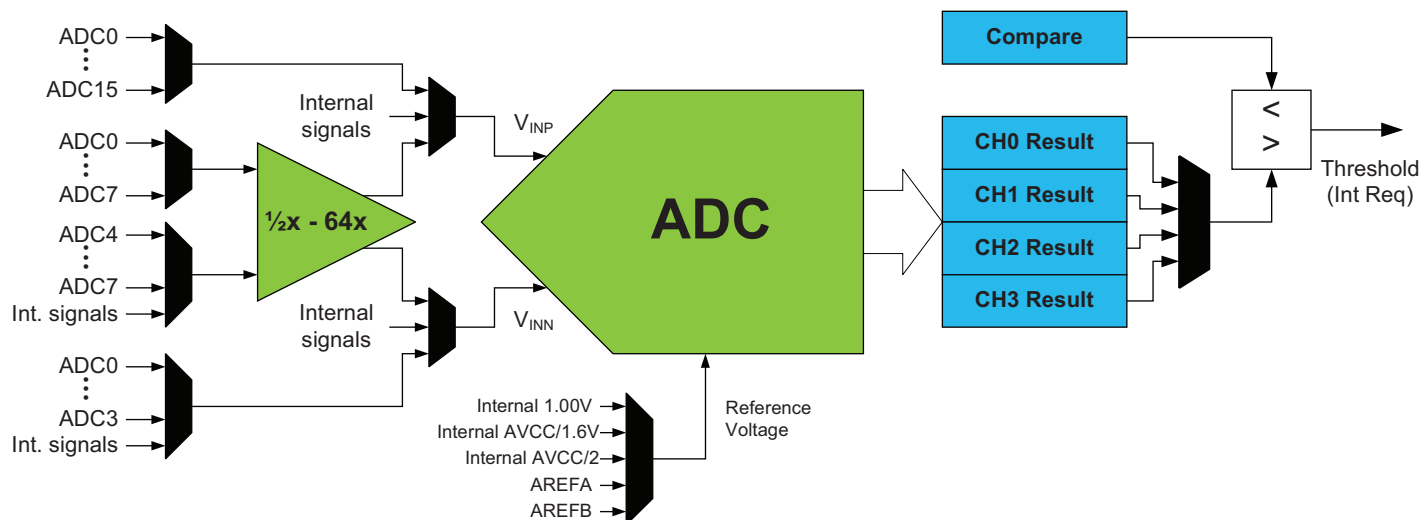
### 26.1 Features

- Pulse modulation/demodulation for infrared communication
- IrDA compatible for baud rates up to 115.2Kbps
- Selectable pulse modulation scheme
  - 3/16 of the baud rate period
  - Fixed pulse period, 8-bit programmable
  - Pulse modulation disabled
- Built-in filtering
- Can be connected to and used by any USART

### 26.2 Overview

Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2Kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

**Figure 29-1. ADC overview.**



Two inputs can be sampled simultaneously as both the ADC and the gain stage include sample and hold circuits, and the gain stage has 1x gain setting.

Four inputs can be sampled within 1.5µs without any intervention by the application.

The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.5µs for 12-bit to 2.5µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional '1' or '0' padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA and PORTB each has one ADC. Notation of these peripherals are ADCA and ADCB, respectively.

## 31. AC – Analog Comparator

### 31.1 Features

- Four Analog Comparators (AC)
- Selectable propagation delay versus current consumption
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal  $AV_{CC}$  voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

### 31.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

Two important properties of the analog comparator's dynamic behavior are: hysteresis and propagation delay. Both of these parameters may be adjusted in order to achieve the optimal operation for each application.

The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

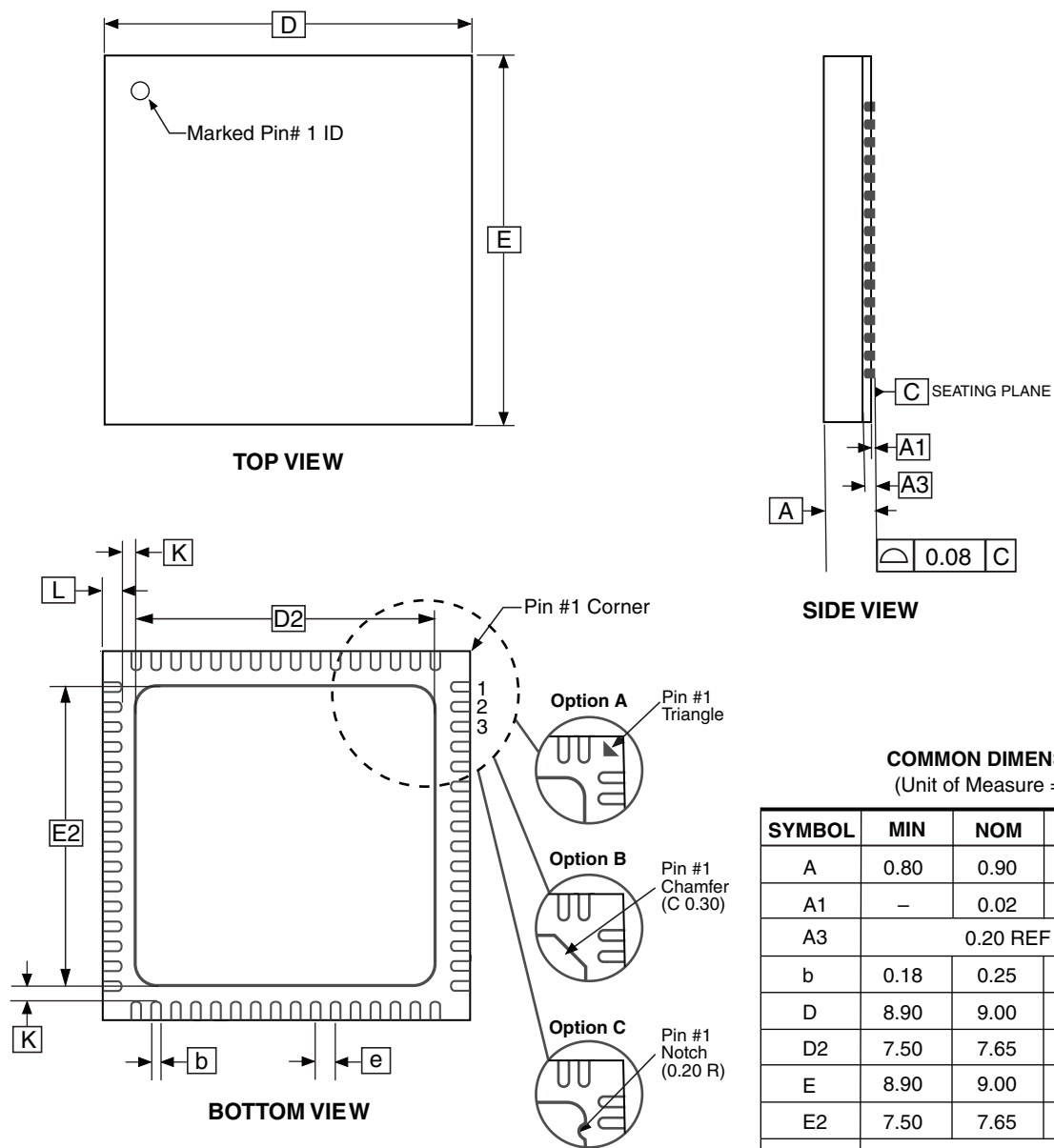
A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA and PORTB each has one AC pair. Notations are ACA and ACB, respectively.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
IN	Rd, A	In From I/O Location	$Rd \leftarrow I/O(A)$	None	1
OUT	A, Rr	Out To I/O Location	$I/O(A) \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	1 <sup>(1)</sup>
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2 <sup>(1)</sup>
XCH	Z, Rd	Exchange RAM location	$Temp \leftarrow Rd,$ $Rd \leftarrow (Z),$ $(Z) \leftarrow Temp$	None	2
LAS	Z, Rd	Load and Set RAM location	$Temp \leftarrow Rd,$ $Rd \leftarrow (Z),$ $(Z) \leftarrow Temp \vee (Z)$	None	2
LAC	Z, Rd	Load and Clear RAM location	$Temp \leftarrow Rd,$ $Rd \leftarrow (Z),$ $(Z) \leftarrow (\$FFh - Rd) \cdot (Z)$	None	2
LAT	Z, Rd	Load and Toggle RAM location	$Temp \leftarrow Rd,$ $Rd \leftarrow (Z),$ $(Z) \leftarrow Temp \oplus (Z)$	None	2
Bit and bit-test instructions					
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n),$ $Rd(0) \leftarrow 0,$ $C \leftarrow Rd(7)$	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1),$ $Rd(7) \leftarrow 0,$ $C \leftarrow Rd(0)$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C,$ $Rd(n+1) \leftarrow Rd(n),$ $C \leftarrow Rd(7)$	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C,$ $Rd(n) \leftarrow Rd(n+1),$ $C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftrightarrow Rd(7..4)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	$I/O(A, b) \leftarrow 1$	None	1
CBI	A, b	Clear Bit in I/O Register	$I/O(A, b) \leftarrow 0$	None	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1

## 36.2 64M2



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	—	0.02	0.05	
A3	0.20 REF			
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	7.50	7.65	7.80	
E	8.90	9.00	9.10	
E2	7.50	7.65	7.80	
e	0.50 BSC			
L	0.35	0.40	0.45	
K	0.20	0.27	0.40	

Notes: 1. JEDEC Standard MO-220, (SAW Singulation) Fig. 1, VMMD.  
2. Dimension and tolerance conform to ASMEY14.5M-1994.

2014-05-30



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**64M2**, 64-pad, 9 x 9 x 1.0mm Body, Lead Pitch 0.50mm,  
7.65mm Exposed Pad, Quad Flat No Lead Package (QFN)

### DRAWING NO.

64M2

### REV.

F

## 37.17 Two-Wire Interface Characteristics

Table 37-33 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 37-7.

Figure 37-7. Two-Wire Interface bus timing.

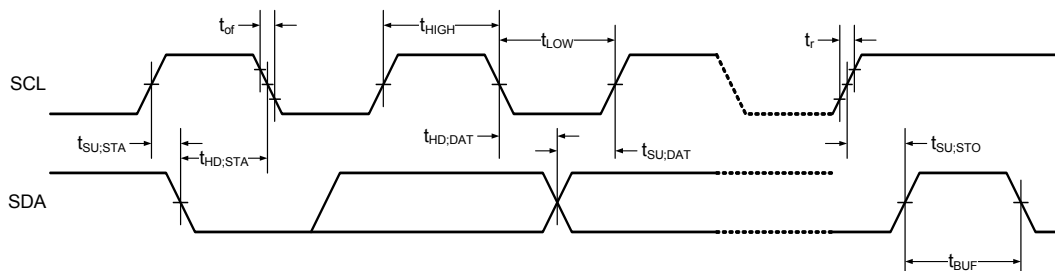
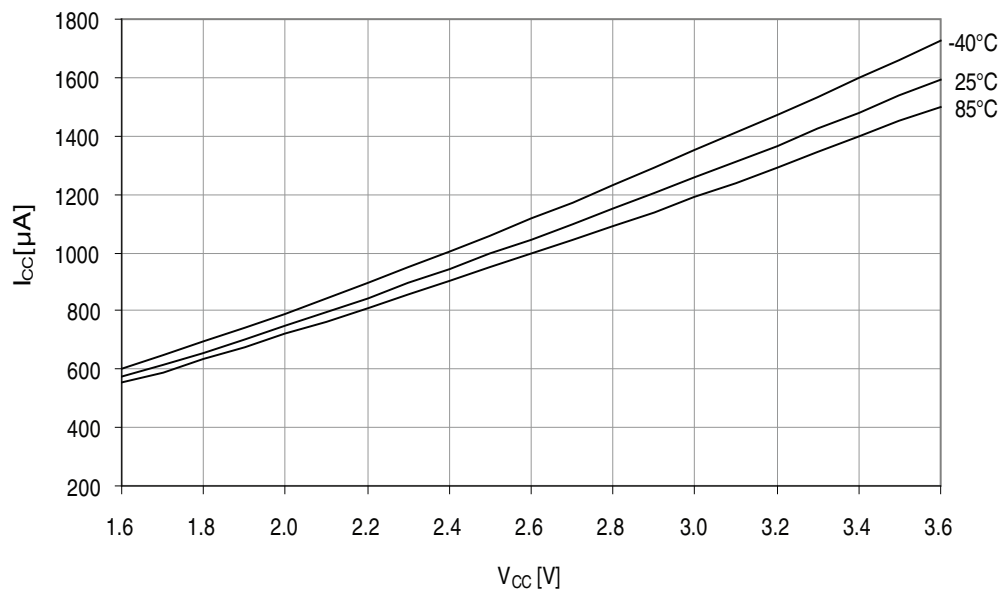


Table 37-33. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{IH}$	Input high voltage		$0.7V_{CC}$		$V_{CC}+0.5$	V
$V_{IL}$	Input low voltage		0.5		$0.3 \times V_{CC}$	
$V_{hys}$	Hysteresis of Schmitt Trigger inputs		$0.05V_{CC}^{(1)}$			
$V_{OL}$	Output low voltage	3mA, sink current	0		0.4	
$t_r$	Rise time for both SDA and SCL		$20+0.1C_b^{(1)(2)}$		300	ns
$t_{of}$	Output fall time from $V_{IHmin}$ to $V_{ILmax}$	$10pF < C_b < 400pF^{(2)}$	$20+0.1C_b^{(1)(2)}$		250	
$t_{SP}$	Spikes suppressed by input filter		0		50	
$I_I$	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	$\mu A$
$C_I$	Capacitance for each I/O pin				10	pF
$f_{SCL}$	SCL clock frequency	$f_{PER}^{(3)} > \max(10f_{SCL}, 250kHz)$	0		400	kHz
$R_P$	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	$\Omega$
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	

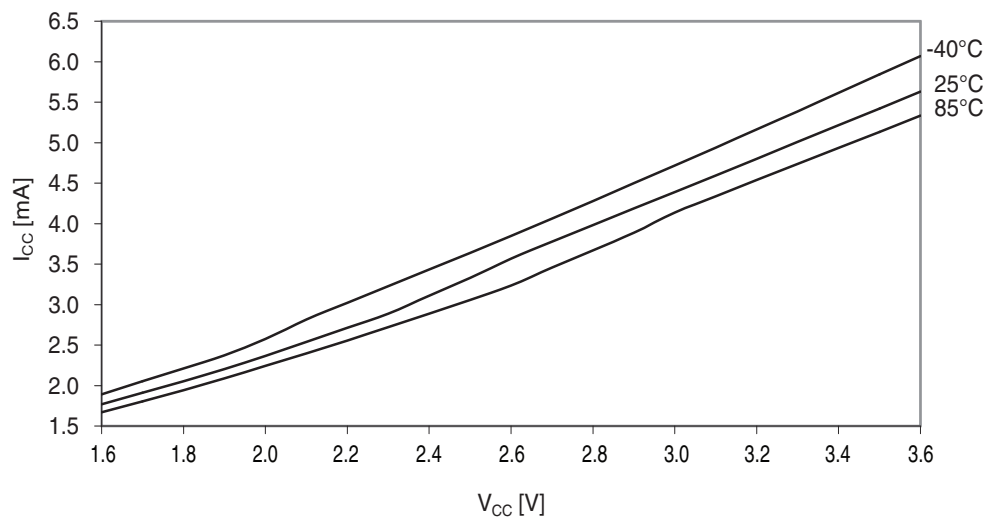
**Figure 38-5. Active mode supply current vs.  $V_{CC}$ .**

$f_{SYS} = 2\text{MHz}$  internal oscillator.



**Figure 38-6. Active mode supply current vs.  $V_{CC}$ .**

$f_{SYS} = 32\text{MHz}$  internal oscillator prescaled to 8MHz.



### 38.7 BOD Characteristics

Figure 38-59.BOD thresholds vs. temperature.  
*BOD level = 1.6V.*

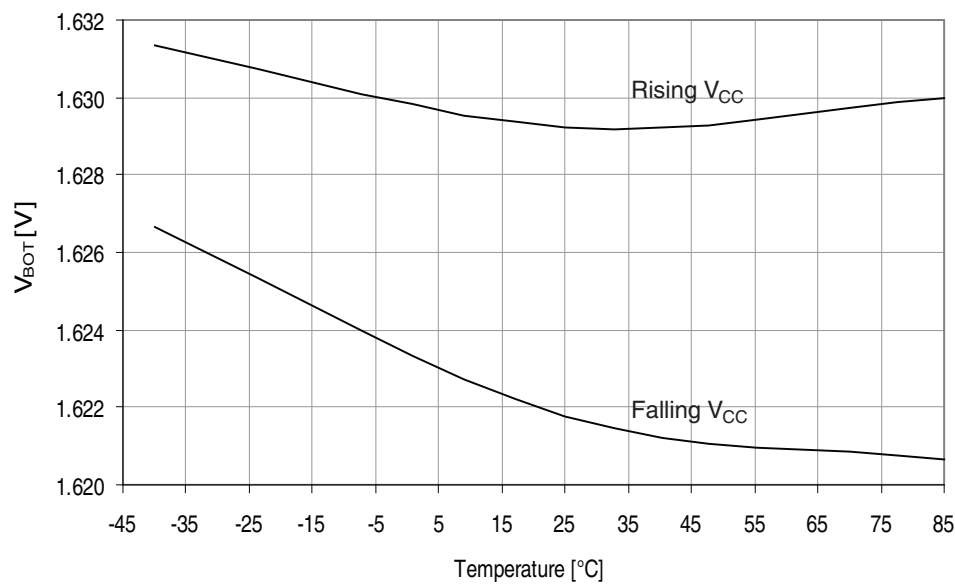
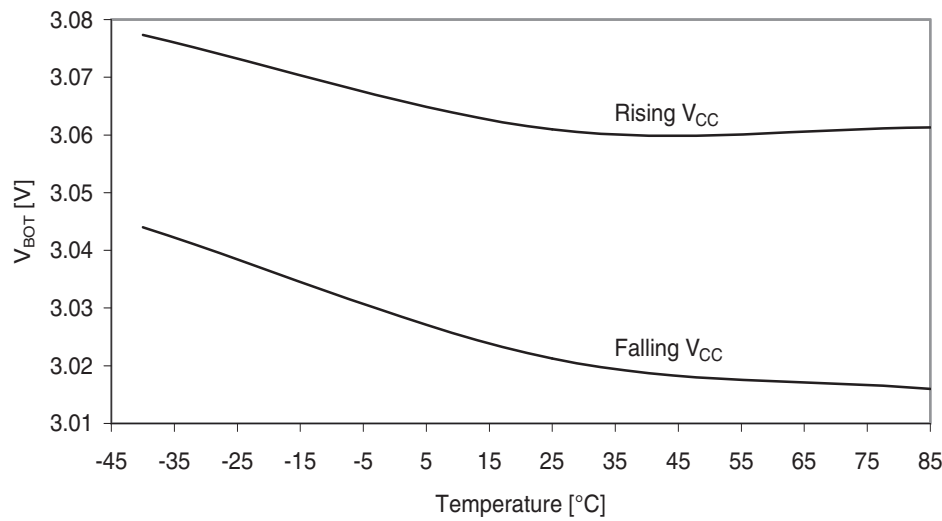


Figure 38-60.BOD thresholds vs. temperature.  
*BOD level = 3.0V.*



### 38.8 External Reset Characteristics

Figure 38-61. Minimum Reset pin pulse width vs.  $V_{CC}$ .

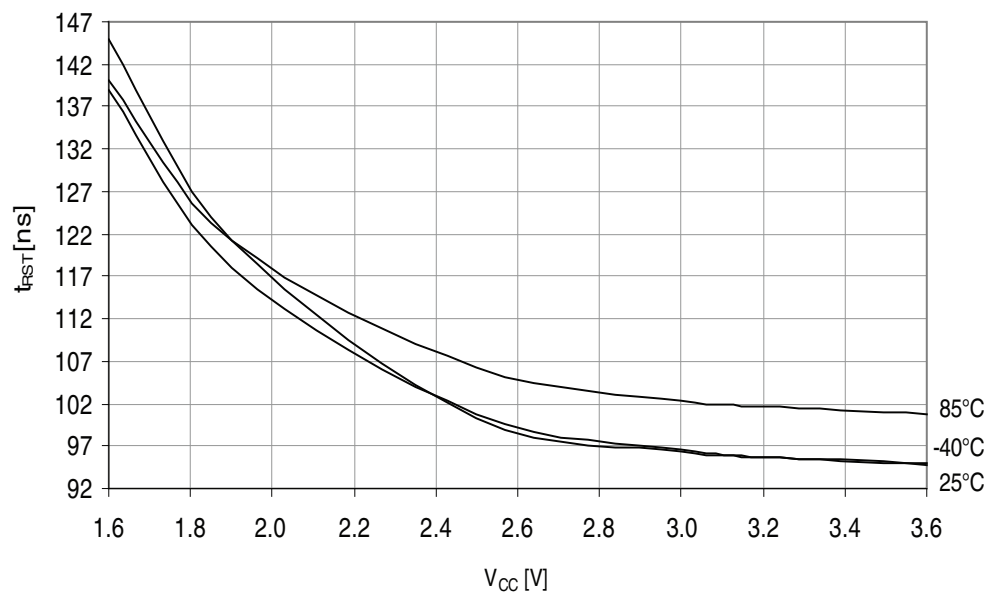
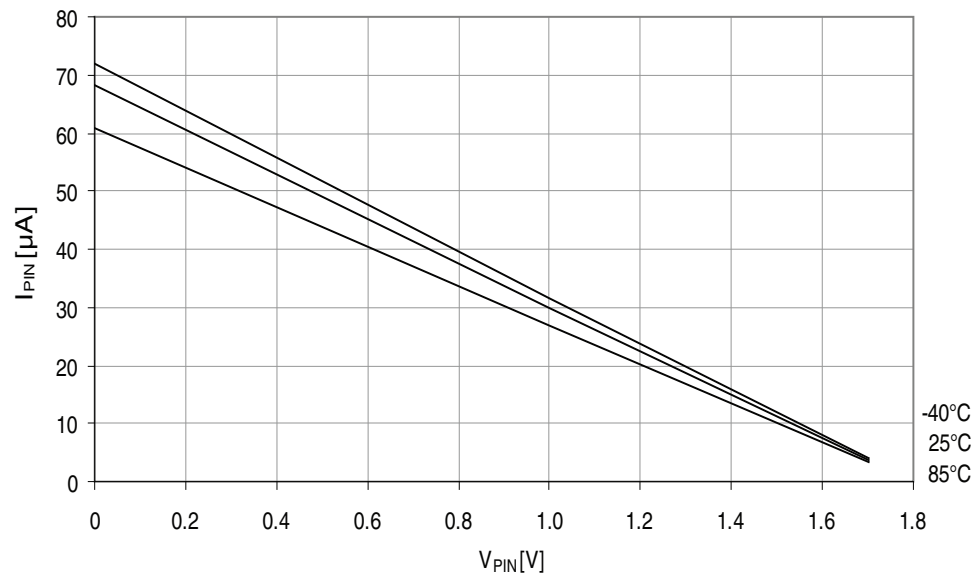


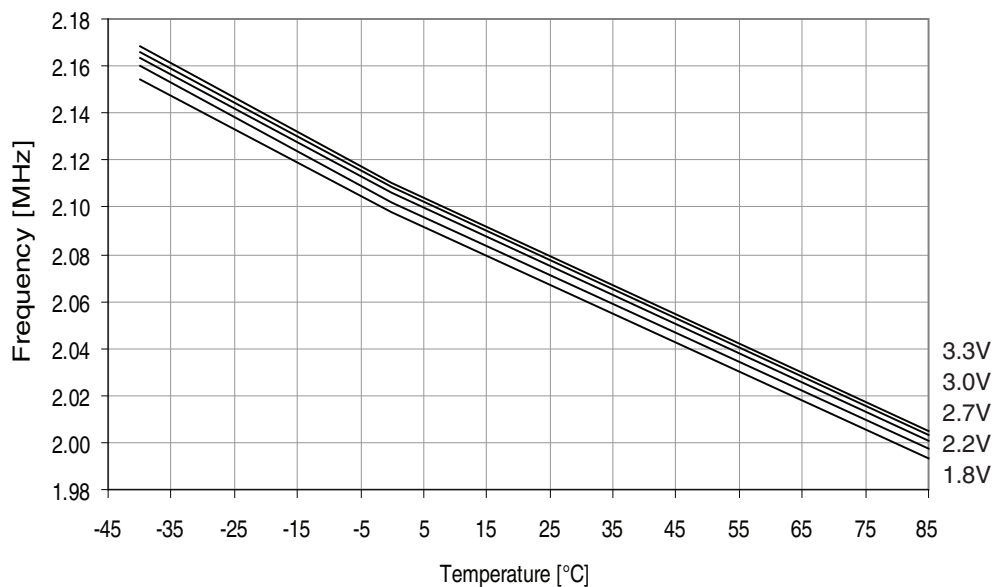
Figure 38-62. Reset pin pull-up resistor current vs. reset pin voltage.

$V_{CC} = 1.8V$ .

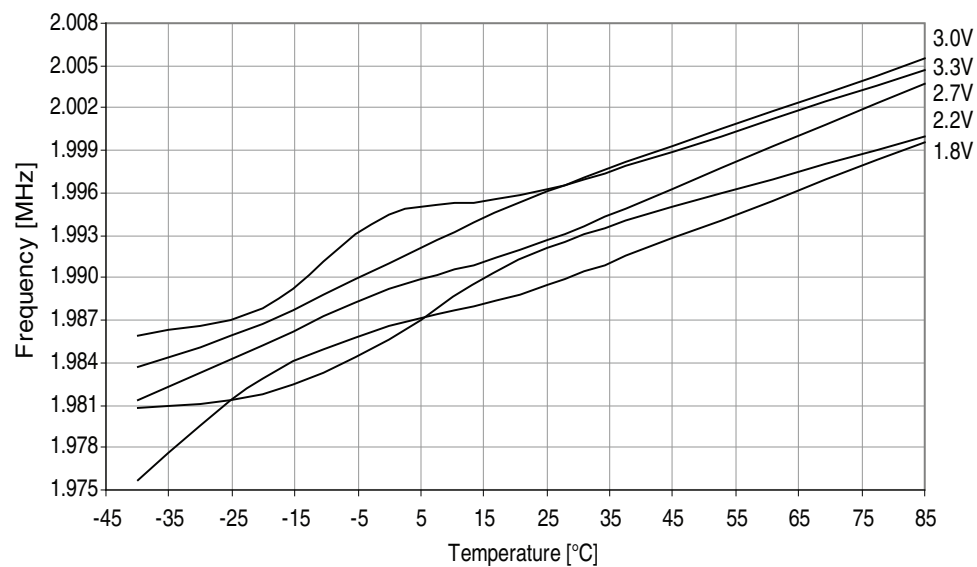


### 38.10.3 2MHz Internal Oscillator

**Figure 38-71. 2MHz internal oscillator frequency vs. temperature.**  
*DPLL disabled.*



**Figure 38-72. 2MHz internal oscillator frequency vs. temperature.**  
*DPLL enabled, from the 32.768kHz internal oscillator .*



## 38.12 PDI characteristics

Figure 38-83. Maximum PDI frequency vs.  $V_{CC}$ .

