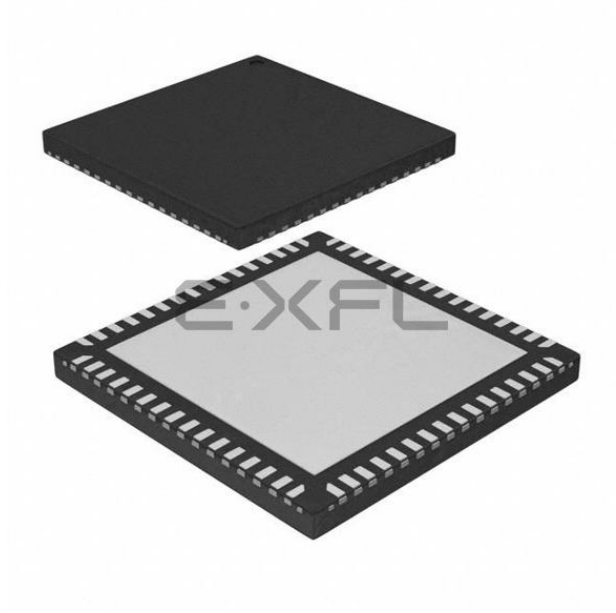


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	47
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3bu-mn

corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 69.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID bytes for Atmel AVR XMEGA A3BU devices.

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega256A3BU	43	98	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, JTAG enable, and JTAG user ID.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-2. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

10.3.1 32kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device.

10.3.2 32.768kHz Calibrated Internal Oscillator

This oscillator provides an approximate 32.768kHz clock. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, which provides both a 32.768kHz output and a 1.024kHz output.

10.3.3 32.768kHz Crystal Oscillator

A 32.768kHz crystal oscillator can be connected between the TOSC1 and TOSC2 pins and enables a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on TOSC2 is available. This oscillator can be used as a clock source for the system clock and RTC, and as the DFLL reference clock.

10.3.4 0.4 - 16MHz Crystal Oscillator

This oscillator can operate in four different modes optimized for different frequency ranges, all within 0.4 - 16MHz.

10.3.5 2MHz Run-time Calibrated Internal Oscillator

The 2MHz run-time calibrated internal oscillator is the default system clock source after reset. It is calibrated during production to provide a default frequency close to its nominal frequency. A DFLL can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy.

10.3.6 32MHz Run-time Calibrated Internal Oscillator

The 32MHz run-time calibrated internal oscillator is a high-frequency oscillator. It is calibrated during production to provide a default frequency close to its nominal frequency. A digital frequency looked loop (DFLL) can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy. This oscillator can also be adjusted and calibrated to any frequency between 30MHz and 55MHz. The production signature row contains 48MHz calibration values intended used when the oscillator is used a full-speed USB clock source.

10.3.7 External Clock Sources

The XTAL1 and XTAL2 pins can be used to drive an external oscillator, either a quartz crystal or a ceramic resonator. XTAL1 can be used as input for an external clock signal. The TOSC1 and TOSC2 pins is dedicated to driving a 32.768kHz crystal oscillator.

10.3.8 PLL with 1x-31x Multiplication Factor

The built-in phase locked loop (PLL) can be used to generate a high-frequency system clock. The PLL has a user-selectable multiplication factor of from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

11.3.3 Power-save Mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.

11.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time.

11.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

14. Battery Backup System

14.1 Features

- Battery Backup voltage supply from dedicated V_{BAT} power pin for:
  - One Ultra Low-power 32-bit Real Time Counter (RTC)
  - One 32.768kHz crystal oscillator with failure detection monitor
  - Two Backup Registers
- Typical power consumption of 500nA with Real Time Counter running
- Automatic switching from main power to battery backup power at:
  - Brown-Out Detection (BOD) reset
- Automatic switching from battery backup power to main power:
  - Device reset after Brown-Out Reset (BOR) is released
  - Device reset after Power-On Reset (POR) and BOR is released

14.2 Overview

Atmel AVR XMEGA family is already running in an ultra low leakage process with power-save current consumption below 2µA with RTC, BOD and watchdog enabled. Still, for some applications where time keeping is important, the system would have one main battery or power source used for day to day tasks, and one backup battery power for the time keeping functionality. The Battery Backup System includes functionality that enable automatic power switching between main power and a battery backup power. Figure 14-1 on page 27 shows an overview of the system.

The Battery Backup Module support connection of a backup battery to the dedicated V_{BAT} power pin. This will ensure power to the 32-bit Real Time Counter, a 32.768kHz crystal oscillator with failure detection monitor and two backup registers, when the main battery or power source is unavailable.

Upon main power loss the device will automatically detect this and the Battery Backup Module will switch to be powered from the V_{BAT} pin. After main power has been restored and both main POR and BOR are released, the Battery Backup Module will automatically switch back to be powered from main power again.

The 32-bit real time counter (RTC) must be clocked from the 1Hz output of a 32.768kHz crystal oscillator connected between the TOSC1 and TOSC2 pins when running from V_{BAT}. For more details on the 32-bit RTC refer to the "RTC32 – 32-bit Real-Time Counter" on page 39".

19. AWeX – Advanced Waveform Extension

19.1 Features

- Waveform output with complementary output from each compare channel
- Four dead-time insertion (DTI) units
  - 8-bit resolution
  - Separate high and low side dead-time setting
  - Double buffered dead time
  - Optionally halts timer during dead-time insertion
- Pattern generation unit creating synchronised bit pattern across the port pins
  - Double buffered pattern generation
  - Optional distribution of one compare channel output across the port pins
- Event controlled fault protection for instant and predictable fault triggering

19.2 Overview

The advanced waveform extension (AWeX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for use with different types of motor control and other power control applications. It enables low- and high side output with dead-time insertion and fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

Each of the waveform generator outputs from the timer/counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a dead-time insertion (DTI) unit that generates the non-inverted low side (LS) and inverted high side (HS) of the WG output with dead-time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The pattern generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the WG output from compare channel A can be distributed to and override all the port pins. When the pattern generator unit is enabled, the DTI unit is bypassed.

The fault protection unit is connected to the event system, enabling any event to trigger a fault condition that will disable the AWeX output. The event system ensures predictable and instant fault reaction, and gives flexibility in the selection of fault triggers.

The AWeX is available for TCC0. The notation of this is AWEXC.

24. SPI – Serial Peripheral Interface

24.1 Features

- Two identical SPI peripherals
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- Lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

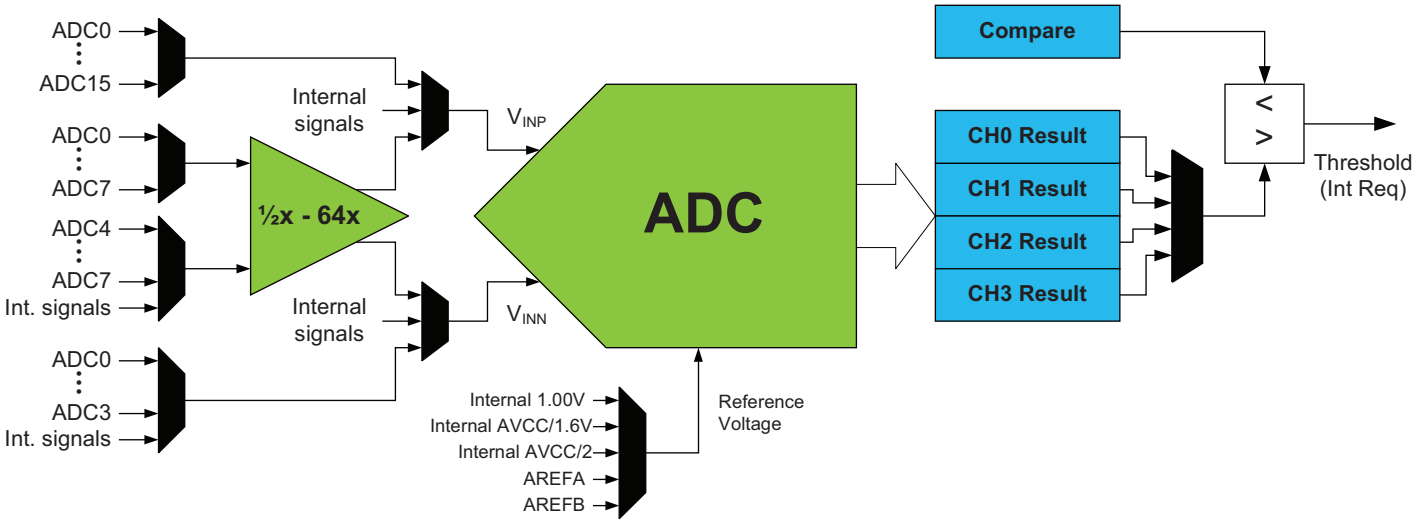
24.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID.

Figure 29-1. ADC overview.



Two inputs can be sampled simultaneously as both the ADC and the gain stage include sample and hold circuits, and the gain stage has 1x gain setting.

Four inputs can be sampled within 1.5µs without any intervention by the application.

The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.5µs for 12-bit to 2.5µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA and PORTB each has one ADC. Notation of these peripherals are ADCA and ADCB, respectively.

34. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in Atmel AVR XMEGA A3BU. For complete register description and summary for each peripheral module, refer to the XMEGA AU Manual.

Table 34-1. Peripheral module address map.

Base Address	Name	Description
0x0000	GPIO	General purpose IO registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32MHz internal oscillator
0x0068	DFLLRC2M	DFLL for the 2MHz internal oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watch-Dog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable Multilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x00C0	AES	AES module
0x00D0	CRC	CRC generator
0x00F0	VBAT	VBAT Battery Backup module
0x0100	DMA	DMA Controller
0x0180	EVSYS	Event System
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0240	ADCB	Analog to Digital Converter on port B
0x0320	DACB	Digital to Analog Converter on port B
0x0380	ACA	Analog Comparator pair on port A
0x0390	ACB	Analog Comparator pair on port B
0x0420	RTC32	32-bit Real Time Counter
0x0480	TWIC	Two-wire Interface on port C
0x04A0	TWIE	Two-wire Interface on port E
0x04D0	USBD	USB Device
0x0600	PORTA	Port A
0x0620	PORTB	Port B

Base Address	Name	Description
0x0640	PORTC	Port C
0x0660	PORTD	Port D
0x0680	PORTE	Port E
0x06A0	PORTF	Port F
0x07E0	PORTR	Port R
0x0800	TCC0	Timer/Counter 0 on port C
0x0840	TCC1	Timer/Counter 1 on port C
0x0880	AWEXC	Advanced Waveform Extension on port C
0x0890	HIRESC	High Resolution Extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08B0	USARTC1	USART 1 on port C
0x08C0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0900	TCD0	Timer/Counter 0 on port D
0x0940	TCD1	Timer/Counter 1 on port D
0x0990	HIRESD	High Resolution Extension on port D
0x09A0	USARTD0	USART 0 on port D
0x09B0	USARTD1	USART 1 on port D
0x09C0	SPID	Serial Peripheral Interface on port D
0x0A00	TCE0	Timer/Counter 0 on port E
0x0A40	TCE1	Timer/Counter 1 on port E
0x0A80	AWEXE	Advanced Waveform Extension on port E
0x0A90	HIRESE	High Resolution Extension on port E
0x0AA0	USARTE0	USART 0 on port E
0x0B00	TCF0	Timer/Counter 0 on port F
0x0B90	HIRESF	High Resolution Extension on port F
0x0BA0	USARTF0	USART 0 on port F

Table 37-5. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				27		
	2MHz int. oscillator				85		
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				270		
		DFLL enabled with 32.768kHz int. osc. as reference			460		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			220		
	Watchdog timer				1.0		
	BOD	Continuous mode			138		
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				100		
	Temperature sensor				95		
	ADC	250ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	DAC	250ksps V_{REF} = Ext ref No load	Normal mode		1.9		
			Low Power mode		1.1		
	AC	High Speed Mode			330		µA
		Low Power Mode			130		
	DMA	615KBps between I/O registers and SRAM			115		
	Timer/Counter				16		
	USART	Rx and Tx enabled, 9600 BAUD			2.5		
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are givenAll parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

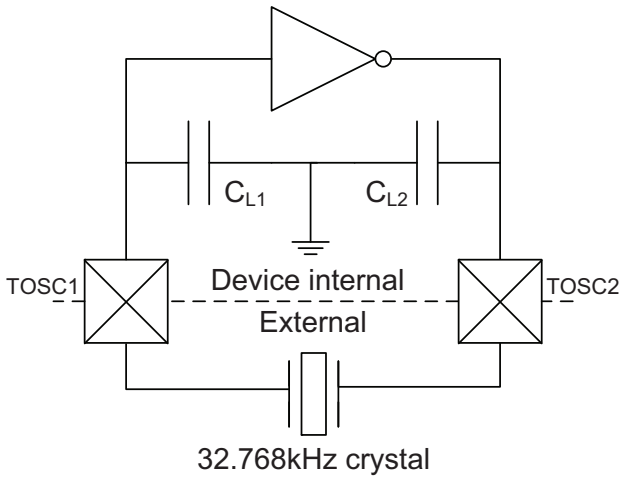
37.15.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 37-31. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.0		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			2.9		
C_L	Parasitic capacitance load			2.0		
	Recommended safety factor	capacitance load matched to crystal specification	3.0			

Note: 1. See Figure 37-4 for definition.

Figure 37-4. TOSC input capacitance.

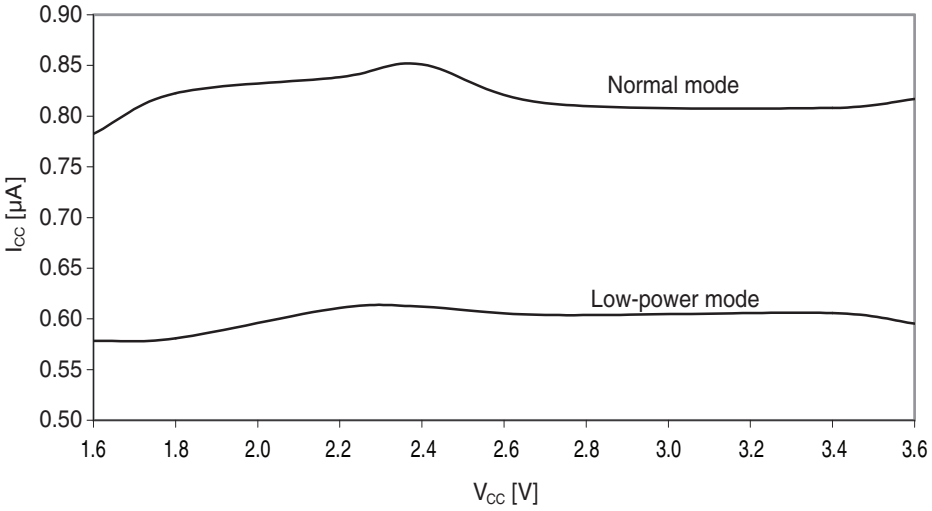


The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

38.1.4 Power-save mode supply current

Figure 38-17.Power-save mode supply current vs. V_{CC}.

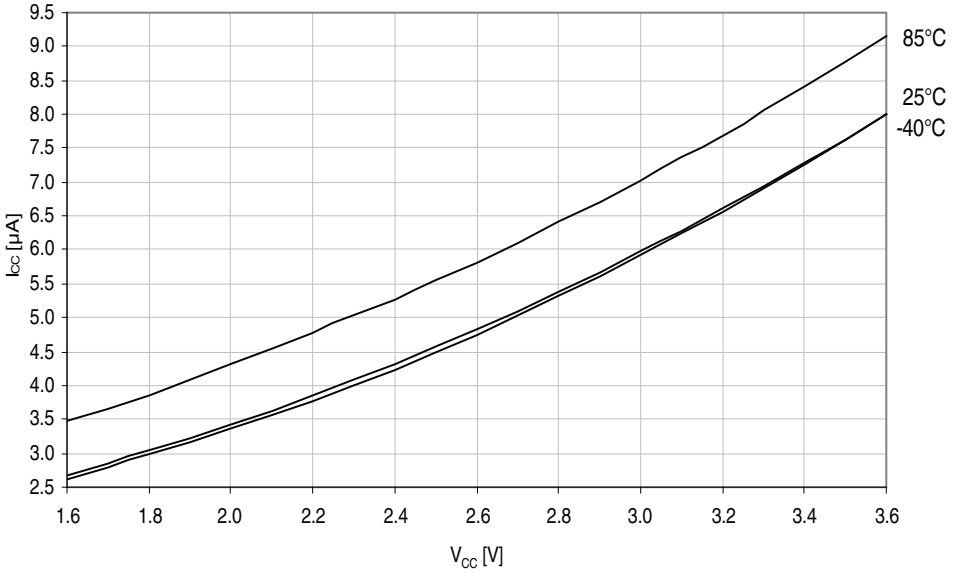
Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.



38.1.5 Standby mode supply current

Figure 38-18.Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.



38.2.2 Output Voltage vs. Sink/Source Current

Figure 38-23.I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

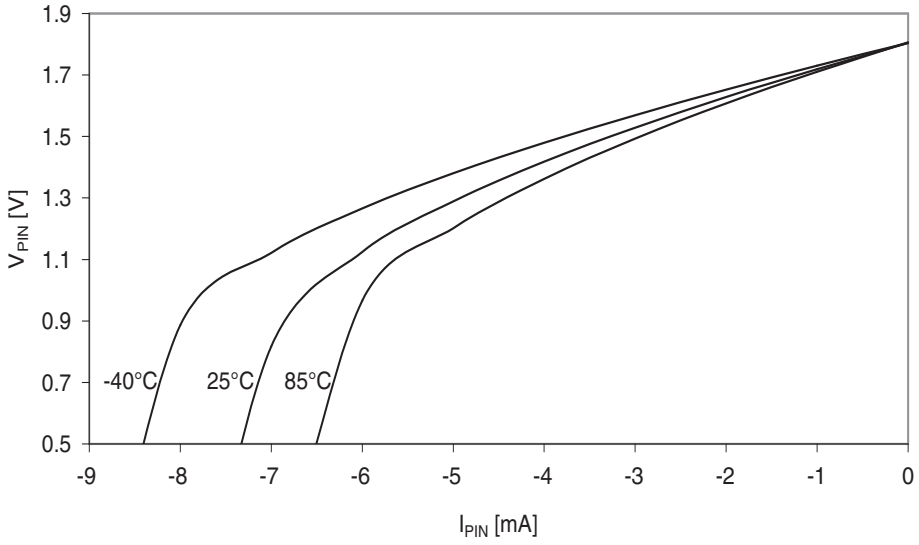
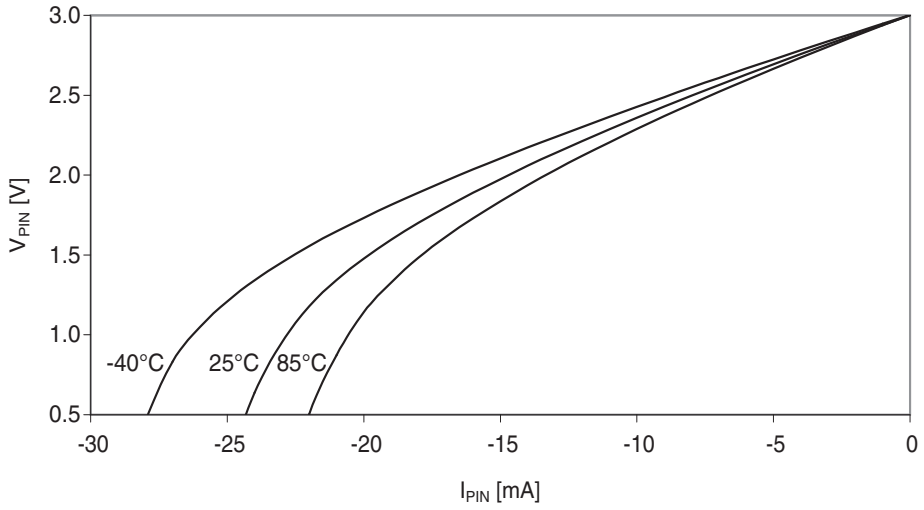


Figure 38-24.I/O pin output voltage vs. source current.
V_{CC} = 3.0V.



38.2.3 Thresholds and Hysteresis

Figure 38-31.I/O pin input threshold voltage vs. V_{CC}.
T = 25°C.

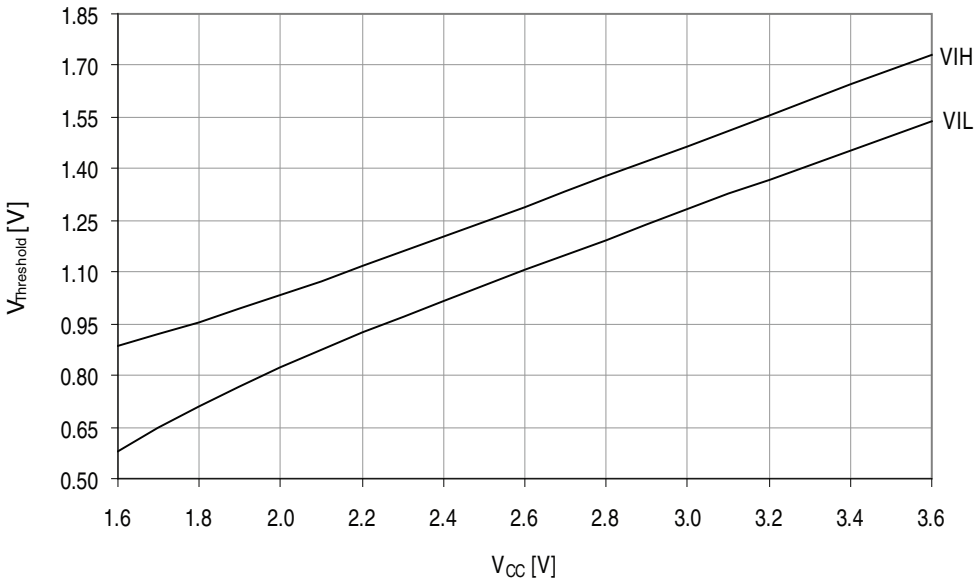


Figure 38-32.I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

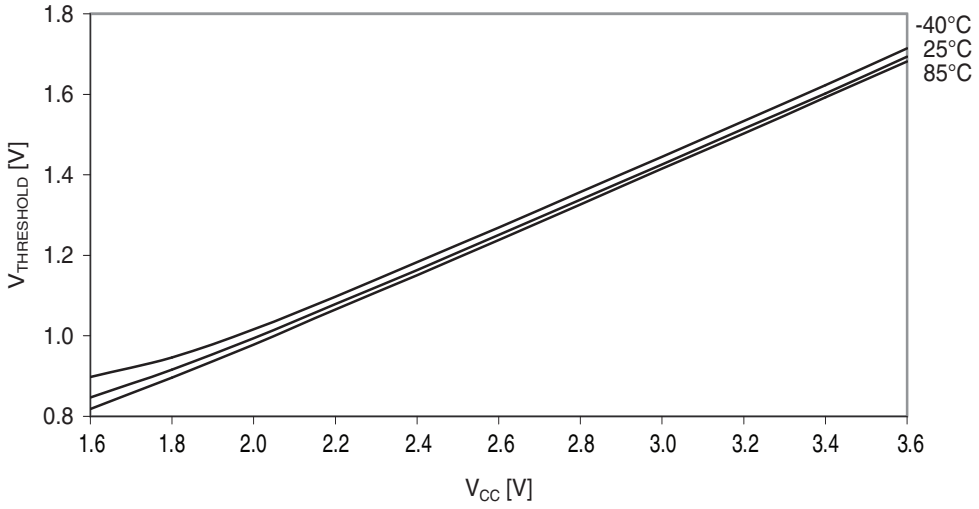
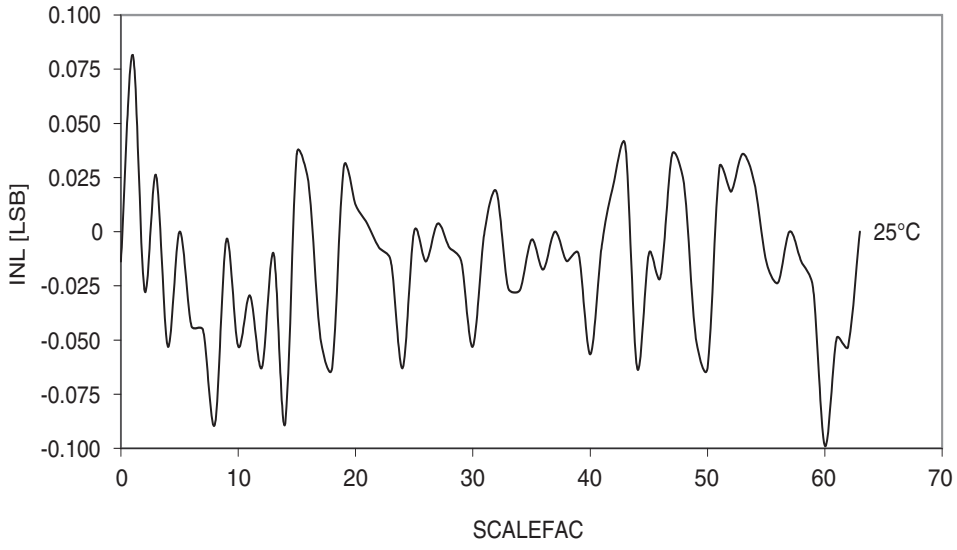


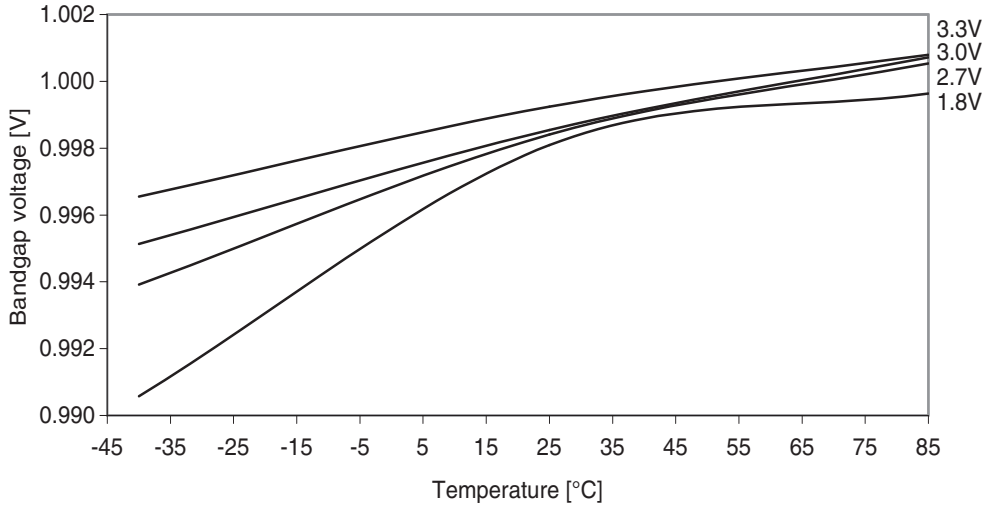
Figure 38-57.Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.



38.6 Internal 1.0V reference Characteristics

Figure 38-58.ADC/DAC Internal 1.0V reference vs. temperature.



38.7 BOD Characteristics

Figure 38-59.BOD thresholds vs. temperature.

BOD level = 1.6V.

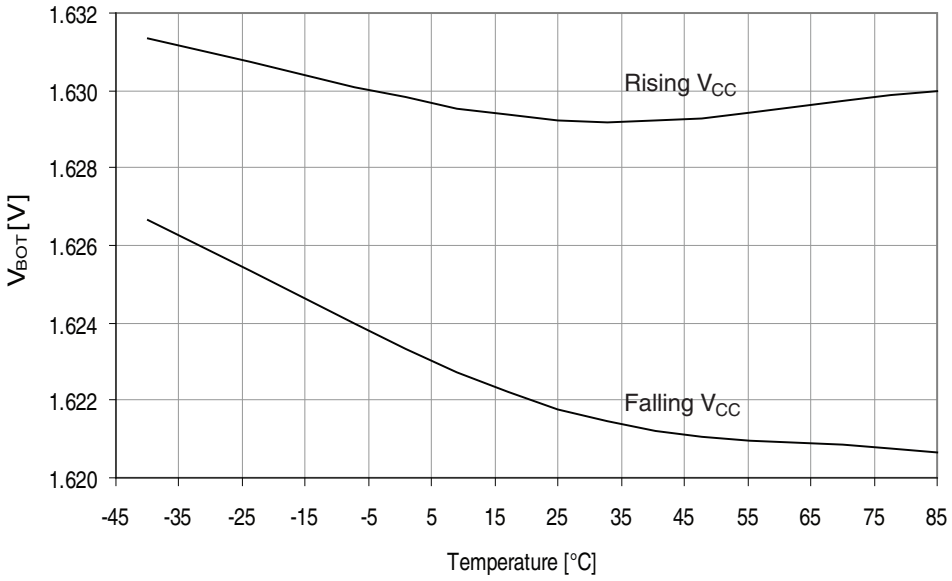


Figure 38-60.BOD thresholds vs. temperature.

BOD level = 3.0V.

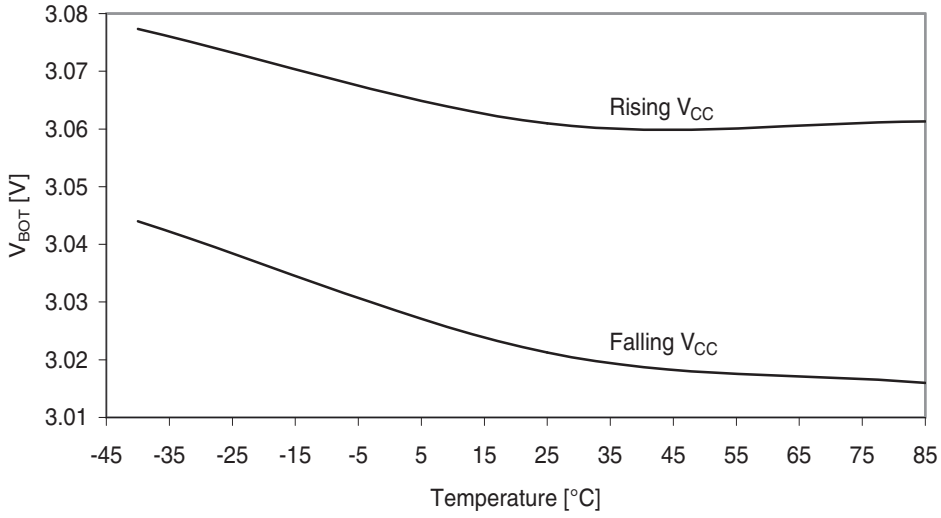


Figure 38-63. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.0V.

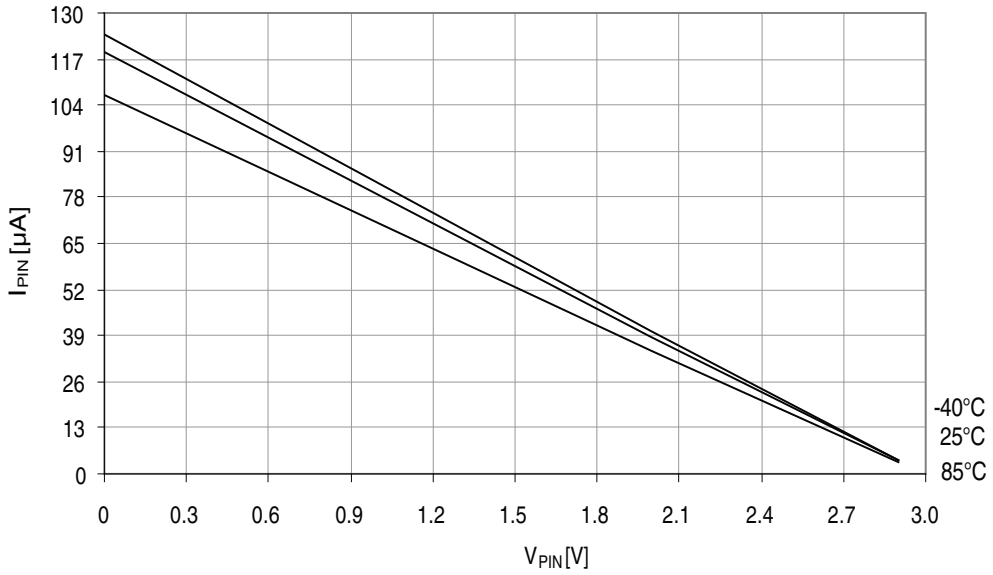


Figure 38-64. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.3V.

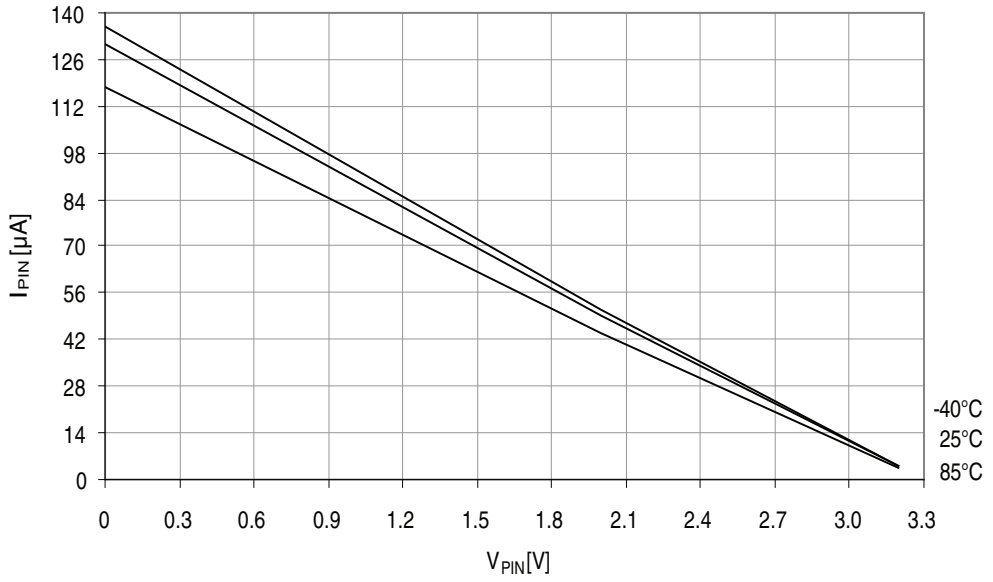


Figure 38-75. 32MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

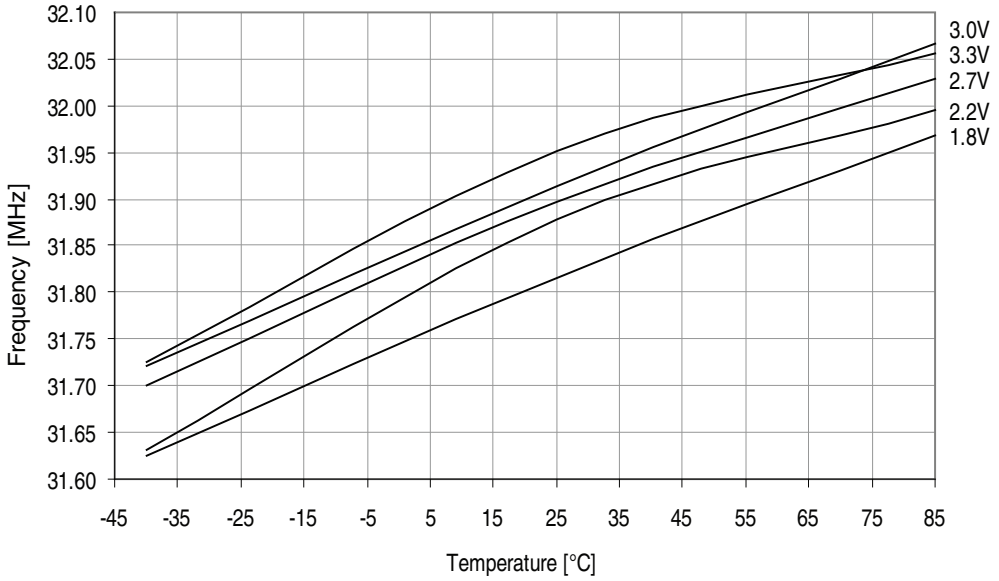
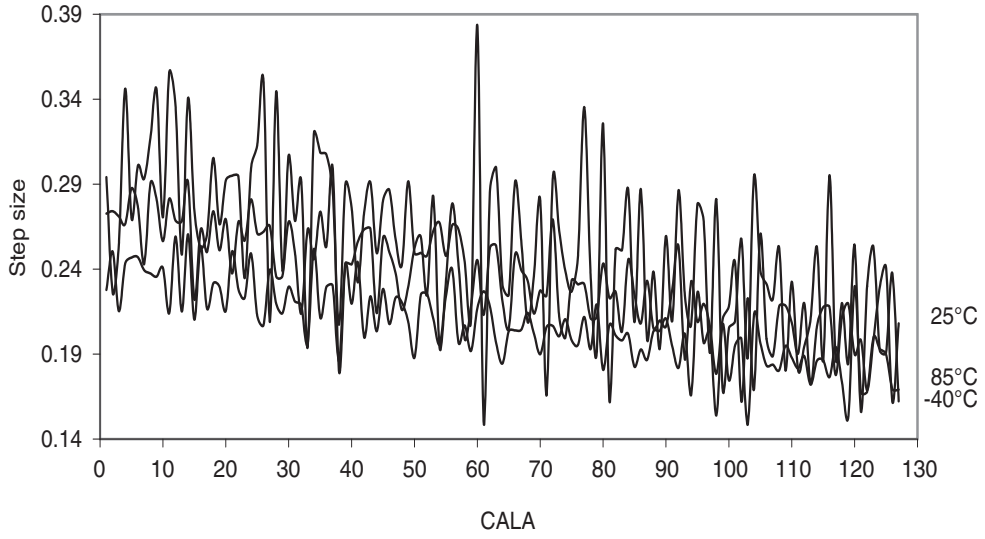


Figure 38-76. 32MHz internal oscillator CALA calibration step size.

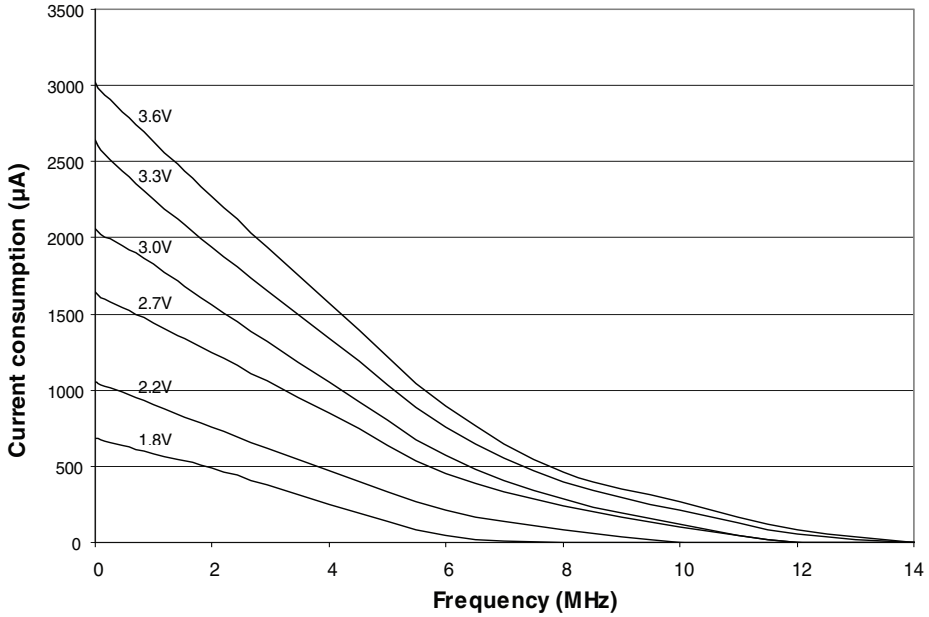
V_{CC} = 3.0V.



Problem fix/Workaround

None, avoid running at low frequenices and use higher frequnecies in compination with sleep modes where possible.

Figure 39-1. Current consumption increase vs. V_{CC} voltage and CPU clock frequency



8. USB Transfer Complete interrupt generated for each IN packet in Multipacket Mode

When multipacket is used, a Transfer Complete interrupt will be generated for each IN packet transferred on USB line instead of just at the end of the multipacket transfer.

Problem fix/Workaround

Ignore interrupt until multipacket is complete.

9. Disabling the USART transmitter does not automatically set the TxD pin direction to input

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

Problem fix/Workaround

The TxD pin direction can be set to input using the Port DIR register. Using Port DIR register to set direction to input only will be immediate and ongoing transmissions will be truncated.

10. AWeX PWM output after fault restarted with wrong values

When recovering from fault state, the PWM output will drive wrong values to the port for up to 2x CLK_{PER} + 1 CLK_{PER4} cycles.

Problem fix/Workaround

If the glitch can not be tolerated or not filtered out by external components the following sequence can be used in Latched Mode for restaring without glitch: