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Details	
Product Status	Obsolete
Applications	USB Host/Slave Controller
Core Processor	-
Program Memory Type	-
Controller Series	USB-Hosts
RAM Size	256 x 8
Interface	USB
Number of I/O	8
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 65°C
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.51x11.51)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sl811hs

Data Port, Microprocessor Interface

The SL811HS microprocessor interface provides an 8-bit bidirectional data path along with appropriate control lines to interface to external processors or controllers. Programmed I/O or memory mapped I/O designs are supported through the 8-bit interface, chip select, read and write input strobes, and a single address line, A0.

Access to memory and control register space is a simple two step process, requiring an address Write with A0 = '0', followed by a register/memory Read or Write cycle with address line A0 = '1'.

In addition, a DMA bidirectional interface in slave mode is available with handshake signals such as nDRQ, nDACK, nWR, nRD, nCS and INTRQ.

The SL811HS WRITE or READ operation terminates when either nWR or nCS goes inactive. For devices interfacing to the SL811HS that deactivate the Chip Select nCS before the Write nWR, the data hold timing must be measured from the nCS and will be the same value as specified. Therefore, both Intel®- and Motorola-type CPUs work easily with the SL811HS without any external glue logic requirements.

DMA Controller (slave mode only)

In applications that require transfers of large amounts of data such as scanner interfaces, the SL811HS provides a DMA interface. This interface supports DMA READ or WRITE transfers to the SL811HS internal RAM buffer, it is done through the microprocessor data bus via two control lines (nDRQ - Data Request and nDACK - Data Acknowledge), along with the nWR line and controls the data flow into the SL811HS. The SL811HS has a count register that allows selection of programmable block sizes for DMA transfer. The control signals, both nDRQ and nDACK, are designed for compatibility with standard DMA interfaces.

Interrupt Controller

The SL811HS interrupt controller provides a single output signal (INTRQ) that is activated by a number of programmable events that may occur as result of USB activity. Control and status registers are provided to allow the user to select single or multiple events, which generate an interrupt (assert INTRQ) and let the user view interrupt status. The interrupts are cleared by writing to the Interrupt Status Register.

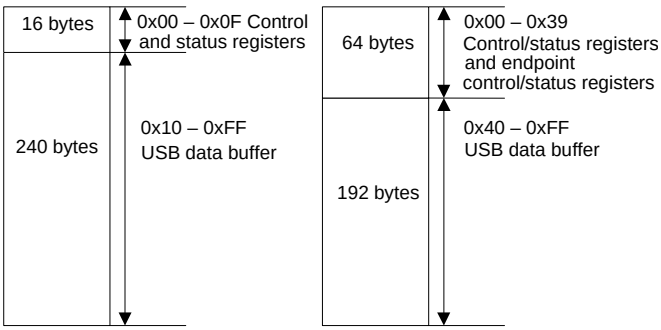
Buffer Memory

The SL811HS contains 256 bytes of internal memory used for USB data buffers, control registers, and status registers. When in master mode (host mode), the memory is defined where the first 16 bytes are registers and the remaining 240 bytes are used for USB data buffers. When in slave mode (peripheral mode), the first 64 bytes are used for the four endpoint control and status registers along with the various other registers. This leaves 192 bytes of endpoint buffer space for USB data transfers.

Access to the registers and data memory is through the 8-bit external microprocessor data bus, in either indexed or direct addressing. Indexed mode uses the Auto Address Increment mode described in Auto Address Increment Mode, where direct addressing is used to READ/WRITE to an individual address.

USB transactions are automatically routed to the memory buffer that is configured for that transfer. Control registers are provided so that pointers and block sizes in buffer memory are determined and allocated.

Figure 1. Memory Map



Auto Address Increment Mode

The SL811HS supports auto increment mode to reduce READ and WRITE memory cycles. In this mode, the microcontroller needs to set up the address only once. Whenever any subsequent DATA is accessed, the internal address counter advances to the next address location.

Auto Address Increment Example. To fill the data buffer that is configured for address 10h, follow these steps:

1. Write 10h to SL811HS with A0 LOW. This sets the memory address that is used for the next operation.
2. Write the first data byte into address 10h by doing a write operation with A0 HIGH. An example is a Get Descriptor; the first byte that is sent to the device is 80h (bmRequestType) so you would write 80h to address 10h.
3. Now the internal RAM address pointer is set to 11h. So, by doing another write with A0 HIGH, RAM address location 11h is written with the data. Continuing with the Get Descriptor example, a 06h is written to address 11h for the bRequest value.
4. Repeat Step 3 until all the required bytes are written as necessary for a transfer. If auto-increment is not used, you write the address value each time before writing the data as shown in Step 1.

The advantage of auto address increment mode is that it reduces the number of required SL811HS memory READ/WRITE cycles to move data to/from the device. For example, transferring 64 bytes of data to/from SL811HS, using auto increment mode, reduces the number of cycles to 1 address WRITE and 64 READ/WRITE data cycles, compared to 64 address writes and 64 data cycles for random access.

PLL Clock Generator

Either a 12 MHz or a 48 MHz external crystal is used with the SL811HS[1]. Two pins, X1 and X2, are provided to connect a low cost crystal circuit to the device as shown in Figure 2 and Figure 3. Use an external clock source if available in the application instead of the crystal circuit by connecting the source directly to the X1 input pin. When a clock is used, the X2 pin is not connected.

When the CM pin is tied to a logic 0, the internal PLL is bypassed so the clock source must meet the timing requirements specified by the USB specification.

Figure 2. Full Speed 48 MHz Crystal Circuit

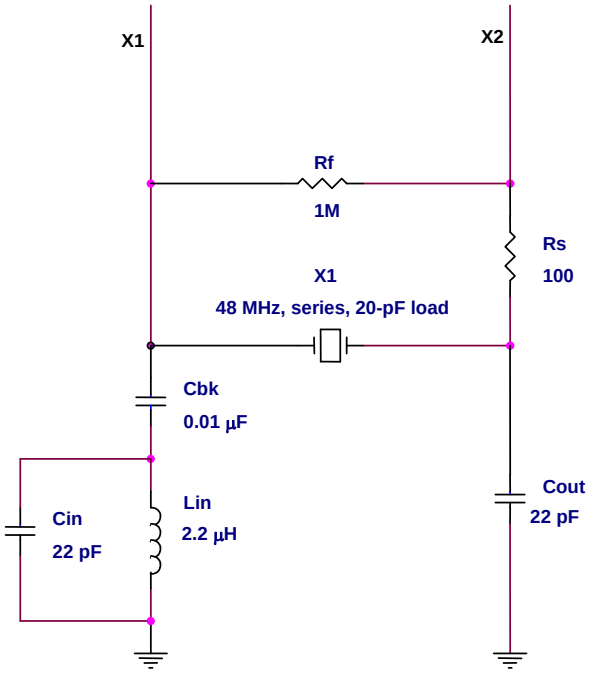
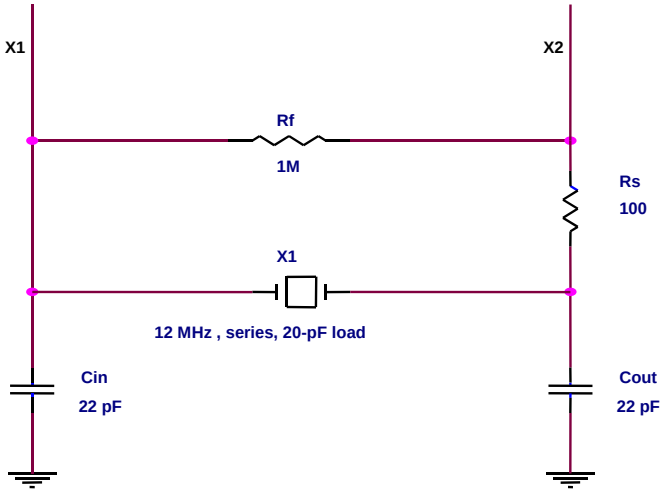


Figure 3. Optional 12 MHz Crystal Circuit



Typical Crystal Requirements

The following are examples of 'typical requirements.' Note that these specifications are generally found as standard crystal values and are less expensive than custom values. If crystals are used in series circuits, load capacitance is not applicable. Load capacitance of parallel circuits is a requirement. 48 MHz third overtone crystals require the Cin/Lin filter to guarantee 48 MHz operation.

12 MHz Crystals:

Frequency Tolerance:	±100 ppm or better
Operating Temperature Range:	0°C to 70°C
Frequency:	12 MHz
Frequency Drift over Temperature:	± 50 ppm
ESR (Series Resistance):	60Ω
Load Capacitance:	10 pF min.
Shunt Capacitance:	7 pF max.
Drive Level:	0.1–0.5 mW
Operating Mode:	fundamental

48 MHz Crystals:

Frequency Tolerance:	±100 ppm or better
Operating Temperature Range:	0°C to 70°C
Frequency:	48 MHz
Frequency Drift over Temperature:	± 50 ppm
ESR (Series Resistance):	40 Ω
Load Capacitance:	10 pF min.
Shunt Capacitance:	7 pF max.
Drive Level:	0.1–0.5 mW
Operating Mode:	third overtone

USB Transceiver

The SL811HS has a built in transceiver that meets USB Specification 1.1. The transceiver is capable of transmitting and receiving serial data at USB full speed (12 Mbits) and low speed (1.5 Mbits). The driver portion of the transceiver is differential while the receiver section is comprised of a differential receiver and two single-ended receivers. Internally, the transceiver interfaces to the Serial Interface Engine (SIE) logic. Externally, the transceiver connects to the physical layer of the USB.

SL811HS Registers

Operation and control of the SL811HS is managed through internal registers. When operating in Master/Host mode, the first 16 address locations are defined as register space. In Slave/Peripheral mode, the first 64 bytes are defined as register space. The register definitions vary greatly between each mode of operation and are defined separately in this document (section "SL811HS Master (Host) Mode Registers" on page 4 describes Host register definitions, while section

Note
1. CM (Clock Multiply) pin of the SL811HS must be tied to GND when 48 MHz crystal circuit or 48 MHz clock source is used.

"SL811HS Slave Mode Registers" on page 12 describes Slave register definitions). Access to the registers are through the microprocessor interface similar to normal RAM accesses (see "Bus Interface Timing Requirements" on page 26) and provide control and status information for USB transactions.

Any write to control register 0FH enables the SL811HS full features bit. This is an internal bit of the SL811HS that enables additional features.

Table 1 shows the memory map and register mapping of the SL811HS in master/host mode.

SL811HS Master (Host) Mode Registers

Table 1. SL811HS Master (Host) Register Summary

Register Name SL811HS	SL811HS (hex) Address
USB-A Host Control Register	00h
USB-A Host Base Address	01h
USB-A Host Base Length	02h
USB-A Host PID, Device Endpoint (Write)/USB Status (Read)	03h
USB-A Host Device Address (Write)/Transfer Count (Read)	04h
Control Register 1	05h
Interrupt Enable Register	06h
Reserved Register	Reserved
USB-B Host Control Register	08h
USB-B Host Base Address	09h
USB-B Host Base Length	0Ah
USB-B Host PID, Device Endpoint (Write)/USB Status (Read)	0Bh
USB-B Host Device Address (Write)/Transfer Count (Read)	0Ch
Status Register	0Dh
SOF Counter LOW (Write)/HW Revision Register (Read)	0Eh
SOF Counter HIGH and Control Register 2	0Fh
Memory Buffer	10H-FFh

The registers in the SL811HS are divided into two major groups. The first group is referred to as USB Control registers. These registers enable and provide status for control of USB transactions and data flow. The second group of registers provides control and status for all other operations.

Register Values on Power Up and Reset

The following registers initialize to zero on power up and reset:

- USB-A/USB-B Host Control Register [00H, 08H] bit 0 only
- Control Register 1 [05H]
- USB Address Register [07H]
- Current Data Set/Hardware Revision/SOF Counter LOW Register [0EH]

All other register's power up and reset in an unknown state and firmware for initialization.

USB Control Registers

Communication and data flow on the USB bus uses the SL811HS' USB A-B Control registers. The SL811HS communicates with any USB Device function and any specific endpoint via the USB-A or USB-B register sets.

The USB A-B Host Control registers are used in an overlapped configuration to manage traffic on the USB bus. The USB Host Control register also provides a means to interrupt an external CPU or microcontroller when one of the USB protocol transactions is completed. Table 1 and Table 2 show the two sets of USB Host Control registers, the 'A' set and 'B' set. The two register sets allow for overlapping operation. When one set of parameters is being set up, the other is transferring. On completion of a transfer to an endpoint, the next operation is controlled by the other register set.

Note The USB-B register set is used only when SL811HS mode is enabled by initializing register 0FH.

The SL811HS USB Host Control has two groups of five registers each which map in the SL811HS memory space. These registers are defined in the following tables.

SL811HS Host Control Registers.

Table 2. SL811HS Host Control Registers

Register Name SL811H	SL811HS (hex) Address
USB-A Host Control Register	00h
USB-A Host Base Address	01h
USB-A Host Base Length	02h
USB-A Host PID, Device Endpoint (Write)/USB Status (Read)	03h
USB-A Host Device Address (Write)/Transfer Count (Read)	04h
USB-B Host Control Register	08h
USB-B Host Base Address	09h
USB-B Host Base Length	0Ah
USB-B Host PID, Device Endpoint (Write)/USB Status (Read)	0Bh
USB-B Host Device Address (Write)/Transfer Count (Read)	0Ch

USB-A/USB-B Host Base Length [Address = 02h, 0Ah].

Table 5. USB-A / USB-B Host Base Length Definition [Address 02h, 0Ah]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HBL7	HBL6	HBL5	HBL4	HBL3	HBL2	HBL1	HBL0

The USB A/B Host Base Length register contains the maximum packet size transferred between the SL811HS and a slave USB peripheral. Essentially, this designates the largest packet size that is transferred by the SL811HS. Base Length designates the size of data packet sent or received. For example, in full speed BULK mode, the maximum packet length is 64 bytes. In ISO mode, the maximum packet length is 1023 bytes since the SL811HS only has an 8-bit length; the maximum packet size for the ISO mode using the SL811HS is 255 – 16 bytes (register space). When the Host Base length register is set to zero, a Zero-Length packet is transmitted.

USB-A/USB-B USB Packet Status (Read) and Host PID, Device Endpoint (Write) [Address = 03h, 0Bh]. This register has two modes dependent on whether it is read or written. When read, this register provides packet status and contains information relative to the last packet that has been received or transmitted. This register is not valid for reading until after the Done interrupt occurs, which causes the register to update.

Table 6. USB-A/USB-B USB Packet Status Register Definition when READ [Address 03h, 0Bh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STALL	NAK	Overflow	Setup	Sequence	Time-out	Error	ACK

Bit Position	Bit Name	Function
7	STALL	Slave device returned a STALL.
6	NAK	Slave device returned a NAK.
5	Overflow	Overflow condition - maximum length exceeded during receives. For underflow, see USB-A/USB-B Host Transfer Count Register (Read), USB Address (Write) [Address = 04h, 0Ch] on page 7.
4	Setup	This bit is not applicable for Host operation since a SETUP packet is generated by the host.
3	Sequence	Sequence bit. ’0’ if DATA0, ’1’ if DATA1.
2	Time-out	Timeout occurred. A timeout is defined as 18-bit times without a device response (in full speed).
1	Error	Error detected in transmission. This includes CRC5, CRC16, and PID errors.
0	ACK	Transmission Acknowledge.

When written, this register provides the PID and Endpoint information to the USB SIE engine used in the next transaction. All 16 Endpoints can be addressed by the SL811HS.

Table 7. USB-A / USB-B Host PID and Device Endpoint Register when WRITTEN [Address 03h, 0Bh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PID3	PID2	PID1	PID0	EP3	EP2	EP1	EP0

PID[3:0]: 4-bit PID Field (See Table Below), EP[3:0]: 4-bit Endpoint Value in Binary.

PID TYPE	D7-D4
SETUP	1101 (D Hex)
IN	1001 (9 Hex)
OUT	0001 (1 Hex)
SOF	0101 (5 Hex)
PREAMBLE	1100 (C Hex)
NAK	1010 (A Hex)
STALL	1110 (E Hex)
DATA0	0011 (3 Hex)
DATA1	1011 (B Hex)

USB-A/USB-B Host Transfer Count Register (Read), USB Address (Write) [Address = 04h, 0Ch]. This register has two different functions depending on whether it is read or written. When read, this register contains the number of bytes remaining (from Host Base Length value) after a packet is transferred. For example, if the Base Length register is set to 0x040 and an IN Token was sent to the peripheral device. If, after the transfer is complete, the value of the Host Transfer Count is 0x10, the number of bytes actually transferred is 0x30. This is considered as an underflow indication.

Table 8. USB-A / USB-B Host Transfer Count Register when READ [Address 04h, 0Ch]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HTC7	HTC6	HTC5	HTC4	HTC3	HTC2	HTC1	HTC0

When written, this register contains the USB Device Address with which the Host communicates.

Table 9. USB-A / USB-B USB Address when WRITTEN [Address 04h, 0Ch]

Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
0	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA6-DA0 Device address, up to 127 devices can be addressed.

DA7 Reserved bit must be set to zero.

SL811HS Control Registers

The next set of registers are the Control registers and control more of the operation of the chip instead of USB packet type of transfers. Table 10 is a summary of the control registers.

Table 10. SL811HS Control Registers Summary

Register Name SL811H	SL811HS (hex) Address
Control Register 1	05h
Interrupt Enable Register	06h
Reserved Register	07h
Status Register	0Dh
SOF Counter LOW (Write)/HW Revision Register (Read)	0Eh
SOF Counter HIGH and Control Register 2	0Fh
Memory Buffer	10h-FFh

Control Register 1 [Address = 05h]. The Control Register 1 enables/disables USB transfer operation with control bits defined as follows.

Table 11. Control Register 1 [Address 05h]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Suspend	USB Speed	J-K state force	USB Engine Reset	Reserved	Reserved	SOF ena/dis

Bit Position	Bit Name	Function
7	Reserved	'0'
6	Suspend	'1' = enable, '0' = disable.
5	USB Speed	'0' setup for full speed, '1' setup low speed.
4	J-K state force	See Table 12.
3	USB Engine Reset	USB Engine reset = '1'. Normal set '0'. When a device is detected, the first thing that to do is to send it a USB Reset to force it into its default address of zero. The USB 2.0 specification states that for a root hub a device must be reset for a minimum of 50 mS.
2	Reserved	Some existing firmware examples set bit 2, but it is not necessary.
1	Reserved	'0'
0	SOF ena/dis	'1' = enable auto Hardware SOF generation; '0' = disable. In the SL811HS, bit 0 is used to enable hardware SOF autogeneration. The generation of SOFs continues when set to '0', but SOF tokens are not output to USB.

At powe -up this register is cleared to all zeros.

Low-power Modes [Bit 6 Control Register, Address 05h]

When bit 6 (Suspend) is set to '1', the power of the transmit transceiver is turned off, the internal RAM is in suspend mode, and the internal clocks are disabled.

Note Any activity on the USB bus (i.e., K-State, etc.) resumes normal operation. To resume normal operation from the CPU side, a Data Write cycle (i.e., A0 set HIGH for a Data Write cycle) is done. This is a special case and not a normal direct write where the address is first written and then the data. To resume normal operation from the CPU side, you must do a Data Write cycle only.

Low Speed/Full Speed Modes [Bit 5 Control Register 1, Address 05h]

The SL811HS is designed to communicate with either full- or low speed devices. At power up bit 5 is LOW, i.e., for full speed. There are two cases when communicating with a low speed device. When a low speed device is connected directly to the SL811HS, bit 5 of Register 05h is set to '1' and bit 6 of register 0Fh, Polarity Swap, is set to '1' in order to change the polarity of D+ and D–. When a low speed device is connected via a HUB to SL811HS, bit 5 of Register 05h is set to '0' and bit 6 of register 0Fh is set to '0' in order to keep the polarity of D+ and D– for full speed. In addition, make sure that bit 7 of USB-A/USB-B Host Control registers [00h, 08h] is set to '1' for preamble generation.

J-K Programming States [Bits 4 and 3 of Control Register 1, Address 05h]

The J-K force state control and USB Engine Reset bits are used to generate a USB reset condition. Forcing K-state is used for Peripheral device remote wake up, resume, and other modes. These two bits are set to zero on power up.

Table 12. Control Register 1 Address 05h – Bits 3 and 4

Bit 4	Bit 3	Function
0	0	Normal operating mode
0	1	Force USB Reset, D+ and D– are set LOW (SE0)
1	0	Force J-State, D+ set HIGH, D– set LOW[2]
1	1	Force K-State, D– set HIGH, D+ set LOW[3]

USB Reset Sequence

After a device is detected, write 08h to the Control register (05h) to initiate the USB reset, then wait for the USB reset time (root hub should be 50 ms) and additionally some types of devices such as a Forced J-state. Lastly, set the Control register (05h) back to 0h. After the reset is complete, the auto-SOF generation is enabled.

SOF Packet Generation

The SL811HS automatically computes the frame number and CRC5 by hardware. No CRC or SOF generation is required by external firmware for the SL811HS, although it can be done by sending an SOF PID in the Host PID, Device Endpoint register.

To enable SOF generation, assuming host mode is configured:

1. Set up the SOF interval in registers 0x0F and 0x0E.
2. Enable the SOF hardware generation in this register by setting bit 0 = '1'.
3. Set the Arm bit in the USB-A Host Control register.

Notes
2. Force K-State for low speed.
3. Force J-State for low speed.

SL811HS Slave Mode Registers

Table 19. SL811HS Slave/Peripheral Mode Register Summary

Register Name	Endpoint specific register addresses							
	EP 0 – A	EP 0 - B	EP 1 – A	EP 1 - B	EP 2 - A	EP 2 - B	EP 3 - A	EP 3 - B
EP Control Register	00h	08h	10h	18h	20h	28h	30h	0x38
EP Base Address Register	01h	09h	11h	19h	21h	29h	31h	0x39
EP Base Length Register	02h	0Ah	12h	1Ah	22h	2Ah	0x32	0x3A
EP Packet Status Register	03h	0Bh	13h	1Bh	23h	2Bh	0x33	0x3B
EP Transfer Count Register	04h	0Ch	14h	1Ch	24h	2Ch	0x34	0x3C
Register Name		**Miscellaneous register addresses**						
Control Register 1	05h	Interrupt Status Register			0Dh			
Interrupt Enable Register	06h	Current Data Set Register			0Eh			
USB Address Register	07h	Control Register 2			0Fh			
SOF Low Register (read only)	15h	Reserved			1Dh1Fh			
SOF High Register (read only)	16h	Reserved			25h-27h			
Reserved	17h	Reserved			2Dh-2Fh			
DMA Total Count Low Register	35h							
DMA Total Count High Register	36h							
Reserved	37h							
Memory Buffer	40h – FFh							

When in slave mode, the registers in the SL811HS are divided into two major groups. The first group contains Endpoint registers that manage USB control transactions and data flow. The second group contains the USB Registers that provide the control and status information for all other operations.

Endpoint Registers

Communication and data flow on USB is implemented using endpoints. These uniquely identifiable entities are the terminals of communication flow between a USB host and USB devices. Each USB device is composed of a collection of independently operating endpoints. Each endpoint has a unique identifier, which is the Endpoint Number. For more information, see USB Specification 1.1 section 5.3.1.

The SL811HS supports four endpoints numbered 0–3. Endpoint 0 is the default pipe and is used to initialize and generically manipulate the device to configure the logical device as the Default Control Pipe. It also provides access to the device's configuration information, allows USB status and control access, and supports control transfers.

Endpoints 1–3 support Bulk, Isochronous, and Interrupt transfers. Endpoint 3 is supported by DMA. Each endpoint has two sets of registers—the 'A' set and the 'B' set. This allows overlapped operation where one set of parameters is set up and the other is transferring. Upon completion of a transfer to an endpoint, the ‘next data set’ bit indicates whether set 'A' or set 'B' is used next. The ‘armed’ bit of the next data set indicates whether the SL811HS is ready for the next transfer without interruption.

Endpoints 0–3 Register Addresses

Each endpoint set has a group of five registers that are mapped within the SL811HS memory. The register sets have address assignments as shown in the following table.

Table 20. Endpoints 0–3 Register Addresses

Endpoint Register Set	Address (in Hex)
Endpoint 0 – a	00 - 04
Endpoint 0 – b	08 - 0C
Endpoint 1 – a	10 - 14
Endpoint 1 – b	18 - 1C
Endpoint 2 – a	20 - 24
Endpoint 2 – b	28 - 2C
Endpoint 3 – a	30 - 34
Endpoint 3 – b	38 - 3C

For each endpoint set (starting at address Index = 0), the registers are mapped as shown in the following table.

Table 21. Register Address Map

Endpoint Register Sets (for Endpoint *n* starting at register position *Index=0*)	
Index	Endpoint *n* Control
Index + 1	Endpoint *n* Base Address
Index + 2	Endpoint *n* Base Length
Index + 3	Endpoint *n* Packet Status
Index + 4	Endpoint *n* Transfer Count

Endpoint Packet Status [Address a = (EP# * 10h)+3, b = (EP# * 10h)+Bh]. The packet status contains information relative to the packet that is received or transmitted. The register is defined as follows:

Table 25. Endpoint Packet Status Reg [Address EP0a/b:03h/0Bh, EP1a/b:13h/1Bh, EP2a/b:23h/2Bh, EP3a/b:33h/3Bh]

7	6	5	4	3	2	1	0
Reserved	Reserved	Overflow	Setup	Sequence	Time-out	Error	ACK

Bit Position	Bit Name	Function
7	Reserved	Not applicable.
6	Reserved	Not applicable.
5	Overflow	Overflow condition - maximum length exceeded during receives. This is considered a serious error. The maximum number of bytes that can be received by an endpoint is determined by the Endpoint Base Length register for each endpoint. The Overflow bit is only relevant during OUT Tokens from the host.
4	Setup	'1' indicates Setup Packet. If this bit is set, the last packet received was a setup packet.
3	Sequence	This bit indicates if the last packet was a DATA0 (0) or DATA1 (1).
2	Time-out	This bit is not used in slave mode.
1	Error	Error detected in transmission, this includes CRC5/16 and PID errors.
0	ACK	Transmission Acknowledge.

Endpoint Transfer Count [Address a = (EP# * 10h)+4, b = (EP# * 10h)+Ch]. As a peripheral device, the Endpoint Transfer Count register is only important with OUT tokens (host sending the slave data). When a host sends the peripheral data, the Transfer Count register contains the difference between the Endpoint Base Length and the actual number of bytes received in the last packet. In other words, if the Endpoint Base Length register was set for 64 (40h) bytes and an OUT token was sent to the endpoint that only had 16 (10h) bytes, the Endpoint Transfer Count register has a value of 48 (30h). If more bytes were sent in an OUT token then the Endpoint Base Length register was programmed for, the overflow flag is set in the Endpoint Packet Status register and is considered a serious error.

Table 26. Endpoint Transfer Count Reg [Address EP0a/b:04h/0Ch, EP1a/b:14h/1Ch, EP2a/b:24h/2Ch, EP3a/b:34h/3Ch]

7	6	5	4	3	2	1	0
EPxCNT7	EPxCNT6	EPxCNT5	EPxCNT4	EPxCNT3	EPxCNT2	EPxCNT1	EPxCNT0

USB Control Registers

The USB Control registers manage communication and data flow on the USB. Each USB device is composed of a collection of independently operating endpoints. Each endpoint has a unique identifier, which is the Endpoint Number. For more details about USB endpoints, refer to the USB Specification 1.1, Section 5.3.1.

The Control and Status registers are mapped as follows:

Table 27. Control and Status Register Map

Register Name	Address (in Hex)
Control Register 1	05h
Interrupt Enable Register	06h
USB Address Register	07h
Interrupt Status Register	0Dh
Current Data Set Register	0Eh
Control Register 2	0Fh
SOF Low Byte Register	15h
SOF High Byte Register	16h
DMA Total Count Low Byte Register	35h
DMA Total Count High Byte Register	36h

Control Register 1, Address [05h]. The Control register enables or disables USB transfers and DMA operations with control bits.

Table 28. Control Register 1 [Address 05h]

7	6	5	4	3	2	1	0
Reserved	STBYD	SPSEL	J-K1	J-K0	DMA Dir	DMA Enable	USB Enable

Bit Position	Bit Name	Function
7	Reserved	Reserved bit - must be set to '0'.
6	STBYD	XCVR Power Control. ‘1’ sets XCVR to low power. For normal operation set this bit to ‘0’. Suspend mode is entered if bit 6 = ‘1’ and bit ‘0’ (USB Enable) = ‘0’.
5	SPSEL	Speed Select. ‘0’ selects full speed. ‘1’ selects low speed (also see Table 34 on page 17).
4	J-K1	J-K1 and J-K0 force state control bits are used to generate various USB bus conditions. Forcing K-state is used for Peripheral device remote wake-up, Resume, and other modes. These two bits are set to zero on power up, see Table 29 for functions.
3	J-K0	
2	DMA Dir	DMA Transfer Direction. Set equal to ‘1’ for DMA READ cycles from SL811HS. Set equal to ‘0’ for DMA WRITE cycles.
1	DMA Enable	Enable DMA operation when equal to ‘1’. Disable = ‘0’. DMA is initiated when DMA Count High is written.
0	USB Enable	Overall Enable for Transfers. ‘1’ enables and’ ‘0 disables. Set this bit to ‘1’ to enable USB communication. Default at power up = ‘0’

Table 29. J-K Force-state Control Bits

JK-Force State	USB Engine Reset	Function
0	0	Normal operating mode
0	1	Force SE0, D+ and D– are set low
1	0	Force K-State, D– set high, D+ set low
1	1	Force J-State, D+ set high, D– set low

Interrupt Enable Register, Address [06h] . The SL811HS provides an Interrupt Request Output that is activated resulting from a number of conditions. The Interrupt Enable register allows the user to select events that generate the Interrupt Request Output assertion. A separate Interrupt Status register is read in order to determine the condition that initiated the interrupt (see the description in section Interrupt Status Register, Address [0Dh]). When a bit is set to '1', the corresponding interrupt is enabled. Setting a bit in the Interrupt Enable register does not effect the Interrupt Status register's value; it just determines which interrupts are output on INTRQ.

Table 30. Interrupt Enable Register [Address: 06h]

7	6	5	4	3	2	1	0
DMA Status	USB Reset	SOF Received	DMA Done	Endpoint 3 Done	Endpoint 2 Done	Endpoint 1 Done	Endpoint 0 Done

Bit Position	Bit Name	Function
7	DMA Status	When equal to '1', indicates DMA transfer is in progress. When equal to '0', indicates DMA transfer is complete.
6	USB Reset	Enable USB Reset received interrupt when = '1'.
5	SOF Received	Enable SOF Received Interrupt when = '1'.
4	DMA Done	Enable DMA done Interrupt when = '1'.
3	Endpoint 3 Done	Enable Endpoint 3 done Interrupt when = '1'.
2	Endpoint 2 Done	Enable Endpoint 2 done Interrupt when = '1'.
1	Endpoint 1 Done	Enable Endpoint 1 done Interrupt when = '1'.
0	Endpoint 0 Done	Enable Endpoint 0 done Interrupt when = '1'.

USB Address Register, Address [07h]. This register contains the USB Device Address after assignment by USB host during configuration. On power up or reset, USB Address register is set to Address 00h. After USB configuration and address assignment, the device recognizes only USB transactions directed to the address contained in the USB Address register.

Table 31. USB Address Register [Address 07h]

7	6	5	4	3	2	1	0
USBADD7	USBADD6	USBADD5	USBADD4	USBADD3	USBADD2	USBADD1	USBADD0

Interrupt Status Register, Address [0Dh]. This read/write register serves as an Interrupt Status register when it is read, and an Interrupt Clear register when it is written. To clear an interrupt, write the register with the appropriate bit set to '1'. Writing a '0' has no effect on the status.

Table 32. Interrupt Status Register [Address 0Dh]

7	6	5	4	3	2	1	0
DMA Status	USB Reset	SOF Received	DMA Done	Endpoint 3 Done	Endpoint 2 Done	Endpoint 1 Done	Endpoint 0 Done

Bit Position	Bit Name	Function
7	DMA Status	When equal to '1', indicates DMA transfer is in progress. When equal to 0, indicates DMA transfer is complete. An interrupt is not generated when DMA is complete.
6	USB Reset	USB Reset Received Interrupt.
5	SOF Received	SOF Received Interrupt.
4	DMA Done	DMA Done Interrupt.
3	Endpoint 3 Done	Endpoint 3 Done Interrupt.
2	Endpoint 2 Done	Endpoint 2 Done Interrupt.
1	Endpoint 1 Done	Endpoint 1 Done Interrupt.
0	Endpoint 0 Done	Endpoint 0 Done Interrupt.

Current Data Set Register, Address [0Eh]. This register indicates current selected data set for each endpoint.

Table 33. Current Data Set Register [Address 0Eh]

7	6	5	4	3	2	1	0
Reserved				Endpoint 3	Endpoint 2	Endpoint 1	Endpoint 0

Bit Position	Bit Name	Function
7-4	Reserved	Not applicable.
3	Endpoint 3 Done	Endpoint 3a = 0, Endpoint 3b = 1.
2	Endpoint 2 Done	Endpoint 2a = 0, Endpoint 2b = 1.
1	Endpoint 1 Done	Endpoint 1a = 0, Endpoint 1b = 1.
0	Endpoint 0 Done	Endpoint 0a = 0, Endpoint 0b = 1.

Control Register 2, Address [0Fh]. Control Register 2 is used to control if the device is configured as a master or a slave. It can change the polarity of the Data+ and Data- pins to accommodate both full- and low speed operation.

Table 34. Control Register 2 [Address 0Fh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SL811HS Master/Slave selection	SL811HS D+/D– Data Polarity Swap	Reserved					

Bit Position	Bit Name	Function
7	SL811HS Master/Slave selection	Master = ‘1’ Slave = ‘0’
6	SL811HS D+/D– Data Polarity Swap	’1’ = change polarity (low speed) ’0’ = no change of polarity (full speed)
5-0	Reserved	NA

SOF Low Register, Address [15h]. Read only register contains the 7 low order bits of Frame Number in positions: bit 7:1. Bit 0 is undefined. Register is updated when a SOF packet is received. Do not write to this register.

SOF High Register, Address [16h]. Read only register contains the 4 low order bits of Frame Number in positions: bit 7:4. Bits 3:0 are undefined and should be masked when read by the user. This register is updated when a SOF packet is received. The user should not write to this register.

DMA Total Count Low Register, Address [35h]. The DMA Total Count Low register contains the low order 8 bits of DMA count. DMA total count is the total number of bytes to be transferred between a peripheral to the SL811HS. The count may sometimes require up to 16 bits, therefore the count is represented in two registers: Total Count Low and Total Count High. EP3 is only supported with DMA operation.

DMA Total Count High Register, Address [36h]. The DMA Total Count High register contains the high order 8 bits of DMA count. When written, this register enables DMA if the DMA Enable bit is set in Control Register 1. The user should always write Low Count register first, followed by a write to High Count register, even if high count is 00h.

Physical Connections

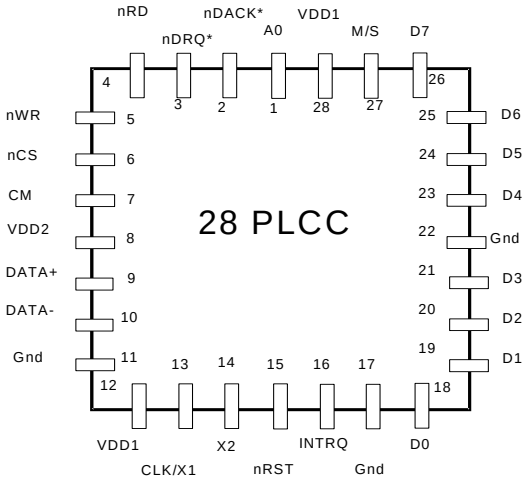
These parts are offered in both a 28-pin PLCC package and a 48-pin TQFP package. The 28-pin PLCC packages are the SL811HS and SL811HS-JCT. The 48-pin TQFP packages is the SL811HST-AXC.

28-Pin PLCC Physical Connections

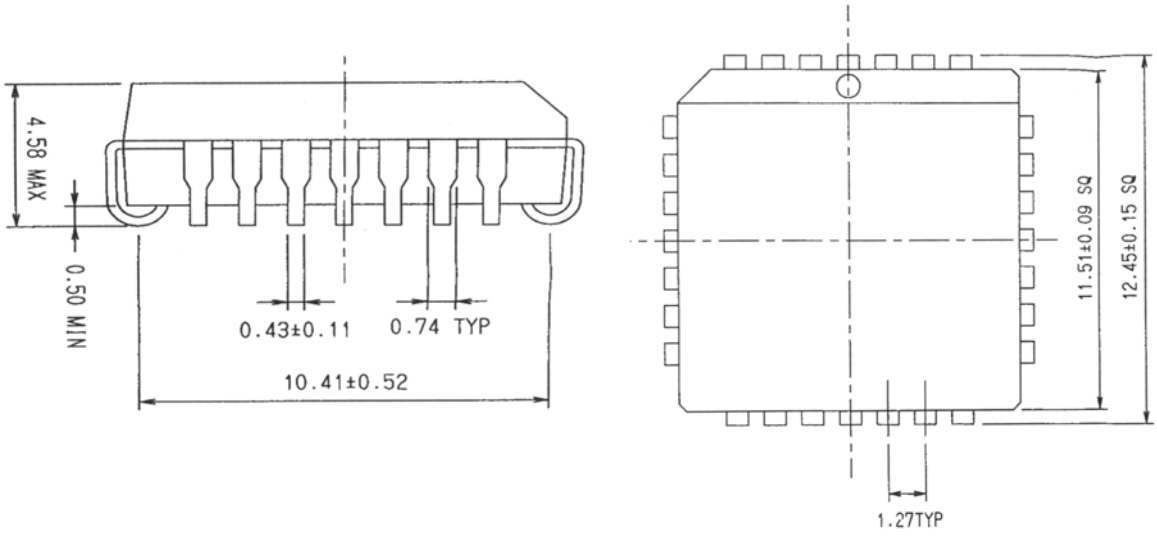
28-Pin PLCC Pin Layout

*See Table 35 on page 21 for Pin and Signal Description for Pins 2 and 3 in Host Mode.

Figure 4. 28-pin PLCC USB Host/Slave Controller — Pin Layout



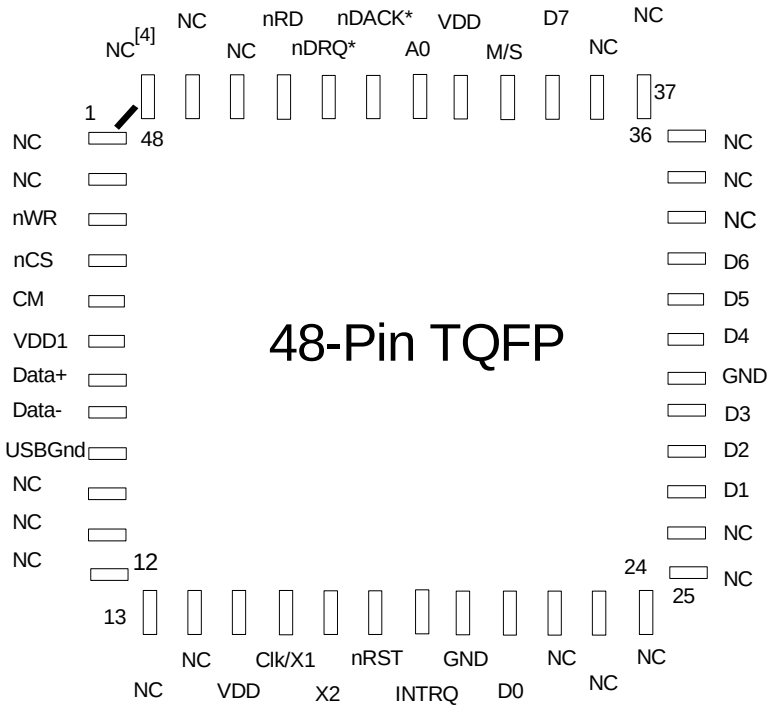
28-Pin PLCC Mechanical Dimensions



48-Pin TQFP Physical Connections

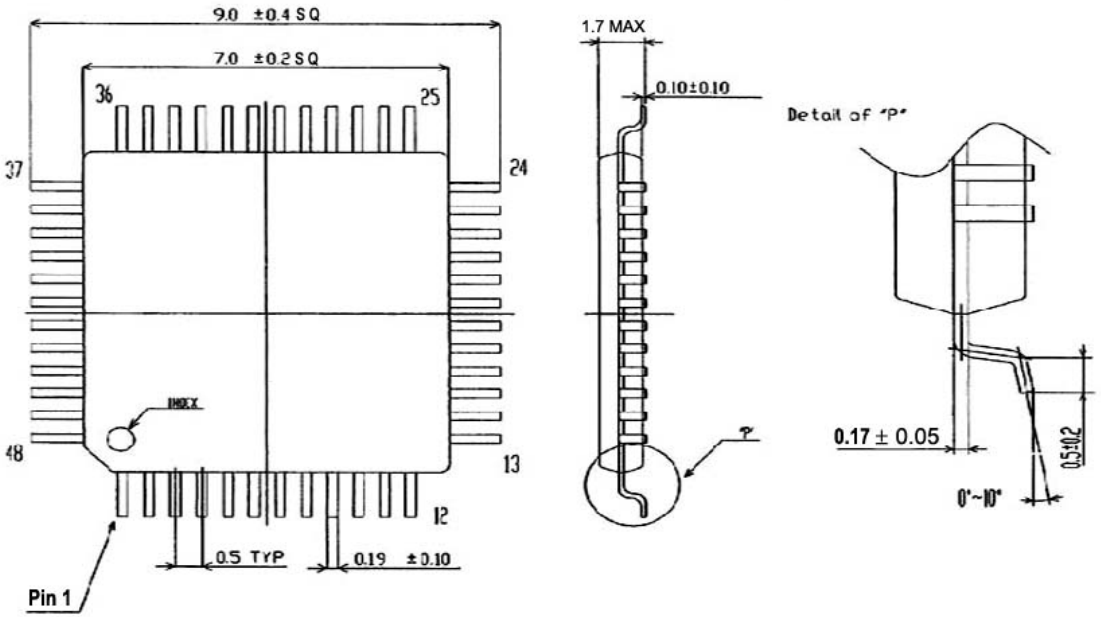
48-Pin TQFP AXC Pin Layout

Figure 6. 48-Pin TQFP AXC USB Host/Slave Controller Pin Layout



*See Table 35 on page 21 for Pin and Signal Description for Pins 43 and 44 in Host Mode.

48-Pin TQFP Mechanical Dimensions



Note
4. NC. Indicates No Connection. NC Pins must be left unconnected.

48/28-Pin USB Host Controller Pins Description

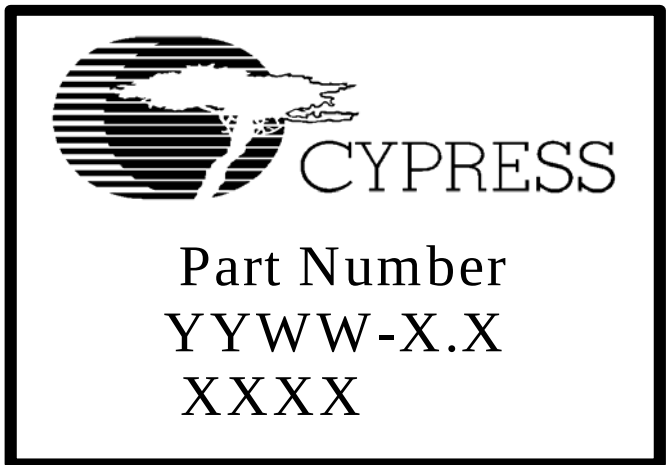
The SL811HST-AXC is packaged in a 48-pin TQFP. The SL811HS and SL811HS-JCT packages are 28-pin PLCC's. These devices require a 3.3 VDC power source. The 48-Pin TQFP requires an external 12 or 48 MHz crystal or clock.

Table 35. 48/28-Pin TQFP AXC Pin Assignments and Definitions

48-Pin TQFP AXC Pin No.	28-Pin PLCC Pin No.	Pin Type	Pin Name	Pin Description
1	–	NC	NC	No connection.
2	–	NC	NC	No connection.
3	5	IN	nWR	**Write Strobe Input**. An active LOW input used with nCS to write to registers/data memory.
4	6	IN	nCS	**Active LOW 48-Pin TQFP Chip select**. Used with nRD and nWr when accessing the 48-Pin TQFP.
5[5]	7[6]	IN	CM	**Clock Multiply**. Select 12 MHz/48 MHz Clock Source.
6	8	VDD1	+3.3 VDC	**Power for USB Transceivers**. V_{DD1} may be connected to V_{DD}.
7	9	BIDIR	DATA +	USB Differential Data Signal HIGH Side.
8	10	BIDIR	DATA -	USB Differential Data Signal LOW Side.
9	11	GND	USB GND	Ground Connection for USB.
10	–	NC	NC	No connection.
11	–	NC	NC	No connection.
12	–	NC	NC	No connection.
13	–	NC	NC	No connection.
14	–	NC	NC	No connection.
15[7]	12	VDD	+3.3 VDC	Device V_{DD} Power.
16	13	IN	CLK/X1	Clock or External Crystal X1 connection. The X1/X2 Clock requires external 12 or 48 MHz matching crystal or clock source.
17	14	OUT	X2	External Crystal X2 connection.
18	15	IN	nRST	Device active low reset input.
19	16	OUT	INTRQ	Active HIGH Interrupt Request output to external controller.
20	17	GND	GND	Device Ground.
21	18	BIDIR	D0	**Data 0**. Microprocessor Data/Address Bus.
22	–	NC	NC	No connection.
23	–	NC	NC	No connection.
24	–	NC	NC	No connection.
25	–	NC	NC	No connection.
26	–	NC	NC	No connection.
27	19	BIDIR	D1	**Data 1**. Microprocessor Data/Address Bus.
28	20	BIDIR	D2	**Data 2**. Microprocessor Data/Address Bus.
29	21	BIDIR	D3	**Data 3**. Microprocessor Data/Address Bus.
30	22	GND	GND	Device Ground.
31	23	BIDIR	D4	**Data 4**. Microprocessor Data/Address Bus.
32	24	BIDIR	D5	**Data 5**. Microprocessor Data/Address Bus.

Notes
5. The CM Clock Multiplier pin must be tied HIGH for a 12 MHz clock source and tied to ground for a 48 MHz clock source.
6. The CM Clock Multiplier pin must be tied HIGH for a 12 MHz clock source and tied to ground for a 48 MHz clock source. In 28-pin PLCC's, this pin is designated as an ALE input pin.
7. VDD can be derived from the USB supply. See Figure 5 on page 19.

Package Markings (48-Pin TQFP)



YYWW = Date code
XXXX = Product code
X.X = Silicon revision number

Electrical Specifications

Absolute Maximum Ratings

This section lists the absolute maximum ratings of the SL811HS. Stresses above those listed can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can affect device operation and reliability.

Description	Condition
Storage Temperature	–40°C to 125°C
Voltage on any pin with respect to ground	–0.3V to 6.0V
Power Supply Voltage (V_{DD})	4.0V
Power Supply Voltage (V_{DD1})	4.0V
Lead Temperature (10 seconds)	180°C

Recommended Operating Condition

Parameter	Min.	Typical	Max.
Power Supply Voltage, VDD	3.0V	3.3V	3.45V
Power Supply Voltage, VDD1	3.0V		3.45V
Operating Temperature	0°C		65°C

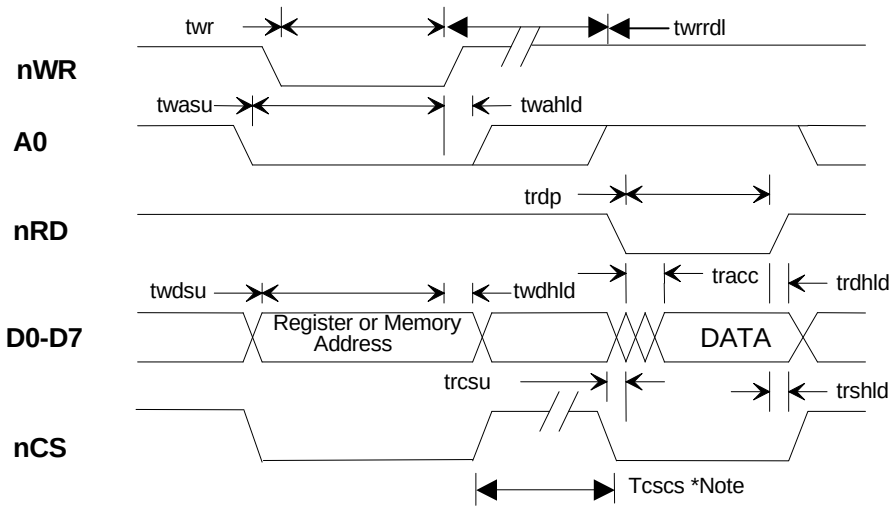
Crystal Requirements, (X1, X2)	Min.	Typical	Max.
Operating Temperature Range	0°C		65°C
Parallel Resonant Frequency[10]		48 MHz	
Frequency Drift over Temperature			±50 ppm
Accuracy of Adjustment			±30 ppm
Series Resistance			100 Ohms
Shunt Capacitance	3 pF		6 pF
Load Capacitance		20 pF	
Drive Level	20 μW		5 mW
Mode of Vibration Third Overtone[11]			

External Clock Input Characteristics (X1)

Parameter	Min.	Typical	Max.
Clock Input Voltage @ X1 (X2 Open)	1.5V		
Clock Frequency[12]		48 MHz	

Notes
10. The 28-PIN plcc can use a 12 MHz Crystal Oscillator or 12 MHz Clock Source.
11. Fundamental mode for 12 MHz Crystal.
12. The SL811HS can use a 12 MHz Clock Source.

I/O Read Cycle

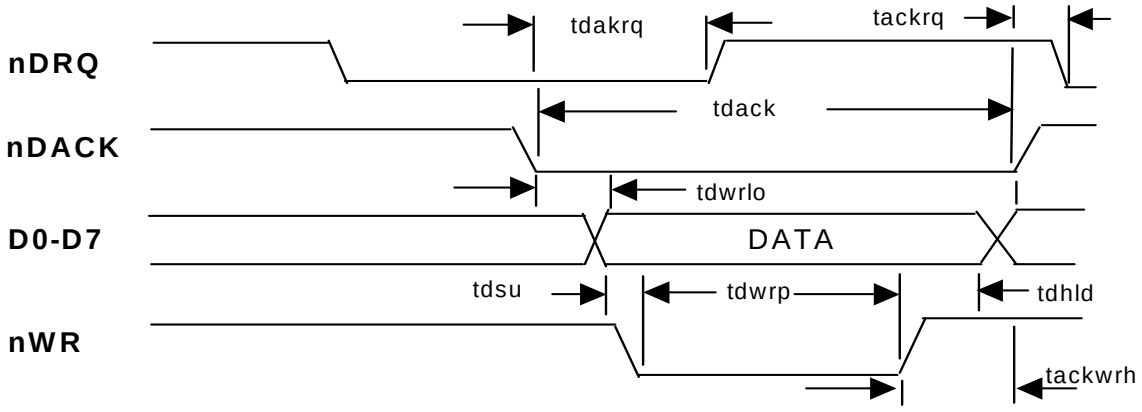


I/O Read Cycle from Register or Memory Buffer

Parameter	Description	Min.	Typ.	Max.
t_{WR}	Write pulse width	85 ns		
t_{RD}	Read pulse width	85 ns		
t_{WCSU}	Chip select set-up to nWR	0 ns		
t_{WASU}	A0 address set-up time	85 ns		
t_{WAHLD}	A0 address hold time	10 ns		
t_{WDSU}	Data to Write HIGH set-up time	85 ns		
t_{WDHLD}	Data hold time after Write HIGH	5 ns		
t_{RACC}	Data valid after Read LOW	25 ns		85 ns
t_{RDHLD}	Data hold after Read HIGH	40 ns		
t_{RCSU}	Chip select LOW to Read LOW	0 ns		
t_{RSHLD}	NCS hold after Read HIGH	0 ns		
T_{CSCS}*	nCS inactive to nCS *asserted	85 ns		
t_{WRRDL}	nWR HIGH to nRD LOW	85ns		

Note nCS can be kept LOW during multiple Read cycles provided nRD is cycled. Rd Cycle Time for Auto Inc Mode Reads is 170 ns minimum.

DMA Write Cycle

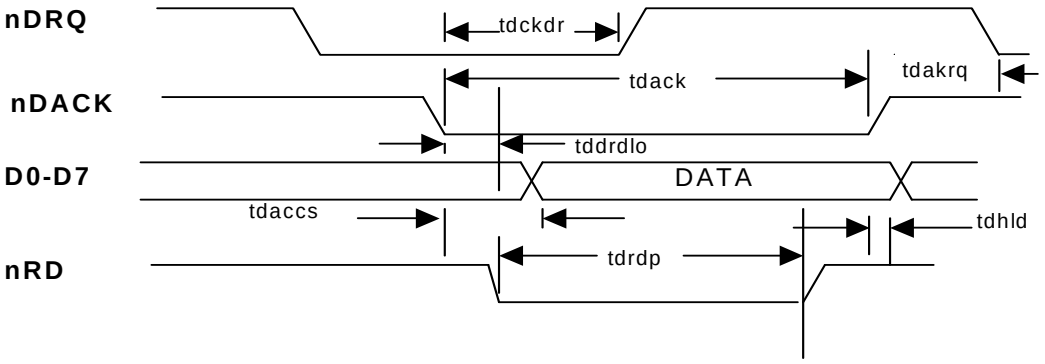


DMA Write Cycle

Parameter	Description	Min.	Typ.	Max.
tdack	nDACK low	80 ns		
tdwrlo	nDACK to nWR low delay	5 ns		
tdakrq	nDACK low to nDRQ high delay	5 ns		
tdwrp	nWR pulse width	65 ns		
tdhld	Data hold after nWR high	5 ns		
tdsu	Data set-up to nWR strobe low	60 ns		
tackrq	NDACK high to nDRQ low	5 ns		
tackwrh	NDACK high to nDRQ low	5 ns		
twrcycle	DMA Write Cycle Time	150 ns		

Note nWR must go low after nDACK goes low in order for nDRQ to clear. If this sequence is not implemented as requested, the next nDRQ is not inserted.

DMA Read Cycle

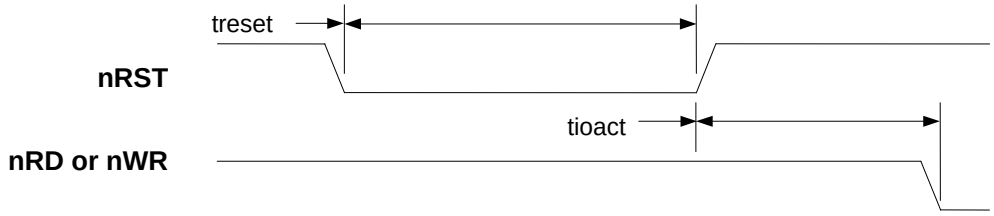


SL811 DMA Read Cycle Timing

Parameter	Description	Min.	Typ.	Max.
tdack	nDACK low	100 ns		
tddrdlo	nDACK to nRD low delay	0 ns		
tdckdr	nDACK low to nDRQ high delay	5 ns		
tdrdp	nRD pulse width	90 ns		
tdhld	Date hold after nDACK high	5 ns		
tddaccs	Data access from nDACK low	85 ns		
tdrdack	nRD high to nDACK high	0 ns		
tdakrq	nDRQ low after nDACK high	5 ns		
trdcycle	DMA Read Cycle Time	150 ns		

Note Data is held until nDACK goes high regardless of state of nREAD.

Reset Timing



Reset Timing

Parameter	Description	Min.	Typ.	Max.
t_{RESET}	nRst Pulse width	16 clocks		
t_{IOACT}	nRst HIGH to nRD or nWR active	16 clocks		

Note Clock is 48 MHz nominal.

Package Diagrams (continued)

48-Lead Thin Plastic Quad Flat Pack (7x7x1.4 mm) A48