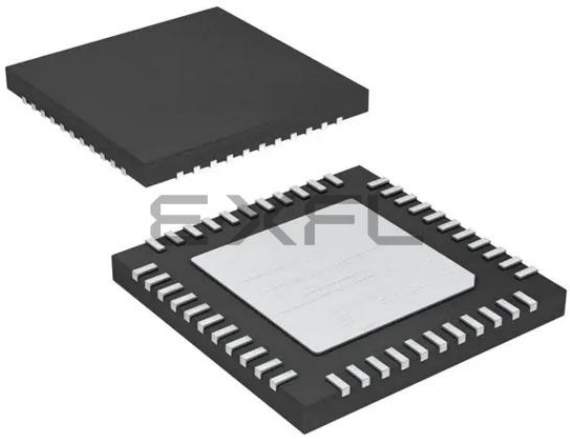

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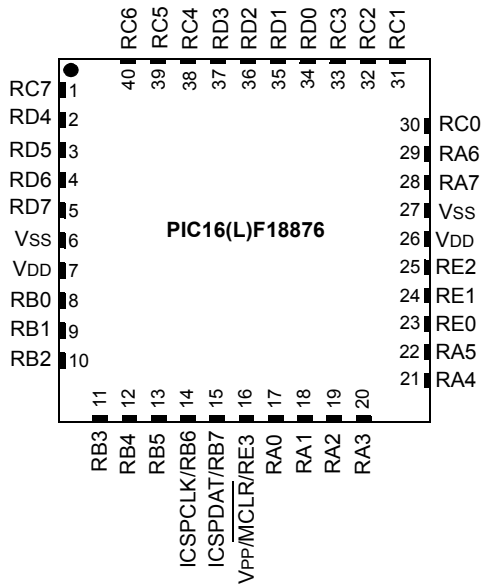
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18876-e-ml

40-pin UQFN (5x5)

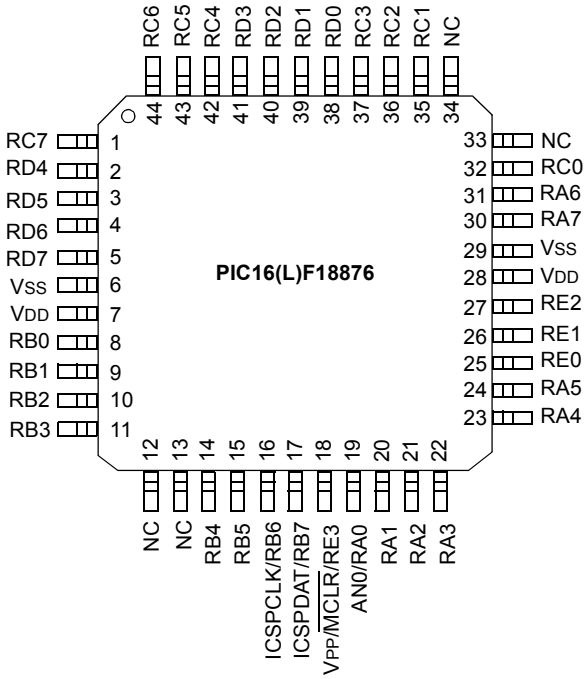


Note 1: See Table 3 for location of all peripheral functions.

2: All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

3: The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

44-pin TQFP (10x10)



Note 1: See Table 3 for location of all peripheral functions.

2: All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

TABLE 3-10: PIC16(L)F18856 MEMORY MAP, BANK 30

	Bank 30
F0Ch	—
F0Dh	—
F0Eh	—
F0Fh	—
F10h	RA0PPS
F11h	RA1PPS
F12h	RA2PPS
F13h	RA3PPS
F14h	RA4PPS
F15h	RA5PPS
F16h	RA6PPS
F17h	RA7PPS
F18h	RB0PPS
F19h	RB1PPS
F1Ah	RB2PPS
F1Bh	RB3PPS
F1Ch	RB4PPS
F1Dh	RB5PPS
F1Eh	RB6PPS
F1Fh	RB7PPS
F20h	RC0PPS
F21h	RC1PPS
F22h	RC2PPS
F23h	RC3PPS
F24h	RC4PPS
F25h	RC5PPS
F26h	RC6PPS
F27h	RC7PPS
F28h F37h	—
F38h	ANSELA
F39h	WPUA
F3Ah	ODCONA
F3Bh	SLRCONA
F3Ch	INLVLA
F3Dh	IOCAP
F3Eh	IOCAN
F3Fh	IOCAF

	Bank 30
F40h	CCDNA
F41h	CCDPA
F42h	—
F43h	ANSELB
F44h	WPUB
F45h	ODCONB
F46h	SLRCONB
F47h	INLVLB
F48h	IOCBP
F49h	IOCBN
F4Ah	IOCBF
F4Bh	CCDNB
F4Ch	CCDPB
F4Dh	—
F4Eh	ANSELC
F4Fh	WPUC
F50h	ODCONC
F51h	SLRCONC
F52h	INLVLC
F53h	IOCCP
F54h	IOCCN
F55h	IOCCF
F56h	CCDNC
F57h	CCDPC
F58h F64h	—
F65h	WPUE
F66h	—
F67h	—
F68h	INLVLE
F69h	IOCEP
F6Ah	IOCEN
F6Bh	IOCEF
F6Ch	—
F6Dh	—
F6Eh	—
F6Fh	—

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18856	PIC16(L)F18876	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 1													
	CPU CORE REGISTERS; see Table 3-2 for specifics												
08Ch	ADRESL			ADRESL<7:0>								0000 0000	0000 0000
08Dh	ADRESH			ADRESH<7:0>								0000 0000	0000 0000
08Eh	ADPREVL			ADPREVL<7:0>								0000 0000	0000 0000
08Fh	ADPREVH			ADPREVH<7:0>								0000 0000	0000 0000
090h	ADACCL			ADACCL<7:0>								xxxx xxxx	uuuu uuuu
091h	ADACCH			ADACCH<7:0>								xxxx xxxx	uuuu uuuu
092h	—	—		Unimplemented								—	—
093h	ADCON0			ADON	ADCONT	—	ADCS	—	ADFRM0	—	ADGO	00-0 -0-0	00-0 -0-0
094h	ADCON1			ADPPOL	ADIPEN	ADGPOL	—	—	—	—	ADDSEN	000- ---0	000- ---0
095h	ADCON2			ADPSIS	ADCRS<2:0>			ADACLR	ADMD<2:0>			0000 0000	0000 0000
096h	ADCON3			—	ADCALC<2:0>			ADSOI	ADTMD<2:0>			-000 0000	-000 0000
097h	ADSTAT			ADAOV	ADUTHR	ADLTHR	ADMATH	—	ADSTAT<2:0>			0000 -000	0000 -000
098h	ADCLK			—	—	ADCCS<5:0>						--00 0000	--00 0000
099h	ADACT			—	—	—	ADACT<4:0>					---0 0000	---0 0000
09Ah	ADREF			—	—	—	ADNREF	—	—	ADPREF<1:0>		---0 --00	---0 --00
09Bh	ADCAP			—	—	—	ADCAP<4:0>					---0 0000	---0 0000
09Ch	ADPRE			ADPRE<7:0>								0000 0000	0000 0000
09Dh	ADACQ			ADACQ<7:0>								0000 0000	0000 0000
09Eh	ADPCH			—	—	ADPCH<5:0>						--00 0000	--00 0000
09Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18856	PIC16(L)F18876	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 30													
CPU CORE REGISTERS; see Table 3-2 for specifics													
F0Ch — F0Fh	—	—		Unimplemented								—	—
F10h	RA0PPS			—	—	RA0PPS<5:0>						--00 0000	--uu uuuu
F11h	RA1PPS			—	—	RA1PPS<5:0>						--00 0000	--uu uuuu
F12h	RA2PPS			—	—	RA2PPS<5:0>						--00 0000	--uu uuuu
F13h	RA3PPS			—	—	RA3PPS<5:0>						--00 0000	--uu uuuu
F14h	RA4PPS			—	—	RA4PPS<5:0>						--00 0000	--uu uuuu
F15h	RA5PPS			—	—	RA5PPS<5:0>						--00 0000	--uu uuuu
F16h	RA6PPS			—	—	RA6PPS<5:0>						--00 0000	--uu uuuu
F17h	RA7PPS			—	—	RA7PPS<5:0>						--00 0000	--uu uuuu
F18h	RB0PPS			—	—	RB0PPS<5:0>						--00 0000	--uu uuuu
F19h	RB1PPS			—	—	RB1PPS<5:0>						--00 0000	--uu uuuu
F1Ah	RB2PPS			—	—	RB2PPS<5:0>						--00 0000	--uu uuuu
F1Bh	RB3PPS			—	—	RB3PPS<5:0>						--00 0000	--uu uuuu
F1Ch	RB4PPS			—	—	RB4PPS<5:0>						--00 0000	--uu uuuu
F1Dh	RB5PPS			—	—	RB5PPS<5:0>						--00 0000	--uu uuuu
F1Eh	RB6PPS			—	—	RB6PPS<5:0>						--00 0000	--uu uuuu
F1Fh	RB7PPS			—	—	RB7PPS<5:0>						--00 0000	--uu uuuu
F20h	RC0PPS			—	—	RC0PPS<5:0>						--00 0000	--uu uuuu
F21h	RC1PPS			—	—	RC1PPS<5:0>						--00 0000	--uu uuuu
F22h	RC2PPS			—	—	RC2PPS<5:0>						--00 0000	--uu uuuu
F23h	RC3PPS			—	—	RC3PPS<5:0>						--00 0000	--uu uuuu

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18856	PIC16(L)F18876	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 30 (Continued)													
F5Ch	SLRCOND	—	X	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	1111 1111	1111 1111
		X	—	Unimplemented								---- ----	---- ----
F5Dh	INLVLD	—	X	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	1111 1111	1111 1111
		X	—	Unimplemented								---- ----	---- ----
F5Eh — F60h	—	—		Unimplemented								—	—
F61h	CCDND	—	X	CCDND7	CCDND6	CCDND5	CCDND4	CCDND3	CCDND2	CCDND1	CCDND0	0000 0000	0000 0000
		X	—	Unimplemented								---- ----	---- ----
F62h	CCDPD	—	X	CCDPD7	CCDPD6	CCDPD5	CCDPD4	CCDPD3	CCDPD2	CCDPD1	CCDPD0	0000 0000	0000 0000
		X	—	Unimplemented								---- ----	---- ----
F63h	—	—		Unimplemented								—	—
F64h	ANSELE	—	X	—	—	—	—	—	ANSE2	ANSE1	ANSE0	---- -111	---- -111
		X	—	Unimplemented								---- ----	---- ----
F65h	WPUE	—	X	—	—	—	—	WPUE3	WPUE2	WPUE1	WPUE0	---- 0000	---- 0000
		X	—	—	—	—	—	WPUE3	—	—	—	---- 0---	---- 0---
F66h	ODCONE	—	X	—	—	—	—	—	ODCE2	ODCE1	ODCE0	---- -000	---- -000
		X	—	Unimplemented								---- ----	---- ----
F67h	SLRCONE	—	X	—	—	—	—	—	SLRE2	SLRE1	SLRE0	---- -111	---- -111
		X	—	Unimplemented								---- ----	---- ----
F68h	INLVLE	—	X	—	—	—	—	INLVLE3	INLVLE2	INLVLE1	INLVLE0	---- 1111	---- 1111
		X	—	—	—	—	—	INLVLE3	—	—	—	---- 1---	---- 1---
F69h	IOCEP			—	—	—	—	IOCEP3	—	—	—	---- 0---	---- 0---
F6Ah	IOCEN			—	—	—	—	IOCEN3	—	—	—	---- 0---	---- 0---

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18856	PIC16(L)F18876	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 30 (Continued)													
F6Bh	IOCEF			—	—	—	—	IOCEF3	—	—	—	---- 0---	---- 0---
F6Ch	CCDNE	—	X	—	—	—	—	—	CCDNE2	CCDNE1	CCDNE0	---- -000	---- -000
		X	—	Unimplemented								---- ----	---- ----
F6Dh	CCDPE	—	X	—	—	—	—	—	CCDPE2	CCDPE1	CCDPE0	---- -000	---- -000
		X	—	Unimplemented								---- ----	---- ----
F6Eh	—	—		Unimplemented								—	—
F6Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

REGISTER 7-12: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **OSFIF**: Oscillator Fail-Safe Interrupt Flag bit
1 = Oscillator fail-safe interrupt has occurred (must be cleared in software)
0 = No oscillator fail-safe interrupt

bit 6 **CSWIF:** Clock Switch Complete Interrupt Flag bit
1 = The clock switch module indicates an interrupt condition (must be cleared in software)
0 = The clock switch does not indicate an interrupt condition

bit 5-2 **Unimplemented:** Read as '0'

bit 1 **ADTIF**: Analog-to-Digital Converter (ADC) Threshold Compare Interrupt Flag bit
1 = An A/D measurement was beyond the configured threshold (must be cleared in software)
0 = A/D measurements have been within the configured threshold

bit 0 **ADIF**: Analog-to-Digital Converter (ADC) Interrupt Flag bit
1 = An A/D conversion or complex operation has completed (must be cleared in software)
0 = An A/D conversion or complex operation is not complete

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

18.8 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in Table 37-14 for more details.

18.9 Analog Input Connection Considerations

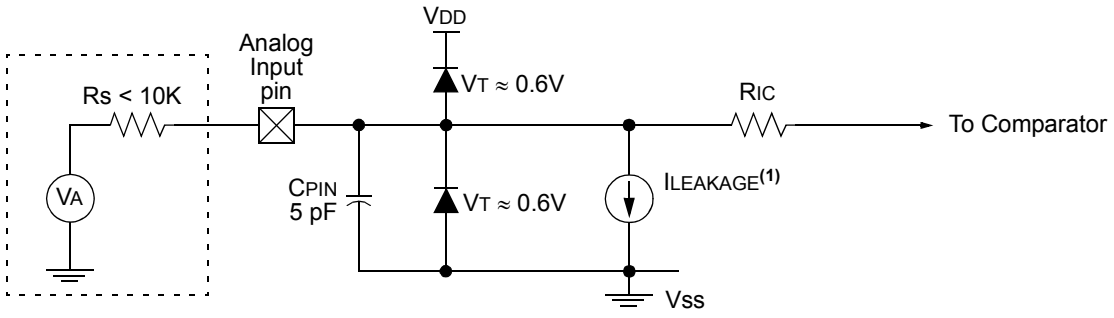
A simplified circuit for an analog input is shown in Figure 18-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to V_{DD} and V_{SS}. The analog input, therefore, must be between V_{SS} and V_{DD}. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 18-3: ANALOG INPUT MODEL



Legend: C_{PIN} = Input Capacitance
$I_{LEAKAGE}$ = Leakage Current at the pin due to various junctions
R_{IC} = Interconnect Resistance
R_S = Source Impedance
V_A = Analog Voltage
V_T = Threshold Voltage

Note 1: See I/O Ports in Table 37-4.

REGISTER 18-3: CMxNSEL: COMPARATOR Cx NEGATIVE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	NCH<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 2-0 **NCH<2:0>:** Comparator Negative Input Channel Select bits

111 = CxVN connects to AVSS
110 = CxVN connects to FVR Buffer 2
101 = CxVN unconnected
100 = CxVN unconnected
011 = CxVN connects to CxIN3- pin
010 = CxVN connects to CxIN2- pin
001 = CxVN connects to CxIN1- pin
000 = CxVN connects to CxIN0- pin

REGISTER 18-4: CMxPSEL: COMPARATOR Cx POSITIVE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	PCH<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 5-3 **PCH<2:0>:** Comparator Positive Input Channel Select bits

111 = CxVP connects to AVSS
110 = CxVP connects to FVR Buffer 2
101 = CxVP connects to DAC output
100 = CxVP unconnected
011 = CxVP unconnected
010 = CxVP unconnected
001 = CxVP connects to CxIN1+ pin
000 = CxVP connects to CxIN0+ pin

TABLE 19-3: SUMMARY OF REGISTERS ASSOCIATED WITH PWMx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PWM6CON	PWM6EN	—	PWM6OUT	PWM6POL	—	—	—	—	287
PWM6DCH	PWM6DC<9:2>								288
PWM6DCL	PWM6DC<1:0>		—	—	—	—	—	—	288
PWM7CON	PWM7EN	—	PWM7OUT	PWM7POL	—	—	—	—	287
PWM7DCH	PWM7DC<9:2>								288
PWM7DCL	PWM7DC<1:0>		—	—	—	—	—	—	288
T2CON	ON	CKPS<2:0>			OUTPS<3:0>				441
T4CON	ON	CKPS<2:0>			OUTPS<3:0>				441
T6CON	ON	CKPS<2:0>			OUTPS<3:0>				441
T2TMR	Holding Register for the 8-bit TMR2 Register								
T4TMR	Holding Register for the 8-bit TMR4 Register								
T6TMR	Holding Register for the 8-bit TMR6 Register								
T2PR	TMR2 Period Register								
T4PR	TMR4 Period Register								
T6PR	TMR6 Period Register								
RxyPPS	—	—	RxyPPS<5:0>						250
CWG1ISM	—	—	—	—	IS<3:0>				312
CWG2ISM					IS<3:0>				312
CWG3ISM					IS<3:0>				312
CLCxSELy	—	—	LCxDyS<5:0>						329
MDSRC	—	—	—	MDMS<4:0>					399
MDCARH	—	—	—	—	MDCHS<3:0>				400
MDCARL	—	—	—	—	MDCLS<3:0>				401
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	204
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	220

Legend: - = Unimplemented locations, read as '0'. Shaded cells are not used by the PWMx module.

FIGURE 22-3: PROGRAMMABLE LOGIC FUNCTIONS

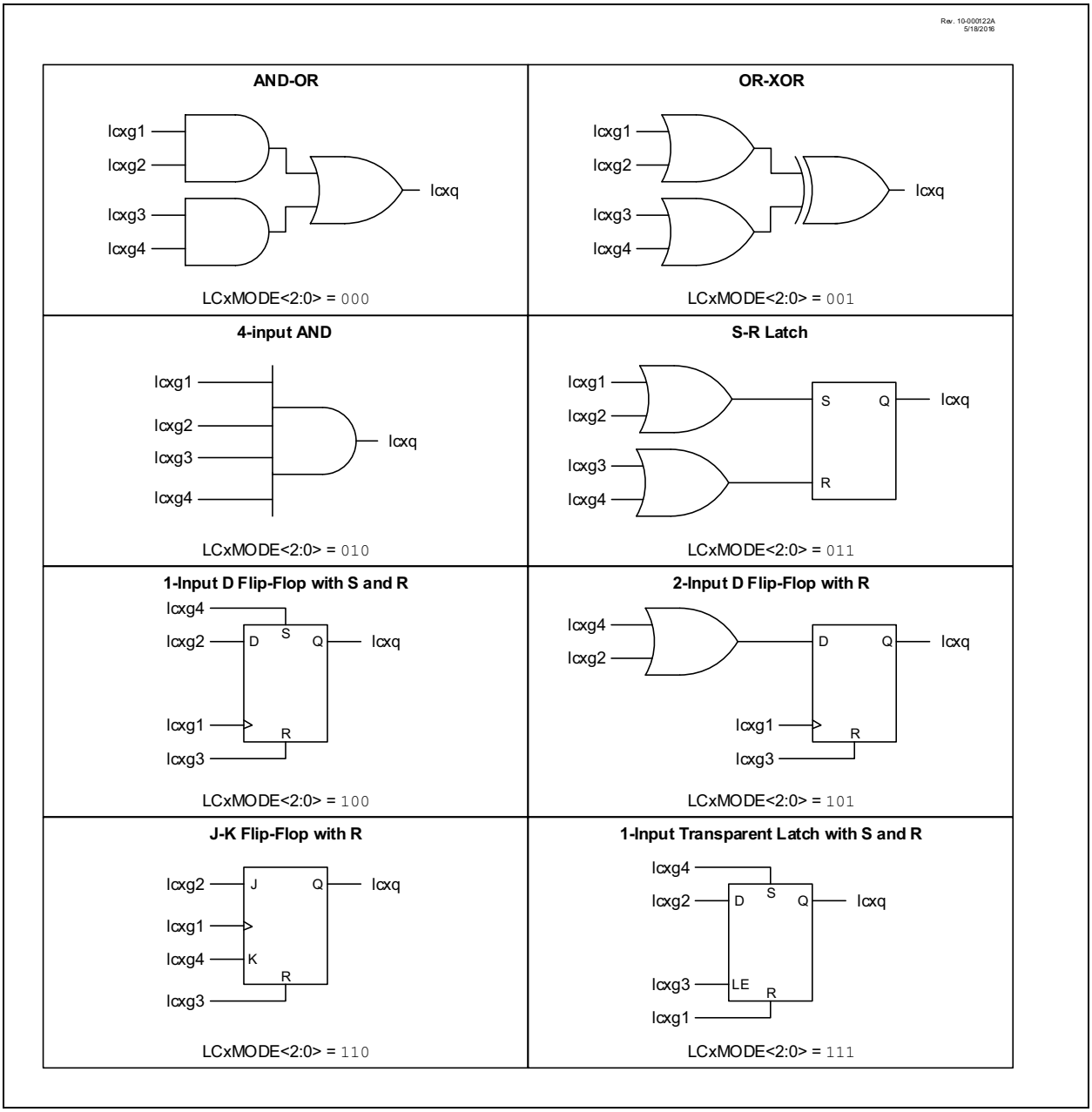


TABLE 23-6: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	ADON	ADCONT	—	ADCS	—	ADFRM0	—	ADGO	357
ADCON1	ADPPOL	ADIPEN	ADGPOL	—	—	—	—	ADDSEN	358
ADCON2	ADPSIS	ADCRS<2:0>			ADACLR	ADMD<2:0>			359
ADCON3	—	ADCALC<2:0>			ADSOI	ADTMD<2:0>			360
ADACT	—	—	—	ADACT<4:0>					359
ADACCH	ADACCH								369
ADACCL	ADACCL								369
ADPREVH	ADPREVH								368
ADPREVL	ADPREVL								369
ADRESH	ADRESH								367
ADRESL	ADRESL								367
ADSTAT	ADAOV	ADUTHR	ADLTHR	ADMATH	—	ADSTAT<2:0>			361
ADCLK	—	—	ADCCS<5:0>						362
ADREF	—	—	—	ADNREF	—	—	ADPREF<1:0>		362
ADCAP	—	—	—	ADCAP<4:0>					365
ADPRE	ADPRE<7:0>								364
ADACQ	ADACQ<7:0>								364
ADPCH	—	—	ADPCH<5:0>						363
ADCNT	ADCNT<7:0>								366
ADRPT	ADRPT<7:0>								365
ADLTHL	ADLTH<7:0>								371
ADLTHH	ADLTH<15:8>								371
ADUTHL	ADUTH<7:0>								372
ADUTHH	ADUTH<15:8>								372
ADSTPTL	ADSTPT<7:0>								370
ADSTPTH	ADSTPT<15:8>								370
ADFLTRL	ADFLTR<7:0>								366
ADFLTRH	ADFLTR<15:8>								366
ADERRL	ADERR<7:0>								371
ADERRH	ADERR<15:8>								370
ANSELA	ANSA7	ANSA6	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	205
ANSELB	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	213
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	221
ANSELD(1)	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	228
ANSELE	—	—	—	—	ANSE3	ANSE2(1)	ANSE1(1)	ANSE0(1)	238
DAC1CON1	—	—	—	DAC1R<4:0>					389
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		269
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	134
PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	136
PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	145
OSCSTAT	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR	124

Legend: – = unimplemented read as '0'. Shaded cells are not used for the ADC module.

Note 1: PIC16(L)F18876 only.

32.5.3 GO STATUS

Timer run status is determined by the TS bit of the SMTxSTAT register, and will be delayed in time by synchronizer delays in non-Counter modes.

32.6 Modes of Operation

The modes of operation are summarized in Table 32-1. The following sections provide detailed descriptions, examples of how the modes can be used. Note that all waveforms assume WPOL/SPOL/CPOL = 0. When WPOL/SPOL/CPOL = 1, all SMTSIGx, SMTWINx and SMT clock signals will have a polarity opposite to that indicated. For all modes, the REPEAT bit controls whether the acquisition is repeated or single. When REPEAT = 0 (Single Acquisition mode), the timer will stop incrementing and the SMTxGO bit will be reset upon the completion of an acquisition. Otherwise, the timer will continue and allow for continued acquisitions to overwrite the previous ones until the timer is stopped in software.

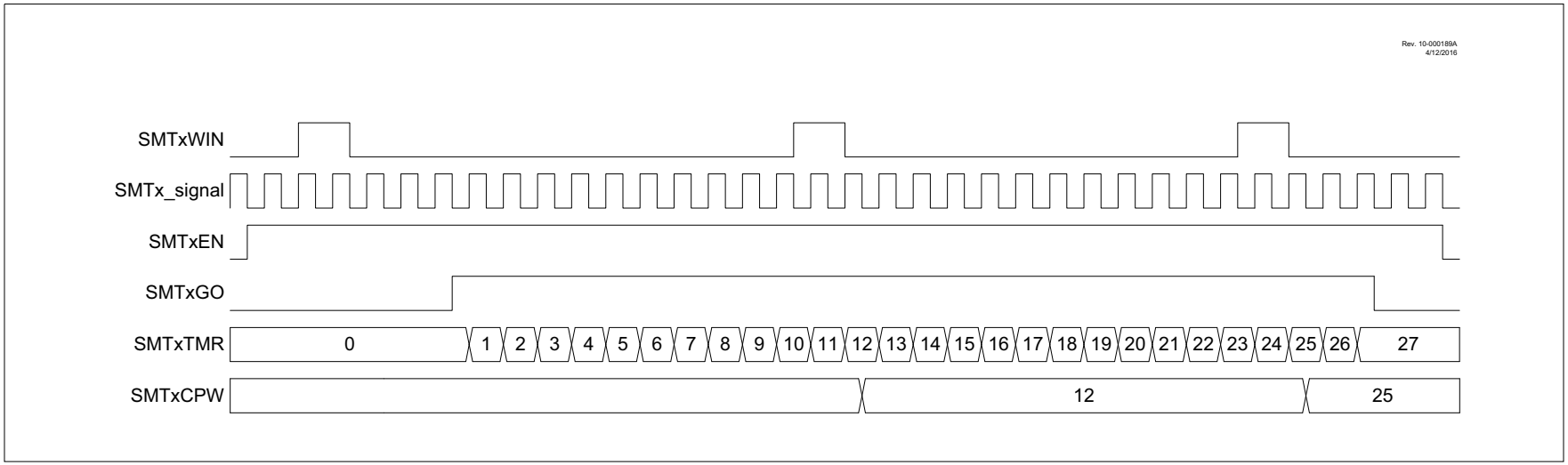
32.6.1 TIMER MODE

Timer mode is the simplest mode of operation where the SMTxTMR is used as a 16/24-bit timer. No data acquisition takes place in this mode. The timer increments as long as the SMTxGO bit has been set by software. No SMT window or SMT signal events affect the SMTxGO bit. Everything is synchronized to the SMT clock source. When the timer experiences a period match (SMTxTMR = SMTxPR), SMTxTMR is reset and the period match interrupt trips. See Figure 32-3.

TABLE 32-1: MODES OF OPERATION

MODE	Mode of Operation	Synchronous Operation	Reference
0000	Timer	Yes	**Section 32.6.1 “Timer Mode”**
0001	Gated Timer	Yes	**Section 32.6.2 “Gated Timer Mode”**
0010	Period and Duty Cycle Acquisition	Yes	**Section 32.6.3 “Period and Duty-Cycle Mode”**
0011	High and Low Time Measurement	Yes	**Section 32.6.4 “High and Low Measure Mode”**
0100	Windowed Measurement	Yes	**Section 32.6.5 “Windowed Measure Mode”**
0101	Gated Windowed Measurement	Yes	**Section 32.6.6 “Gated Window Measure Mode”**
0110	Time of Flight	Yes	**Section 32.6.7 “Time of Flight Measure Mode”**
0111	Capture	Yes	**Section 32.6.8 “Capture Mode”**
1000	Counter	No	**Section 32.6.9 “Counter Mode”**
1001	Gated Counter	No	**Section 32.6.10 “Gated Counter Mode”**
1010	Windowed Counter	No	**Section 32.6.11 “Windowed Counter Mode”**
1011-1111	Reserved	—	—

FIGURE 32-18: COUNTER MODE TIMING DIAGRAM



REGISTER 32-3: SMTxSTAT: SMT STATUS REGISTER

R/W/HC-0/0	R/W/HC-0/0	R/W/HC-0/0	U-0	U-0	R-0/0	R-0/0	R-0/0
CPRUP	CPWUP	RST	—	—	TS	WS	AS
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **CPRUP:** SMT Manual Period Buffer Update bit
1 = Request update to SMTxPRx registers
0 = SMTxPRx registers update is complete

bit 6 **CPWUP:** SMT Manual Pulse Width Buffer Update bit
1 = Request update to SMTxCPW registers
0 = SMTxCPW registers update is complete

bit 5 **RST:** SMT Manual Timer Reset bit
1 = Request Reset to SMTxTMR registers
0 = SMTxTMR registers update is complete

bit 4-3 **Unimplemented**: Read as ‘0’

bit 2 **TS:** SMT GO Value Status bit
1 = SMT timer is incrementing
0 = SMT timer is not incrementing

bit 1 **WS:** SMTxWIN Value Status bit
1 = SMT window is open
0 = SMT window is closed

bit 0 **AS:** SMT_signal Value Status bit
1 = SMT acquisition is in progress
0 = SMT acquisition is not in progress

33.3.5 RECEIVING A BREAK CHARACTER

The Enhanced EUSART module can receive a Break character in two ways.

The first method to detect a Break character uses the FERR bit of the RC1STA register and the received data as indicated by RCREG. The Baud Rate Generator is assumed to have been initialized to the expected baud rate.

A Break character has been received when:

- RCIF bit is set
- FERR bit is set
- RCREG = 00h

The second method uses the Auto-Wake-up feature described in **Section 33.3.3 "Auto-Wake-up on Break"**. By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Detect feature. For both methods, the user can set the ABDEN bit of the BAUD1CON register before placing the EUSART in Sleep mode.

FIGURE 33-9: SEND BREAK CHARACTER SEQUENCE

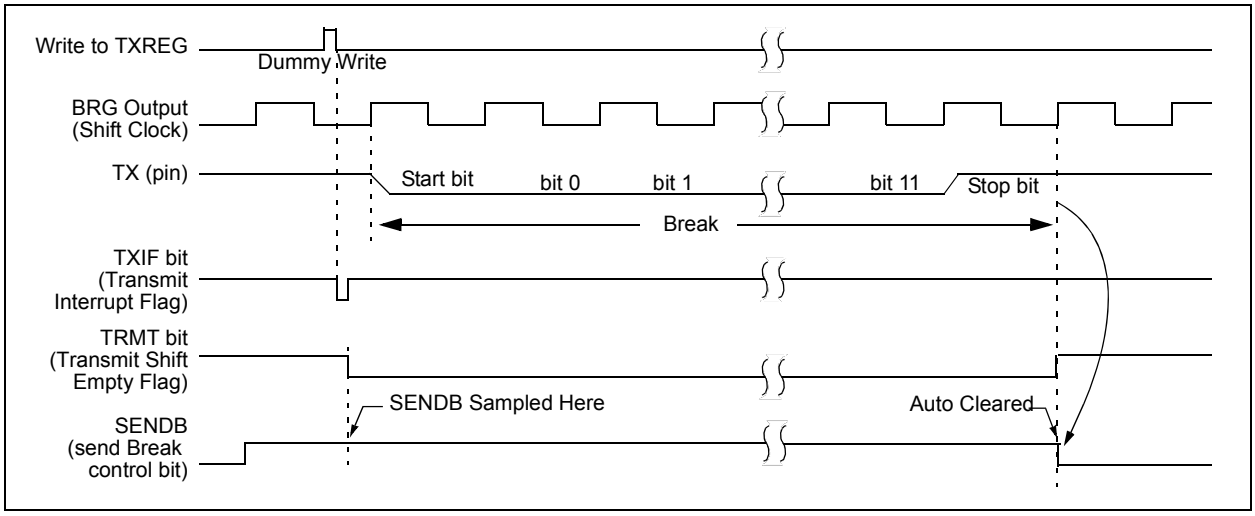


TABLE 37-11: RESET, WDT, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
RST01*	TMCLR	$\overline{\text{MCLR}}$ Pulse Width Low to ensure Reset	2	—	—	µs	
RST02*	TIOZ	I/O high-impedance from Reset detection	—	—	2	µs	
RST03	TWDT	Watchdog Timer Time-out Period	—	16	—	ms	16 ms Nominal Reset Time
RST04*	TPWRT	Power-up Timer Period	—	65	—	ms	
RST05	TOST	Oscillator Start-up Timer Period(1,2)	—	1024	—	TOSC	
RST06	VBOR	Brown-out Reset Voltage(4)	2.55 2.30 1.80	2.70 2.45 1.90	2.85 2.60 2.10	V V V	BORV = 0 BORV = 1 (PIC16F18856/76) BORV = 1 (PIC16LF18856/76)
RST07	VBORHYS	Brown-out Reset Hysteresis	—	40	—	mV	
RST08	TBORDC	Brown-out Reset Response Time	—	3	—	µs	
RST09	VLPBOR	Low-Power Brown-out Reset Voltage	2.3	2.45	2.7	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.

2: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

TABLE 37-12: ANALOG-TO-DIGITAL CONVERTER (ADC) ACCURACY SPECIFICATIONS(1,2):

Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = 25°C							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	10	bit	
AD02	EIL	Integral Error	—	±0.1	±1.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD03	EDL	Differential Error	—	±0.1	±1.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD04	EOFF	Offset Error	—	0.5	2.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD05	EGN	Gain Error	—	±0.2	±1.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD06	VADREF	ADC Reference Voltage (ADREF+ - ADREF-)	1.8	—	VDD	V	
AD07	VAIN	Full-Scale Range	ADREF-	—	ADREF+	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	10	—	kΩ	
AD09	RVREF	ADC Voltage Reference Ladder Impedance	—	50	—	kΩ	**Note 3**

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error is the sum of the offset, gain and integral non-linearity (INL) errors.

2: The ADC conversion result never decreases with an increase in the input and has no missing codes.

3: This is the impedance seen by the VREF pads when the external reference pads are selected.

TABLE 37-25: I^2C BUS DATA REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
SP100*	THIGH	Clock high time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	1.5TCY	—		
SP101*	TLOW	Clock low time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	1.5TCY	—		
SP102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1CB	300	ns	CB is specified to be from 10-400 pF
SP103*	TF	SDA and SCL fall time	100 kHz mode	—	250	ns	
			400 kHz mode	20 + 0.1CB	250	ns	CB is specified to be from 10-400 pF
SP106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
SP107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
SP109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	**(Note 1)**
			400 kHz mode	—	—	ns	
SP110*	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
SP111	CB	Bus capacitive loading		—	400	pF	

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I^2C bus device can be used in a Standard mode (100 kHz) I^2C bus system, but the requirement $T_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line T_R max. + $T_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification), before the SCL line is released.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

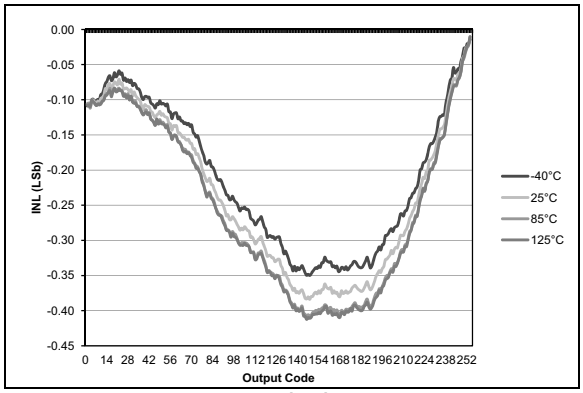


FIGURE 38-61: *Typical DAC INL Error, VDD = 5.0V, VREF = External 5V, PIC16F18856/76 Only.*

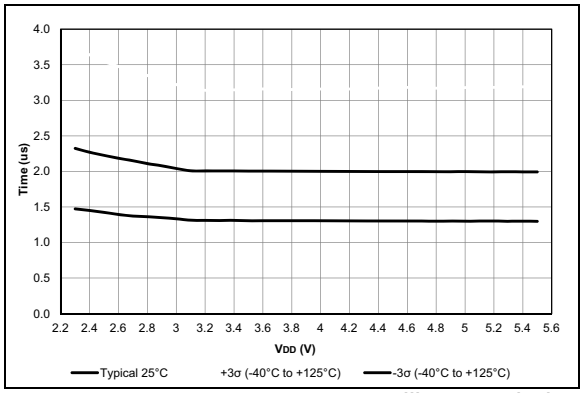


FIGURE 38-64: *ADC RC Oscillator Period, PIC16F18856/76 Only.*

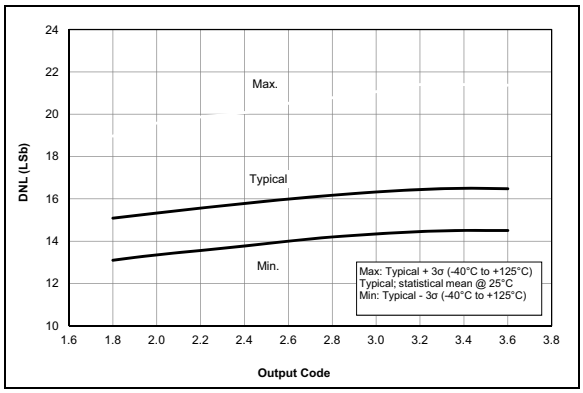


FIGURE 38-62: *DAC INL Error, VDD = 3.0V, PIC16LF18856/76 Only.*

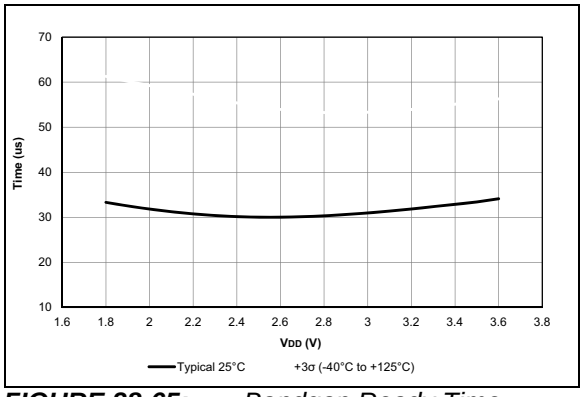


FIGURE 38-65: *Bandgap Ready Time, PIC16LF18856/76 Only.*

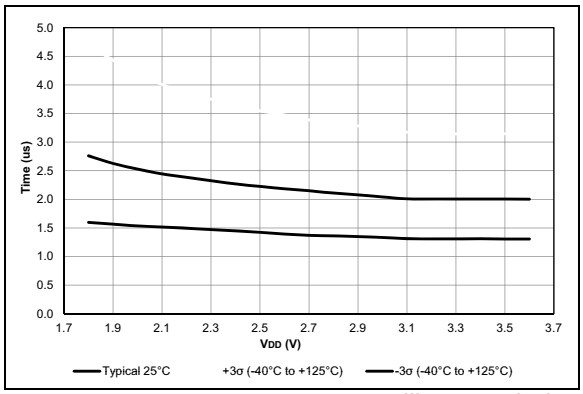


FIGURE 38-63: *ADC RC Oscillator Period, PIC16LF18856/76 Only.*

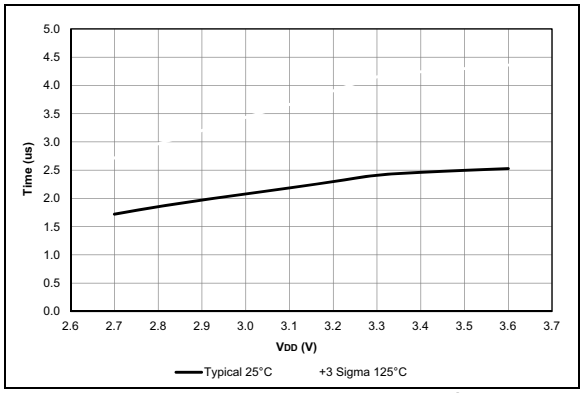
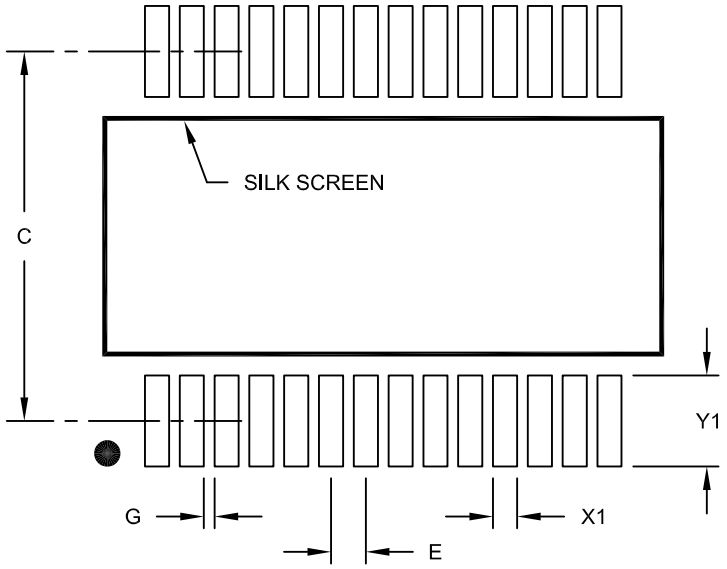


FIGURE 38-66: *BOR Response Time, PIC16LF18856/76 Only.*

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A