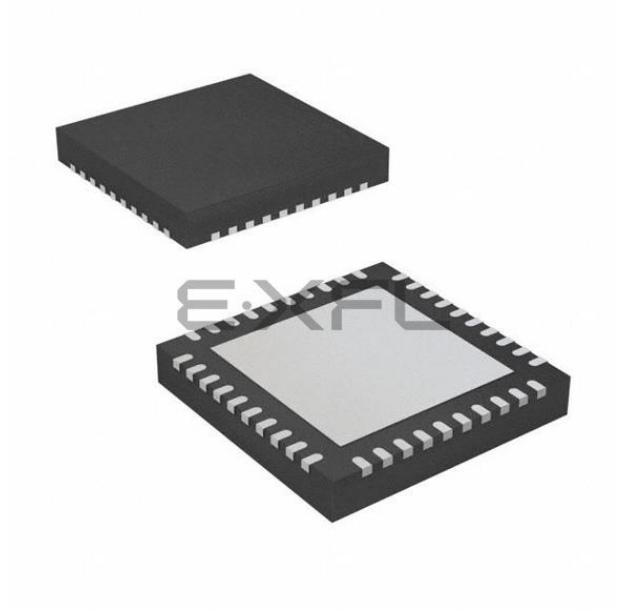

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Product Status	Active
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Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18876-i-mv

TABLE 3: 40/44-PIN ALLOCATION TABLE (PIC16(L)F18876)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	ADC	Voltage Reference	DAC	Comparators	Zero-Cross Detect	MSSP (SPI/I2C)	EUSART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RA0	2	17	19	19	ANA0	—	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	CLCIN0(1)	—	—	IOCA0	—
RA1	3	18	20	20	ANA1	—	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	CLCIN1(1)	—	—	IOCA1	—
RA2	4	19	21	21	ANA2	VREF-	DAC1OUT1	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—	IOCA2	—
RA3	5	20	22	22	ANA3	VREF+	—	C1IN1+	—	—	—	MDCARL(1)	—	—	—	—	—	—	IOCA3	—
RA4	6	21	23	23	ANA4	—	—	—	—	—	—	MDCARH(1)	T0CKI(1)	CCP5(1)	—	—	—	—	IOCA4	—
RA5	7	22	24	24	ANA5	—	—	—	—	SS1(1)	—	MDSRC(1)	—	—	—	—	—	—	IOCA5	—
RA6	14	29	33	31	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA6	OSC2 CLKOUT
RA7	13	28	32	30	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA7	OSC1 CLKIN
RB0	33	8	9	8	ANB0	—	—	C2IN1+	ZCD	SS2(1)	—	—	—	CCP4(1)	CWG1IN(1)	—	—	—	INT(1) IOCB0	—
RB1	34	9	10	9	ANB1	—	—	C1IN3- C2IN3-	—	SCL2(3,4) SCK2(1)	—	—	—	—	CWG2IN(1)	—	—	—	IOCB1	—
RB2	35	10	11	10	ANB2	—	—	—	—	SDA2(3,4) SDI2(1)	—	—	—	—	CWG3IN(1)	—	—	—	IOCB2	—
RB3	36	11	12	11	ANB3	—	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	IOCB3	—
RB4	37	12	14	14	ANB4 ADCACT(1)	—	—	—	—	—	—	—	T5G(1) SMTWIN2(1)	—	—	—	—	—	IOCB4	—
RB5	38	13	15	15	ANB5	—	—	—	—	—	—	—	T1G(1) SMTSIG2(1)	CCP3(1)	—	—	—	—	IOCB5	—
RB6	39	14	16	16	ANB6	—	—	—	—	—	—	—	—	—	—	CLCIN2(1)	—	—	IOCB6	ICSPCLK
RB7	40	15	17	17	ANB7	—	DAC1OUT2	—	—	—	—	—	T6IN(1)	—	—	CLCIN3(1)	—	—	IOCB7	ICSPDAT

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 13-1 for details on which port pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 13-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I2C logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I2C specific or SMbus input buffer thresholds.

1.0 DEVICE OVERVIEW

The PIC16(L)F18856/76 are described within this data sheet. The PIC16(L)F18856 devices are available in 28-pin SPDIP, SSOP, SOIC, and UQFN packages. The PIC16(L)F18876 devices are available in 40-pin PDIP and UQFN and 44-pin TQFP and QFN packages.

Figure 1-1 shows a block diagram of the PIC16(L)F18856/76 devices. Table 1-2 and Table 1-3 show the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F18856	PIC16(L)F18856
Analog-to-Digital Converter with Computation (ADC^2)		•	•
Cyclic Redundancy Check (CRC)		•	•
Digital-to-Analog Converter (DAC)		•	•
Fixed Voltage Reference (FVR)		•	•
Enhanced Universal Synchronous/Asynchronous Receiver/ Transmitter (EUSART1)		•	•
Digital Signal Modulator (DSM)		•	•
Numerically Controlled Oscillator (NCO1)		•	•
Temperature Indicator		•	•
Zero-Cross Detect (ZCD)		•	•
Capture/Compare/PWM (CCP/ECCP) Modules			
	CCP1	•	•
	CCP2	•	•
	CCP3	•	•
	CCP4	•	•
	CCP5	•	•
Comparators			
	C1	•	•
	C2	•	•
Configurable Logic Cell (CLC)			
	CLC1	•	•
	CLC2	•	•
	CLC3	•	•
	CLC4	•	•
Complementary Waveform Generator (CWG)			
	CWG1	•	•
	CWG2	•	•
	CWG3	•	•
Master Synchronous Serial Ports			
	MSSP1	•	•
	MSSP2	•	•
Pulse-Width Modulator (PWM)			
	PWM6	•	•
	PWM7	•	•
Signal Measure Timer (SMT)			
	SMT1	•	•
	SMT2	•	•
Timers			
	Timer0	•	•
	Timer1	•	•
	Timer2	•	•
	Timer3	•	•
	Timer4	•	•
	Timer5	•	•
	Timer6	•	•

TABLE 1-2: PIC16F18856 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/ANC4/SDA1(3,4)/SDI1(1)/IOCC4	RC4	TTL/ST	CMOS/OD	General purpose I/O.
	ANC4	AN	—	ADC Channel C4 input.
	SDA1(3,4)	I2C/ SMBus	OD	MSSP1 I2C serial data input/output.
	SDI1(1)	TTL/ST	—	MSSP1 SPI serial data input.
	IOCC4	TTL/ST	—	Interrupt-on-change input.
RC5/ANC5/T4IN(1)/IOCC5	RC5	TTL/ST	CMOS/OD	General purpose I/O.
	ANC5	AN	—	ADC Channel C5 input.
	T4IN(1)	TTL/ST	—	Timer4 external input.
	IOCC5	TTL/ST	—	Interrupt-on-change input.
RC6/ANC6/CK(3)/IOCC6	RC6	TTL/ST	CMOS/OD	General purpose I/O.
	ANC6	AN	—	ADC Channel C6 input.
	CK(3)	TTL/ST	CMOS/OD	EUSART synchronous mode clock input/output.
	IOCC6	TTL/ST	—	Interrupt-on-change input.
RC7/ANC7/RX(1)/DT(3)/IOCC7	RC7	TTL/ST	CMOS/OD	General purpose I/O.
	ANC7	AN	—	ADC Channel C7 input.
	RX(1)	TTL/ST	—	EUSART Asynchronous mode receiver data input.
	DT(3)	TTL/ST	CMOS/OD	EUSART Synchronous mode data input/output.
	IOCC7	TTL/ST	—	Interrupt-on-change input.
RE3/IOCE3/$\overline{MCLR}$/VPP	RE3	TTL/ST	—	General purpose input only (when $\overline{MCLR}$ is disabled by the Configuration bit).
	IOCE3	TTL/ST	—	Interrupt-on-change input.
	$\overline{MCLR}$	ST	—	Master clear input with internal weak pull up resistor.
	VPP	HV	—	ICSP™ High-Voltage Programming mode entry input.
VDD	VDD	Power	—	Positive supply voltage input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 13-1 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 13-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 6-1: NOSC/COSC BIT SETTINGS

NOSC<2:0>/ COSC<2:0>	Clock Source
111	EXTOSC(1)
110	HFINTOSC(2)
101	LFINTOSC
100	SOSC
011	Reserved (it operates like NOSC = 110)
010	EXTOSC with 4x PLL(1)
001	HFINTOSC with 2x PLL(1)
000	Reserved (it operates like NOSC = 110)

Note 1: EXTOSC configured by the FEXTOSC bits of Configuration Word 1 (Register 4-1).

2: HFINTOSC settings are configured with the HFFRQ bits of the OSCFRQ register (Register 6-6).

TABLE 6-2: NDIV/CDIV BIT SETTINGS

NDIV<3:0>/ CDIV<3:0>	Clock divider
1111-1010	Reserved
1001	512
1000	256
0111	128
0110	64
0101	32
0100	16
0011	8
0010	4
0001	2
0000	1

REGISTER 6-3: OSCCON3: OSCILLATOR CONTROL REGISTER 3

R/W/HC-0/0	R/W-0/0	U-0	R-0/0	R-0/0	U-0	U-0	U-0
CSWHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **CSWHOLD:** Clock Switch Hold bit
- 1 = Clock switch will hold (with interrupt) when the oscillator selected by NOSC is ready
- 0 = Clock switch may proceed when the oscillator selected by NOSC is ready; if this bit is clear at the time that NOSCR becomes ‘1’, the switch will occur

bit 6 **SOSCPWR:** Secondary Oscillator Power Mode Select bit
- 1 = Secondary oscillator operating in High-power mode
- 0 = Secondary oscillator operating in Low-power mode

bit 5 **Unimplemented:** Read as ‘0’.

bit 4 **ORDY:** Oscillator Ready bit (read-only)
- 1 = OSCCON1 = OSCCON2; the current system clock is the clock specified by NOSC
- 0 = A clock switch is in progress

bit 3 **NOSCR:** New Oscillator is Ready bit (read-only)
- 1 = A clock switch is in progress and the oscillator selected by NOSC indicates a “ready” condition
- 0 = A clock switch is not in progress, or the NOSC-selected oscillator is not yet ready

bit 2-0 **Unimplemented:** Read as ‘0’

TABLE 13-3: PPS OUTPUT SIGNAL ROUTING OPTIONS

Output Signal Name	RxyPPS Register Value	Remappable to Pins of PORTx							
		PIC16F18856			PIC16F18876				
		PORTA	PORTB	PORTC	PORTA	PORTB	PORTC	PORTD	PORTE
ADGRDG	0x25	●		●	●		●		
ADGRDA	0x24	●		●	●		●		
CWG3D	0x23	●		●	●			●	
CWG3C	0x22	●		●	●			●	
CWG3B	0x21	●		●	●				●
CWG3A	0x20		●	●		●	●		
CWG2D	0x1F		●	●		●		●	
CWG2C	0x1E		●	●		●		●	
CWG2B	0x1D		●	●		●		●	
CWG2A	0x1C		●	●		●	●		
DSM	0x1B	●		●	●			●	
CLKR	0x1A		●	●		●	●		
NCO	0x19	●		●	●			●	
TMR0	0x18		●	●		●	●		
SDO2/SDA2	0x17		●	●		●		●	
SCK2/SCL2	0x16		●	●		●		●	
SD01/SDA1	0x15		●	●		●	●		
SCK1/SCL1	0x14		●	●		●	●		
C2OUT	0x13	●		●	●				●
C1OUT	0x12	●		●	●			●	
DT	0x11		●	●		●	●		
TX/CK	0x10		●	●		●	●		
PWM7OUT	0x0F	●		●	●		●		
PWM6OUT	0x0E	●		●	●			●	
CCP5	0x0D	●		●	●				●
CCP4	0x0C		●	●		●		●	
CCP3	0x0B		●	●		●		●	
CCP2	0x0A		●	●		●	●		
CCP1	0x09		●	●		●	●		
CWG1D	0x08		●	●		●		●	
CWG1C	0x07		●	●		●		●	
CWG1B	0x06		●	●		●		●	
CWG1A	0x05		●	●		●	●		
CLC4OUT	0x04		●	●		●		●	
CLC3OUT	0x03		●	●		●		●	
CLC2OUT	0x02	●		●	●		●		
CLC1OUT	0x01	●		●	●		●		

Note: When RxyPPS = 0x00, port pin Rxy output value is controlled by the respective LATxy bit.

REGISTER 13-2: RxyPPS: PIN Rxy OUTPUT SOURCE SELECTION REGISTER

U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	RxyPPS<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RxyPPS<5:0>:** Pin Rxy Output Source Selection bits
See Table 13-2.

Note 1: TRIS control is overridden by the peripheral as required.

REGISTER 13-3: PPSLOCK: PPS LOCK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0
—	—	—	—	—	—	—	PPSLOCKED
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-1 **Unimplemented:** Read as ‘0’

bit 0 **PPSLOCKED:** PPS Locked bit
1= PPS is locked. PPS selections can not be changed.
0= PPS is not locked. PPS selections can be changed.

17.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 μs after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μs between consecutive conversions of the temperature indicator output.

TABLE 17-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDFVR<1:0>		ADFVR<1:0>		269

Legend: Shaded cells are unused by the Temperature Indicator module.

REGISTER 24-2: NCO1CLK: NCO1 INPUT CLOCK CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
N1PWS<2:0>(1,2)			—	—	N1CKS<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **N1PWS<2:0>:** NCO1 Output Pulse Width Select bits(1,2)
- 111 = NCO1 output is active for 128 input clock periods
- 110 = NCO1 output is active for 64 input clock periods
- 101 = NCO1 output is active for 32 input clock periods
- 100 = NCO1 output is active for 16 input clock periods
- 011 = NCO1 output is active for 8 input clock periods
- 010 = NCO1 output is active for 4 input clock periods
- 001 = NCO1 output is active for 2 input clock periods
- 000 = NCO1 output is active for 1 input clock period

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **N1CKS<2:0>:** NCO1 Clock Source Select bits
- 110 = Reserved
- •
- •
- •
- 111 = Reserved
- 101 = LC4_out
- 100 = LC3_out
- 011 = LC2_out
- 010 = LC1_out
- 001 = HFINTOSC
- 000 = FOSC

Note 1: N1PWS applies only when operating in Pulse Frequency mode.
2: If NCO1 pulse width is greater than NCO1 overflow period, operation is undefined.

26.5 Carrier Source Polarity Select

The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high source is enabled by setting the MDCHPOL bit of the MDCON1 register. Inverting the signal for the carrier low source is enabled by setting the MDCLPOL bit of the MDCON1 register.

26.6 Programmable Modulator Data

The MDBIT of the MDCON0 register can be selected as the source for the modulator signal. This gives the user the ability to program the value used for modulation.

26.7 Modulated Output Polarity

The modulated output signal provided on the DSM pin can also be inverted. Inverting the modulated output signal is enabled by setting the MDOPOL bit of the MDCON0 register.

26.8 Slew Rate Control

The slew rate limitation on the output port pin can be disabled. The slew rate limitation can be removed by clearing the SLR bit of the SLRCON register associated with that pin. For example, clearing the slew rate limitation for pin RA5 would require clearing the SLRA5 bit of the SLRCONA register.

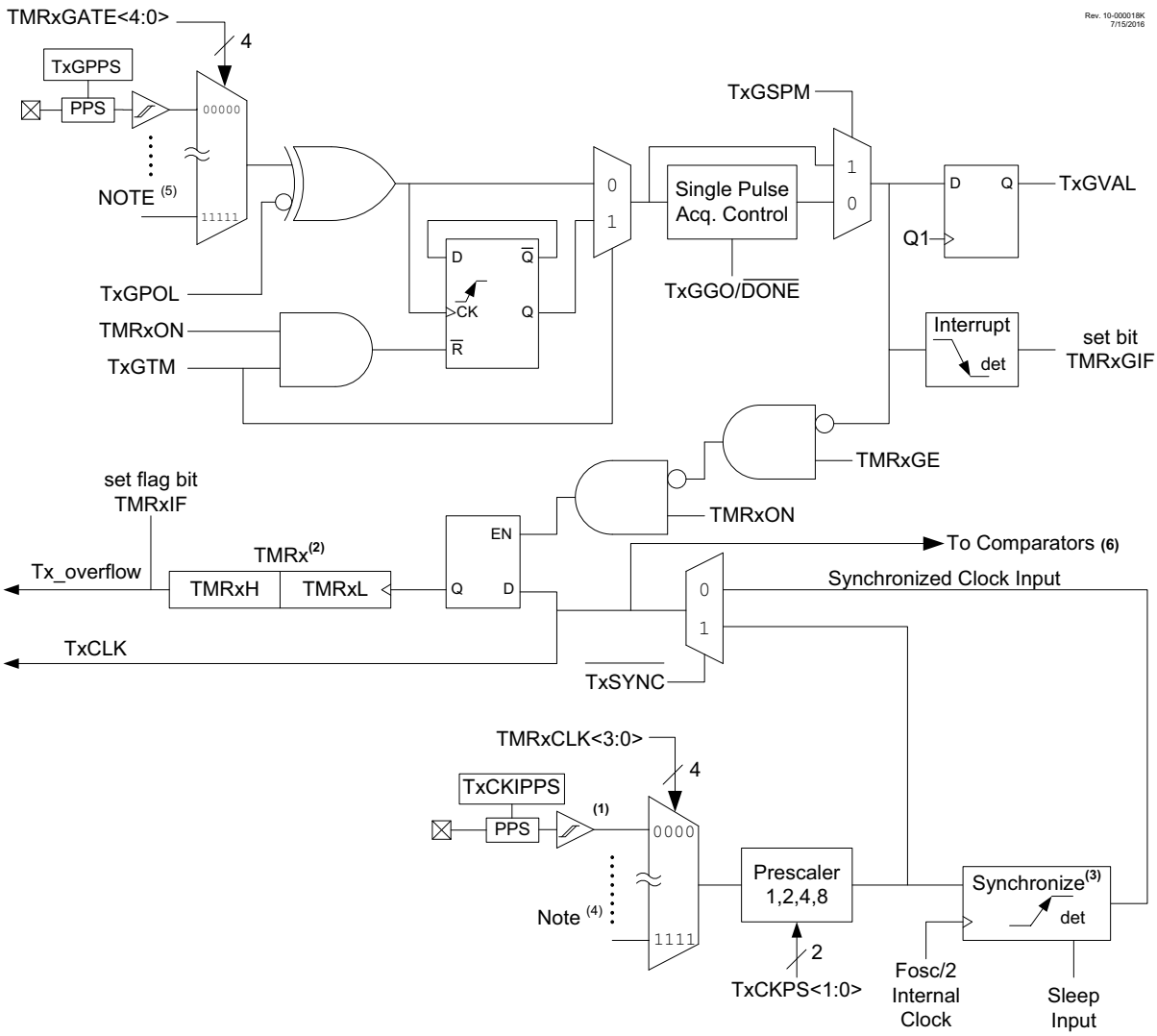
26.9 Operation in Sleep Mode

The DSM module is not affected by Sleep mode. The DSM can still operate during Sleep, if the Carrier and Modulator input sources are also still operable during Sleep.

26.10 Effects of a Reset

Upon any device Reset, the DSM module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

FIGURE 28-1: TIMER1 BLOCK DIAGRAM



Note 1: ST Buffer is high speed type when using TxCKIPPS.
2: TMRx register increments on rising edge.
3: Synchronize does not operate while in Sleep.
4: See Register 28-3 for Clock source selections.
5: See Register 28-4 for GATE source selections.
6: Synchronized comparator output should not be used in conjunction with synchronized input clock.

28.8 Timer1 Interrupts

The timer register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When the timer rolls over, the respective timer interrupt flag bit of the PIR5 register is set. To enable the interrupt on rollover, you must set these bits:

- ON bit of the T1CON register
- TMR1IE bit of the PIE4 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note:	To avoid immediate interrupt vectoring, the TMR1H:TMR1L register pair should be preloaded with a value that is not imminently about to rollover, and the TMR1IF flag should be cleared prior to enabling the timer interrupts.

28.9 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- ON bit of the T1CON register must be set
- TMR1IE bit of the PIE4 register must be set
- PEIE bit of the INTCON register must be set
- $\overline{\text{SYNC}}$ bit of the T1CON register must be set
- CLK bits of the T1CLK register must be configured
- The timer clock source must be enabled and continue operation during sleep. When the SOSC is used for this purpose, the SOSCEN bit of the OSCEN register must be set.

The device will wake-up on an overflow and execute the next instructions. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine.

Secondary oscillator will continue to operate in Sleep regardless of the $\overline{\text{SYNC}}$ bit setting.

28.10 CCP Capture/Compare Time Base

The CCP modules use the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPRxH:CCPRxL register pair on a configured event.

In Compare mode, an event is triggered when the value CCPRxH:CCPRxL register pair matches the value in the TMR1H:TMR1L register pair. This event can be an Auto-conversion Trigger.

The Timer1 to CCP1/2/3/4/5 mapping is not fixed, and can be assigned on an individual CCP module basis. All of the CCP modules may be configured to share a single Timer1 (or Timer3, or Timer5) resource, or different CCP modules may be configured to use different Timer1 resources. This timer to CCP mapping selection is made in the CCPTMRS0 and CCPTMRS1 registers.

For more information, see **Section 30.0 “Capture/Compare/PWM Modules”**.

28.11 CCP Auto-Conversion Trigger

When any of the CCP’s are configured to trigger an auto-conversion, the trigger will clear the TMR1H:TMR1L register pair. This auto-conversion does not cause a timer interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPRxH:CCPRxL register pair becomes the period register for Timer1.

The timer should be synchronized and FOSC/4 should be selected as the clock source in order to utilize the Auto-conversion Trigger. Asynchronous operation of the timer can cause an Auto-conversion Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with an Auto-conversion Trigger from the CCP, the write will take precedence.

For more information, see **Section 30.2.4 “Compare During Sleep”**.

REGISTER 31-2: SSPxCON1: SSPx CONTROL REGISTER 1

R/C/HS-0/0	R/C/HS-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WCOL	SSPOV(1)	SSPEN	CKP	SSPM<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets	
'1' = Bit is set	'0' = Bit is cleared	HS = Bit is set by hardware	C = User cleared

bit 7 **WCOL:** Write Collision Detect bit (Transmit mode only)
1 = The SSPxBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6 **SSPOV:** Receive Overflow Indicator bit(1)
In SPI mode:
1 = A new byte is received while the SSPxBUF register is still holding the previous data. In case of overflow, the data in SSPxSR is lost. Overflow can only occur in Slave mode. In Slave mode, the user must read the SSPxBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPxBUF register (must be cleared in software).
0 = No overflow
In I^2C mode:
1 = A byte is received while the SSPxBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode (must be cleared in software).
0 = No overflow

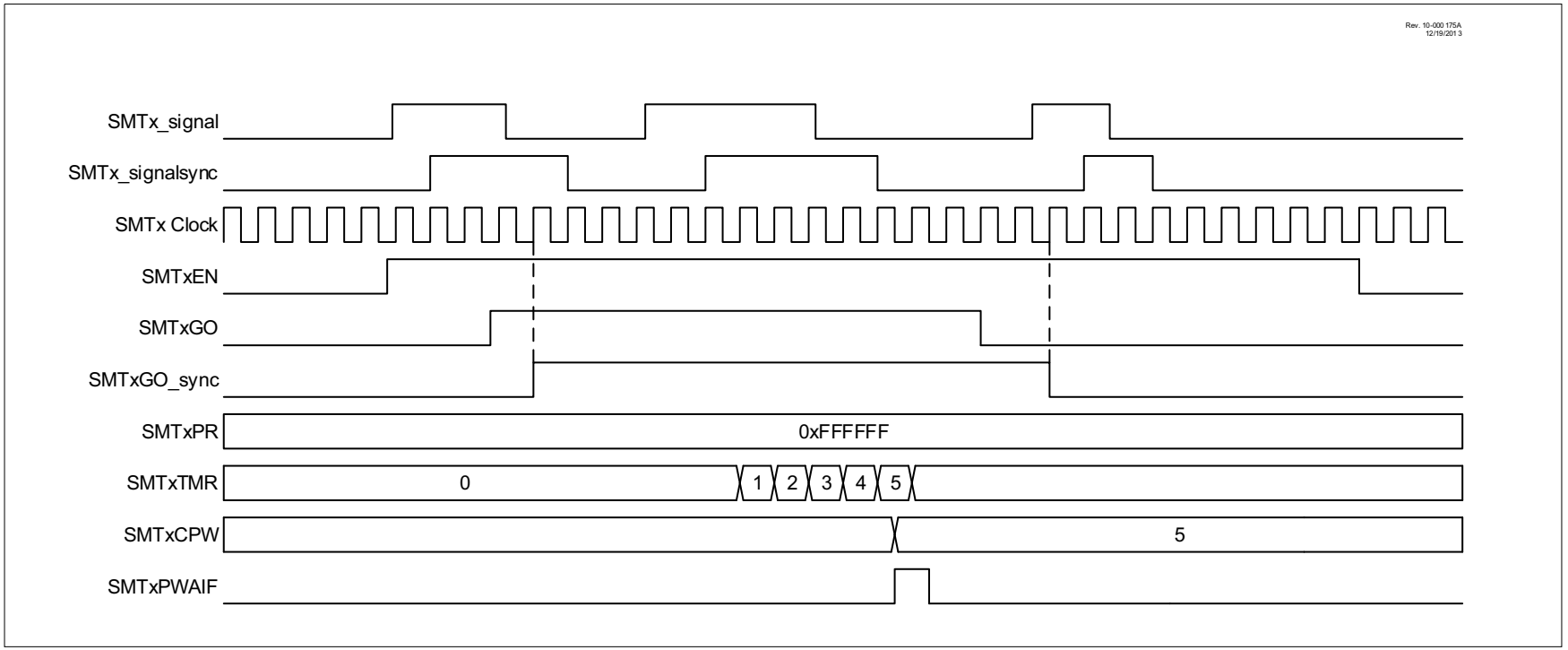
bit 5 **SSPEN:** Synchronous Serial Port Enable bit
In both modes, when enabled, the following pins must be properly configured as input or output
In SPI mode:
1 = Enables serial port and configures SCK, SDO, SDI and $\overline{SS}$ as the source of the serial port pins(2)
0 = Disables serial port and configures these pins as I/O port pins
In I^2C mode:
1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins(3)
0 = Disables serial port and configures these pins as I/O port pins

bit 4 **CKP:** Clock Polarity Select bit
In SPI mode:
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level
In I^2C Slave mode:
SCL release control
1 = Enable clock
0 = Holds clock low (clock stretch). (Used to ensure data setup time.)
In I^2C Master mode:
Unused in this mode

bit 3-0 **SSPM<3:0>:** Synchronous Serial Port Mode Select bits
1111 = I^2C Slave mode, 10-bit address with Start and Stop bit interrupts enabled
1110 = I^2C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1101 = Reserved
1100 = Reserved
1011 = I^2C firmware controlled Master mode (slave idle)
1010 = SPI Master mode, clock = FOSC/(4 * (SSPxADD+1))(5)
1001 = Reserved
1000 = I^2C Master mode, clock = FOSC / (4 * (SSPxADD+1))(4)
0111 = I^2C Slave mode, 10-bit address
0110 = I^2C Slave mode, 7-bit address
0101 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control disabled, $\overline{SS}$ can be used as I/O pin
0100 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control enabled
0011 = SPI Master mode, clock = T2_match/2
0010 = SPI Master mode, clock = FOSC/64
0001 = SPI Master mode, clock = FOSC/16
0000 = SPI Master mode, clock = FOSC/4

Note 1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPxBUF register.
2: When enabled, these pins must be properly configured as input or output. Use SSPxSSPPS, SSPxCLKPPS, SSPxDATPPS, and RxyPPS to select the pins.
3: When enabled, the SDA and SCL pins must be configured as inputs. Use SSPxCLKPPS, SSPxDATPPS, and RxyPPS to select the pins.
4: SSPxADD values of 0, 1 or 2 are not supported for I^2C mode.
5: SSPxADD value of '0' is not supported. Use SSPM = 0000 instead.

FIGURE 32-5: GATED TIMER MODE SINGLE ACQUISITION TIMING DIAGRAM



33.2 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as V_{DD} or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source. See **Section 6.2.2.2 "Internal Oscillator Frequency Adjustment"** for more information.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see **Section 33.3.1 "Auto-Baud Detect"**). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

33.4 EUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The EUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

33.4.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the EUSART for synchronous master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TX1STA register configures the device for synchronous operation. Setting the CSRC bit of the TX1STA register configures the device as a master. Clearing the SREN and CREN bits of the RC1STA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RC1STA register enables the EUSART.

33.4.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the EUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

33.4.1.2 Clock Polarity

A clock polarity option is provided for Microwire compatibility. Clock polarity is selected with the SCKP bit of the BAUD1CON register. Setting the SCKP bit sets the clock Idle state as high. When the SCKP bit is set, the data changes on the falling edge of each clock. Clearing the SCKP bit sets the Idle state as low. When the SCKP bit is cleared, the data changes on the rising edge of each clock.

33.4.1.3 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the EUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXREG register. If the TSR still contains all or part of a previous character the new character data is held in the TXREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

Note:	The TSR register is not mapped in data memory, so it is not available to the user.

33.4.1.4 Synchronous Master Transmission Set-up:

1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 33.3 “EUSART Baud Rate Generator (BRG)”**).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
3. Disable Receive mode by clearing bits SREN and CREN.
4. Enable Transmit mode by setting the TXEN bit.
5. If 9-bit transmission is desired, set the TX9 bit.
6. If interrupts are desired, set the TXIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
8. Start transmission by loading data to the TXREG register.

REGISTER 33-7: SP1BRGH(1, 2): BAUD RATE GENERATOR HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SP1BRG<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **SP1BRG<15:8>:** Upper eight bits of the Baud Rate Generator

Note 1: SPBRGH value is ignored for all modes unless BAUD1CON<BRG16> is active.

2: Writing to SPBRGH resets the BRG counter.

FIGURE 37-11: ADC CONVERSION TIMING (ADC CLOCK FRC-BASED)

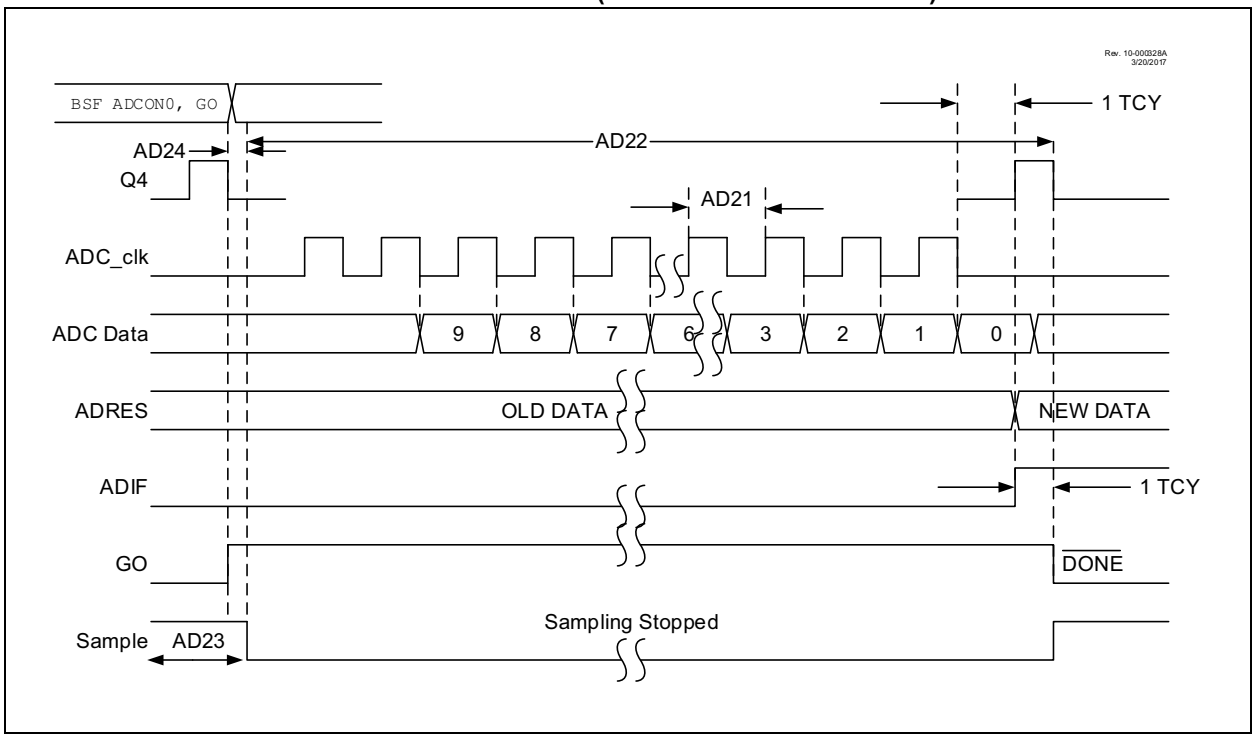


FIGURE 37-19: SPI SLAVE MODE TIMING (CKE = 0)

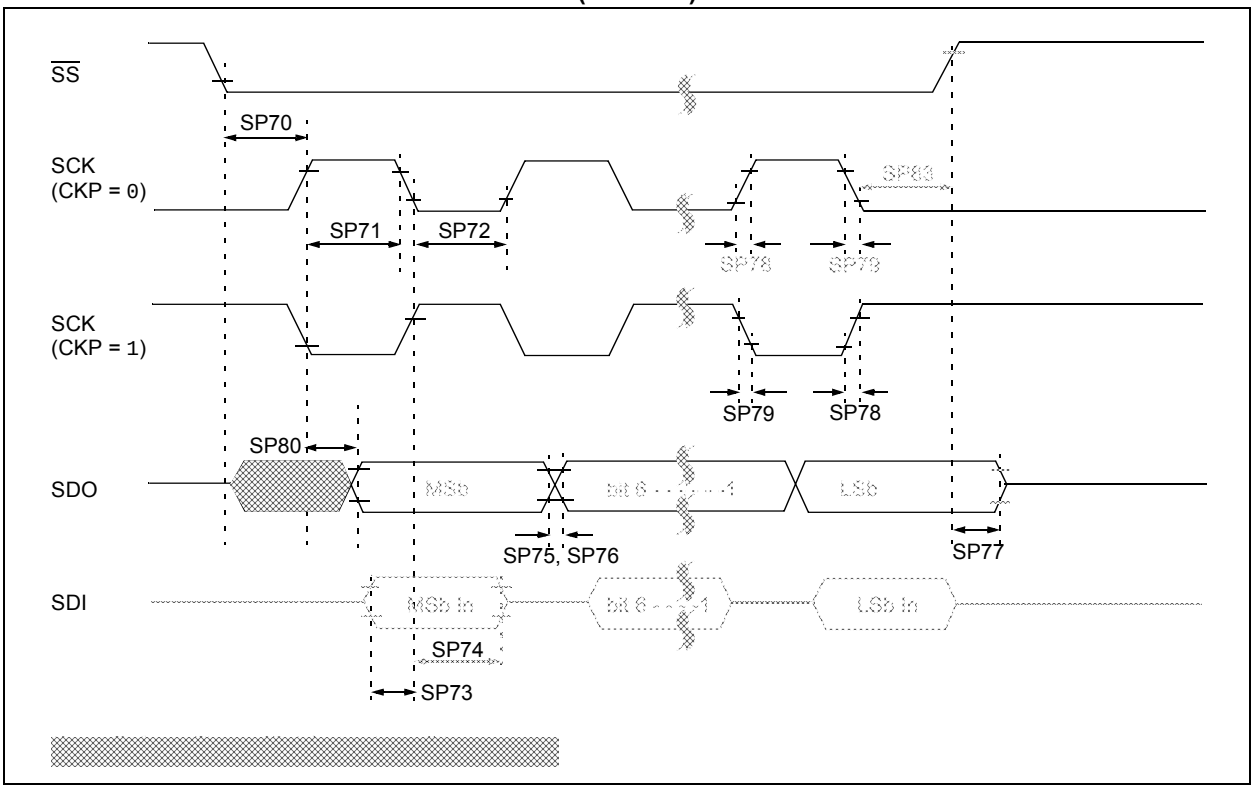
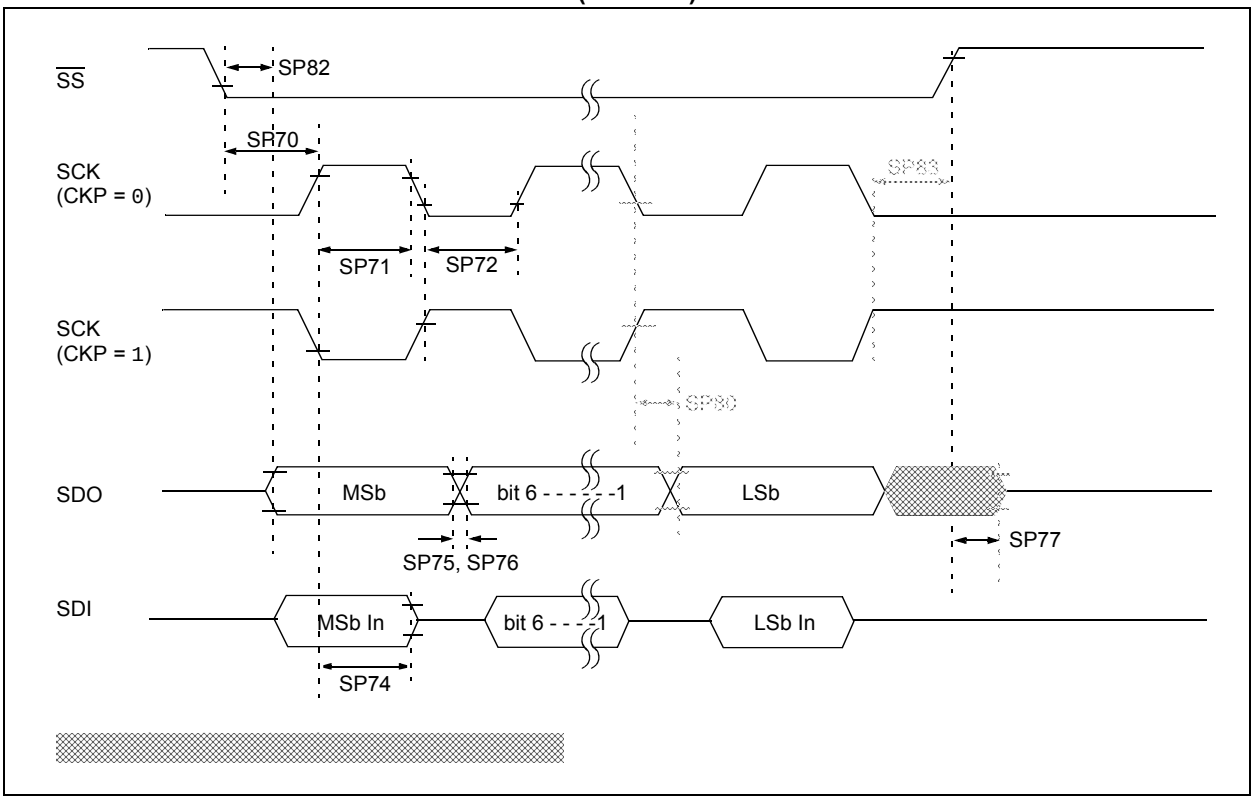
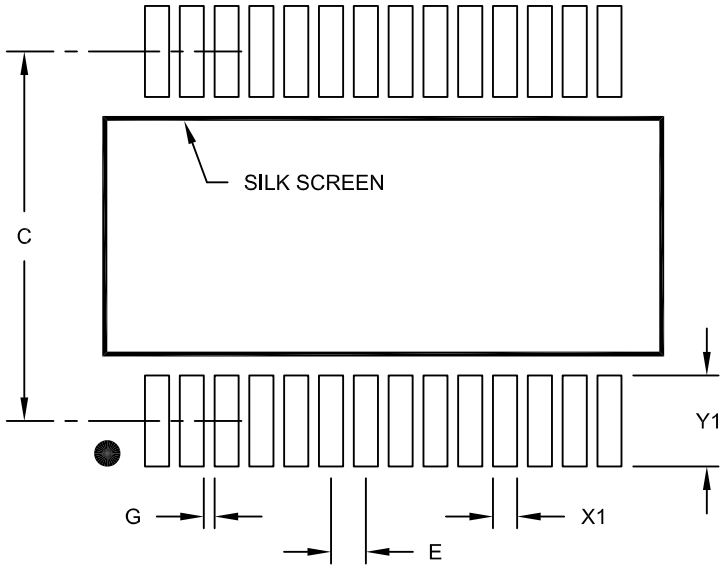


FIGURE 37-20: SPI SLAVE MODE TIMING (CKE = 1)



28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (01/2016)

Initial release of the document.

Revision B (04/2017)

Removed Preliminary Status - Added Char Graphs; Updated Figures 6-1, 23-2, 27-1, 28-1, 29-2, 29-3, 29-8, 29-9, 29-10, 29-11, 29-12, 29-13, 32-14, 32-15, 32-18, and 37-10; Registers 4-1, 4-3, 6-3, 8-2, 9-2, 12-2, 12-4, 12-6, 12-12, 12-14, 12-16, 12-32, 12-33, 12-34, 12-35, 12-36, 12-37, 12-43, 12-45, 12-49, 20-9, 23-1, 23-3, 23-4, 27-2, 28-1, 28-3, 29-1, 31-4, 31-5, 31-6, 34-1, and 34-2; Sections 9.1, 10.4.3, 21.5, 23.1.1, 23.1.4, 23.4.4, 23.5.2, 23.5.3, 29.1, 29.2, 31.6, 32.1.1, 32.6.9, 34.2, and 34.4; Tables 3-5, 3-6, 3-7, 10-2, 20-2, 23-1, 31-3, 36-4, 37-3, 37-5, 37-11 and 37-13.

Added Figure 37-11. Added Section 6.2.2.4 MFINTOSC, 21.5.1 Correction by AC Coupling. Added Section 28.4: Timer1 16-Bit Read/Write Mode.

Updated Instruction Sets MOVWF and NOP.

Removed Figure 37-11.