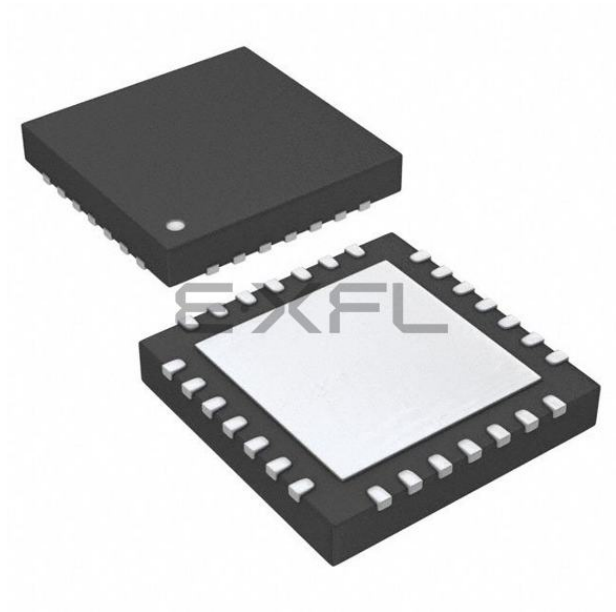

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18856-e-mv

TABLE 3: 40/44-PIN ALLOCATION TABLE (PIC16(L)F18876) (CONTINUED)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	ADC	Voltage Reference	DAC	Comparators	Zero-Cross Detect	MSSP (SPI/I^2C)	EUSART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	$\overline{MCLR}$ V_{PP}
V_{DD}	11, 32	7, 26	8, 28	7, 28	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
V_{SS}	12, 31	6, 27	6, 31, 30	6, 29	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT(2)	—	—	—	—	ADGRDA ADGRDB	—	—	C1OUT C2OUT	—	SDO1 SCK1 SDO2 SCK2	TX/ CK(3) DT(3)	DSM	TMR0	CCP1 CCP2 CCP3 CCP4 CCP5 PWM6OUT PWM7OUT	CWG1A CWG1B CWG1C CWG1D CWG2A CWG2B CWG2C CWG2D CWG3A CWG3B CWG3C CWG3D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	NCO	CLKR	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 13-1 for details on which port pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 13-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMbus input buffer thresholds.

1.0 DEVICE OVERVIEW

The PIC16(L)F18856/76 are described within this data sheet. The PIC16(L)F18856 devices are available in 28-pin SPDIP, SSOP, SOIC, and UQFN packages. The PIC16(L)F18876 devices are available in 40-pin PDIP and UQFN and 44-pin TQFP and QFN packages.

Figure 1-1 shows a block diagram of the PIC16(L)F18856/76 devices. Table 1-2 and Table 1-3 show the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F18856	PIC16(L)F18856
Analog-to-Digital Converter with Computation (ADC^2)		•	•
Cyclic Redundancy Check (CRC)		•	•
Digital-to-Analog Converter (DAC)		•	•
Fixed Voltage Reference (FVR)		•	•
Enhanced Universal Synchronous/Asynchronous Receiver/ Transmitter (EUSART1)		•	•
Digital Signal Modulator (DSM)		•	•
Numerically Controlled Oscillator (NCO1)		•	•
Temperature Indicator		•	•
Zero-Cross Detect (ZCD)		•	•
Capture/Compare/PWM (CCP/ECCP) Modules			
	CCP1	•	•
	CCP2	•	•
	CCP3	•	•
	CCP4	•	•
	CCP5	•	•
Comparators			
	C1	•	•
	C2	•	•
Configurable Logic Cell (CLC)			
	CLC1	•	•
	CLC2	•	•
	CLC3	•	•
	CLC4	•	•
Complementary Waveform Generator (CWG)			
	CWG1	•	•
	CWG2	•	•
	CWG3	•	•
Master Synchronous Serial Ports			
	MSSP1	•	•
	MSSP2	•	•
Pulse-Width Modulator (PWM)			
	PWM6	•	•
	PWM7	•	•
Signal Measure Timer (SMT)			
	SMT1	•	•
	SMT2	•	•
Timers			
	Timer0	•	•
	Timer1	•	•
	Timer2	•	•
	Timer3	•	•
	Timer4	•	•
	Timer5	•	•
	Timer6	•	•

TABLE 1-2: PIC16F18856 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/ANC4/SDA1(3,4)/SDI1(1)/IOCC4	RC4	TTL/ST	CMOS/OD	General purpose I/O.
	ANC4	AN	—	ADC Channel C4 input.
	SDA1(3,4)	I2C/ SMBus	OD	MSSP1 I2C serial data input/output.
	SDI1(1)	TTL/ST	—	MSSP1 SPI serial data input.
	IOCC4	TTL/ST	—	Interrupt-on-change input.
RC5/ANC5/T4IN(1)/IOCC5	RC5	TTL/ST	CMOS/OD	General purpose I/O.
	ANC5	AN	—	ADC Channel C5 input.
	T4IN(1)	TTL/ST	—	Timer4 external input.
	IOCC5	TTL/ST	—	Interrupt-on-change input.
RC6/ANC6/CK(3)/IOCC6	RC6	TTL/ST	CMOS/OD	General purpose I/O.
	ANC6	AN	—	ADC Channel C6 input.
	CK(3)	TTL/ST	CMOS/OD	EUSART synchronous mode clock input/output.
	IOCC6	TTL/ST	—	Interrupt-on-change input.
RC7/ANC7/RX(1)/DT(3)/IOCC7	RC7	TTL/ST	CMOS/OD	General purpose I/O.
	ANC7	AN	—	ADC Channel C7 input.
	RX(1)	TTL/ST	—	EUSART Asynchronous mode receiver data input.
	DT(3)	TTL/ST	CMOS/OD	EUSART Synchronous mode data input/output.
	IOCC7	TTL/ST	—	Interrupt-on-change input.
RE3/IOCE3/$\overline{MCLR}$/VPP	RE3	TTL/ST	—	General purpose input only (when $\overline{MCLR}$ is disabled by the Configuration bit).
	IOCE3	TTL/ST	—	Interrupt-on-change input.
	$\overline{MCLR}$	ST	—	Master clear input with internal weak pull up resistor.
	VPP	HV	—	ICSP™ High-Voltage Programming mode entry input.
VDD	VDD	Power	—	Positive supply voltage input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 13-1 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 13-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18856	PIC16(L)F18876	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Banks 12													
CPU CORE REGISTERS; see Table 3-2 for specifics													
60Ch	CWG1CLKCON			—	—	—	—	—	—	—	CS	---- ---0	---- ---0
60Dh	CWG1ISM			—	—	—	—	IS<3:0>				---- 0000	---- 0000
60Eh	CWG1DBR			—	—	DBR<5:0>						--00 0000	--00 0000
60Fh	CWG1DBF			—	—	DBF<5:0>						--00 0000	--00 0000
610h	CWG1CON0			EN	LD	—	—	—	MODE<2:0>			00-- -000	00-- -000
611h	CWG1CON1			—	—	IN	—	POLD	POLC	POLB	POLA	--x- 0000	--u- 0000
612h	CWG1AS0			SHUTDOWN	REN	LSBD<1:0>		LSAC<1:0>		—	—	0001 01--	0001 01--
613h	CWG1AS1			—	AS6E	AS5E	AS4E	AS3E	AS2E	AS1E	AS0E	-000 0000	-000 0000
614h	CWG1STR			OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	0000 0000	0000 0000
615h	—	—		Unimplemented								—	—
616h	CWG2CLKCON			—	—	—	—	—	—	—	CS	---- ---0	---- ---0
617h	CWG2ISM			—	—	—	—	IS<3:0>				---- 0000	---- 0000
618h	CWG2DBR			—	—	DBR<5:0>						--00 0000	--00 0000
619h	CWG2DBF			—	—	DBF<5:0>						--00 0000	--00 0000
61Ah	CWG2CON0			EN	LD	—	—	—	MODE<2:0>			00-- -000	00-- -000
61Bh	CWG2CON1			—	—	IN	—	POLD	POLC	POLB	POLA	--x- 0000	--u- 0000
61Ch	CWG2AS0			SHUTDOWN	REN	LSBD<1:0>		LSAC<1:0>		—	—	0001 01--	0001 01--
61Dh	CWG2AS1			—	AS6E	AS5E	AS4E	AS3E	AS2E	AS1E	AS0E	-000 0000	-000 0000
61Eh	CWG2STR			OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	0000 0000	0000 0000
61Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18856	PIC16(L)F18876	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Banks 17													
CPU CORE REGISTERS; see Table 3-2 for specifics													
88Ch	CPUDOZE			IDLEN	DOZEN	ROI	DOE	—	DOZE2	DOZE1	DOZE0	0000 -000	0000 -000
88Dh	OSCCON1			—	NOSC<2:0>			NDIV<3:0>				-qqq 0000	-qqq 0000
88Eh	OSCCON2			—	COSC<2:0>			CDIV<3:0>				-qqq qqqq	-qqq qqqq
88Fh	OSCCON3			CSWHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—	00-0 0---	00-0 0---
890h	OSCSTAT			EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR	q0-0 qq-0	q0-0 qq-0
891h	OSCEN			EXTOEN	HFOEN	MFOEN	LFOEN	SOSCEN	ADOEN	—	—	00-0 00--	00-0 00--
892h	OSCTUNE			—	—	HFTUN<5:0>						--10 0000	--10 0000
893h	OSCFRQ			—	—	—	—	—	HFFRQ<2:0>			---- -qqq	---- -qqq
894h	—	—		Unimplemented								—	—
895h	CLKRCON			CLKREN	—	—	CLKRDC<1:0>		CLKRDIV<2:0>			0--1 0000	0--1 0000
896h	CLKRCLK			—	—	—	—	CLKRCLK<3:0>				---- 0000	---- 0000
897h	MDCON0			MDEN	—	MDOUT	MDOPOL	—	—	—	MDBIT	0-00 ---0	0-00 ---0
898h	MDCON1			—	—	MDCHPOL	MDCHSYNC	—	—	MDCLPOL	MDCLSYNC	--00 --00	--00 --00
899h	MDSRC			—	—	—	MDMS<4:0>					---0 0000	---0 0000
89Ah	MDCARL			—	—	—	—	MDCLS<3:0>				---- 0000	---- 0000
89Bh	MDCARH			—	—	—	—	MDCHS<3:0>				---- 0000	---- 0000
89Ch	—	—		Unimplemented								—	—
89Dh	—	—		Unimplemented								—	—
89Eh	—	—		Unimplemented								—	—
89Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

5.13 Register Definitions: Power Control

REGISTER 5-2: PCON0: POWER CONTROL REGISTER 0

R/W/HS-0/q	R/W/HS-0/q	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-q/u	R/W/HC-q/u
STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-m/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **STKOVF:** Stack Overflow Flag bit
1 = A Stack Overflow occurred
0 = A Stack Overflow has not occurred or cleared by firmware

bit 6 **STKUNF:** Stack Underflow Flag bit
1 = A Stack Underflow occurred
0 = A Stack Underflow has not occurred or cleared by firmware

bit 5 **$\overline{\text{WDTWV}}$:** WDT Window Violation Flag bit
1 = A WDT Window Violation Reset has not occurred or set by firmware
0 = A WDT Window Violation Reset has occurred (a CLRWDT instruction was executed either without arming the window or outside the window (cleared by hardware)

bit 4 **$\overline{\text{RWDT}}$:** Watchdog Timer Reset Flag bit
1 = A Watchdog Timer Reset has not occurred or set to '1' by firmware
0 = A Watchdog Timer Reset has occurred (cleared by hardware)

bit 3 **$\overline{\text{RMCLR}}$:** $\overline{\text{MCLR}}$ Reset Flag bit
1 = A $\overline{\text{MCLR}}$ Reset has not occurred or set to '1' by firmware
0 = A $\overline{\text{MCLR}}$ Reset has occurred (cleared by hardware)

bit 2 **$\overline{\text{RI}}$:** RESET Instruction Flag bit
1 = A RESET instruction has not been executed or set to '1' by firmware
0 = A RESET instruction has been executed (cleared by hardware)

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

TABLE 5-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	—	—	—	—	—	—	BORRDY	104
PCON0	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	109
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	38
WDTCON0	—	—	WDTPS<4:0>					SWDTEN	166

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

10.0 NONVOLATILE MEMORY (NVM) CONTROL

NVM is separated into two types: Program Flash Memory (PFM) and Data EEPROM Memory.

NVM is accessible by using both the FSR and INDF registers, or through the NVMREG register interface.

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the operating voltage range of the device.

NVM can be protected in two ways; by either code protection or write protection.

Code protection ($\overline{CP}$ and $\overline{CPD}$ bits in Configuration Word 5) disables access, reading and writing, to both the PFM and EEPROM via external device programmers. Code protection does not affect the self-write and erase functionality. Code protection can only be Reset by a device programmer performing a Bulk Erase to the device, clearing all nonvolatile memory, Configuration bits, and User IDs.

Write protection prohibits self-write and erase to a portion or all of the PFM, as defined by the WRT<1:0> bits of Configuration Word 4. Write protection does not affect a device programmer's ability to read, write, or erase the device.

10.1 Program Flash Memory (PFM)

PFM consists of an array of 14-bit words as user memory, with additional words for User ID information, Configuration words, and interrupt vectors. PFM provides storage locations for:

- User program instructions
- User defined data

PFM data can be read and/or written to through:

- CPU instruction fetch (read-only)
- FSR/INDF indirect access (read-only) (**Section 10.3 "FSR and INDF Access"**)
- NVMREG access (**Section 10.4 "NVMREG Access"**
- In-Circuit Serial Programming™ (ICSP™)

Read operations return a single word of memory. When write and erase operations are done on a row basis, the row size is defined in Table 10-1. PFM will erase to a logic '1' and program to a logic '0'.

TABLE 10-1: FLASH MEMORY ORGANIZATION BY DEVICE

Device	Row Erase (words)	Write Latches (words)	Total Program Flash (words)
PIC16(L)F18856	32	32	16384
PIC16(L)F18876			

It is important to understand the PFM memory structure for erase and programming operations. PFM is arranged in rows. A row consists of 32 14-bit program memory words. A row is the minimum size that can be erased by user software.

After a row has been erased, all or a portion of this row can be programmed. Data to be written into the program memory row is written to 14-bit wide data write latches. These latches are not directly accessible, but may be loaded via sequential writes to the NVMDATH:NVMDATL register pair.

Note:	To modify only a portion of a previously programmed row, then the contents of the entire row must be read and saved in RAM prior to the erase. Then, the new data and retained data can be written into the write latches to reprogram the row of PFM. However, any unprogrammed locations can be written without first erasing the row. In this case, it is not necessary to save and rewrite the other previously programmed locations

10.1.1 PROGRAM MEMORY VOLTAGES

The PFM is readable and writable during normal operation over the full VDD range.

10.1.1.1 Programming Externally

The program memory cell and control logic support write and Bulk Erase operations down to the minimum device operating voltage. Special BOR operation is enabled during Bulk Erase (**Section 5.2.4 "BOR is always OFF"**).

10.1.1.2 Self-programming

The program memory cell and control logic will support write and row erase operations across the entire VDD range. Bulk Erase is not supported when self-programming.

EXAMPLE 10-4: WRITING TO PROGRAM FLASH MEMORY (PFM)

```
; This write routine assumes the following:
; 1. 64 bytes of data are loaded, starting at the address in DATA_ADDR
; 2. Each word of data to be written is made up of two adjacent bytes in DATA_ADDR,
;    stored in little endian format
; 3. A valid starting address (the least significant bits = 00000) is loaded in ADDRH:ADDRL
; 4. ADDRH and ADDRL are located in common RAM (locations 0x70 - 0x7F)
; 5. NVM interrupts are not taken into account

        BANKSEL     NVMADRH
        MOVF        ADDRH,W
        MOVWF       NVMADRH             ; Load initial address
        MOVF        ADDRL,W
        MOVWF       NVMADRL
        MOVLW       LOW DATA_ADDR       ; Load initial data address
        MOVWF       FSR0L
        MOVLW       HIGH DATA_ADDR
        MOVWF       FSR0H
        BCF         NVMCON1,NVMREGS     ; Set Program Flash Memory as write location
        BSF         NVMCON1,WREN        ; Enable writes
        BSF         NVMCON1,LWLO        ; Load only write latches

LOOP
        MOVIW       FSR0++
        MOVWF       NVMDATL             ; Load first data byte
        MOVIW       FSR0++
        MOVWF       NVMDATH             ; Load second data byte

        MOVF        NVMADRL,W
        XORLW       0x1F                ; Check if lower bits of address are 00000
        ANDLW       0x1F                ; and if on last of 32 addresses
        BTFSC       STATUS,Z            ; Last of 32 words?
        GOTO        START_WRITE         ; If so, go write latches into memory

        CALL        UNLOCK_SEQ          ; If not, go load latch
        INCF        NVMADRL,F           ; Increment address
        GOTO        LOOP

START_WRITE
        BCF         NVMCON1,LWLO        ; Latch writes complete, now write memory
        CALL        UNLOCK_SEQ          ; Perform required unlock sequence
        BCF         NVMCON1,WREN        ; Disable writes

UNLOCK_SEQ
        MOVLW       55h
        BCF         INTCON,GIE          ; Disable interrupts
        MOVWF       NVMCON2             ; Begin unlock sequence
        MOVLW       AAh
        MOVWF       NVMCON2
        BSF         NVMCON1,WR
        BSF         INTCON,GIE          ; Unlock sequence complete, re-enable interrupts
        return
```

REGISTER 10-5: NVMCON1: NONVOLATILE MEMORY CONTROL 1 REGISTER

U-0	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W/HC-x/q	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
—	NVMREGS	LWLO	FREE	WRERR(1,2,3)	WREN	WR(4,5,6)	RD(7)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **Unimplemented:** Read as '0'

bit 6 **NVMREGS:** Configuration Select bit
1 = Access EEPROM, Configuration, User ID and Device ID Registers
0 = Access PFM

bit 5 **LWLO:** Load Write Latches Only bit
When FREE = 0:
1 = The next WR command updates the write latch for this word within the row; no memory operation is initiated.
0 = The next WR command writes data or erases
Otherwise: The bit is ignored

bit 4 **FREE:** PFM Erase Enable bit
When NVMREGS:NVMADR points to a PFM location:
1 = Performs an erase operation with the next WR command; the 32-word pseudo-row containing the indicated address is erased (to all 1s) to prepare for writing.
0 = All write operations have completed normally

bit 3 **WRERR:** Program/Erase Error Flag bit(1,2,3)
This bit is normally set by hardware.
1 = A write operation was interrupted by a Reset, interrupted unlock sequence, or WR was written to one while NVMADR points to a write-protected address.
0 = The program or erase operation completed normally

bit 2 **WREN:** Program/Erase Enable bit
1 = Allows program/erase cycles
0 = Inhibits programming/erasing of program Flash

bit 1 **WR:** Write Control bit(4,5,6)
When NVMREG:NVMADR points to a EEPROM location:
1 = Initiates an erase/program cycle at the corresponding EEPROM location
0 = NVM program/erase operation is complete and inactive
When NVMREG:NVMADR points to a PFM location:
1 = Initiates the operation indicated by Table 10-4
0 = NVM program/erase operation is complete and inactive
Otherwise: This bit is ignored

bit 0 **RD:** Read Control bit(7)
1 = Initiates a read at address = NVMADR1, and loads data to NVMDAT Read takes one instruction cycle and the bit is cleared when the operation is complete. The bit can only be set (not cleared) in software.
0 = NVM read operation is complete and inactive

Note 1: Bit is undefined while WR = 1 (during the EEPROM write operation it may be '0' or '1').
2: Bit must be cleared by software; hardware will not clear this bit.
3: Bit may be written to '1' by software in order to implement test sequences.
4: This bit can only be set by following the unlock sequence of **Section 10.4.2 "NVM Unlock Sequence"**.
5: Operations are self-timed, and the WR bit is cleared by hardware when complete.
6: Once a write operation is initiated, setting this bit to zero will have no effect.
7: Reading from EEPROM loads only NVMDATL<7:0> (Register 10-1).

22.2 CLCx Interrupts

An interrupt will be generated upon a change in the output value of the CLCx when the appropriate interrupt enables are set. A rising edge detector and a falling edge detector are present in each CLC for this purpose.

The CLCxIF bit of the associated PIR5 register will be set when either edge detector is triggered and its associated enable bit is set. The LCxINTP enables rising edge interrupts and the LCxINTN bit enables falling edge interrupts. Both are located in the CLCxCON register.

To fully enable the interrupt, set the following bits:

- CLCxIE bit of the PIE5 register
- LCxINTP bit of the CLCxCON register (for a rising edge detection)
- LCxINTN bit of the CLCxCON register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The CLCxIF bit of the PIR5 register, must be cleared in software as part of the interrupt service. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

22.3 Output Mirror Copies

Mirror copies of all LCxCON output bits are contained in the CLCxDATA register. Reading this register reads the outputs of all CLCs simultaneously. This prevents any reading skew introduced by testing or reading the LCxOUT bits in the individual CLCxCON registers.

22.4 Effects of a Reset

The CLCxCON register is cleared to zero as the result of a Reset. All other selection and gating values remain unchanged.

22.5 Operation During Sleep

The CLC module operates independently from the system clock and will continue to run during Sleep, provided that the input sources selected remain active.

The HFINTOSC remains active during Sleep when the CLC module is enabled and the HFINTOSC is selected as an input source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and as a CLC input source, when the CLC is enabled, the CPU will go idle during Sleep, but the CLC will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

22.6 CLCx Setup Steps

The following steps should be followed when setting up the CLCx:

- Disable CLCx by clearing the LCxEN bit.
- Select desired inputs using CLCxSEL0 through CLCxSEL3 registers (See Table 22-2).
- Clear any associated ANSEL bits.
- Set all TRIS bits associated with inputs.
- Clear all TRIS bits associated with outputs.
- Enable the chosen inputs through the four gates using CLCxGLS0, CLCxGLS1, CLCxGLS2, and CLCxGLS3 registers.
- Select the gate output polarities with the LCxGyPOL bits of the CLCxPOL register.
- Select the desired logic function with the LCxMODE<2:0> bits of the CLCxCON register.
- Select the desired polarity of the logic output with the LCxPOL bit of the CLCxPOL register. (This step may be combined with the previous gate output polarity step).
- If driving a device pin, set the desired pin PPS control register and also clear the TRIS bit corresponding to that output.
- If interrupts are desired, configure the following bits:
  - Set the LCxINTP bit in the CLCxCON register for rising event.
  - Set the LCxINTN bit in the CLCxCON register for falling event.
  - Set the CLCxIE bit of the PIE5 register.
  - Set the GIE and PEIE bits of the INTCON register.
- Enable the CLCx by setting the LCxEN bit of the CLCxCON register.

REGISTER 23-21: ADPREVL: ADC PREVIOUS RESULT REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADPREV<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ADPREV<7:0>**: Previous ADC Results Least Significant Byte
If ADPSIS = 1:
Least Significant Byte of ADFLTR at the start of current ADC conversion
If ADPSIS = 0:
Least Significant bits of ADRES at the start of current ADC conversion(1)

Note 1: If ADPSIS = 0, ADPREVH and ADPREVL are formatted the same way as ADRES is, depending on the ADFRM bit.

REGISTER 23-22: ADACCH: ADC ACCUMULATOR REGISTER HIGH

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADACC<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ADACC<15:8>**: ADC Accumulator MSB. Most Significant seven bits of accumulator value and sign bit.

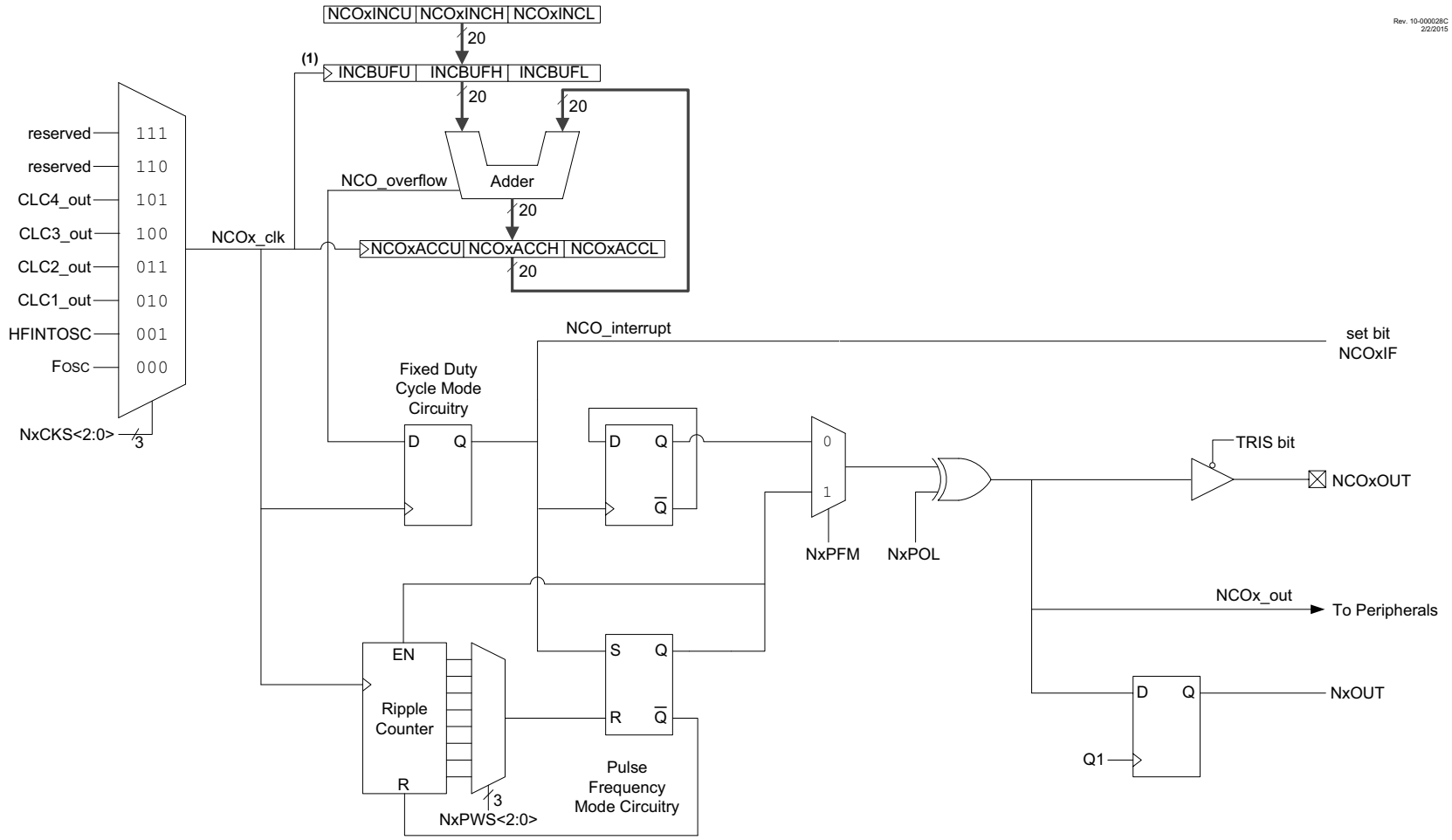
REGISTER 23-23: ADACCL: ADC ACCUMULATOR REGISTER LOW

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADACC<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ADACC<7:0>**: ADC Accumulator LSB. Least Significant eight bits of accumulator value.

FIGURE 24-1: DIRECT DIGITAL SYNTHESIS MODULE SIMPLIFIED BLOCK DIAGRAM



Note 1: The increment registers are double-buffered to allow for value changes to be made without first disabling the NCO module. The full increment value is loaded into the buffer registers on the second rising edge of the NCOx_clk signal that occurs immediately after a write to NCOxINCL register. The buffers are not user-accessible and are shown here for reference.

FIGURE 24-2: FDC OUTPUT MODE OPERATION DIAGRAM

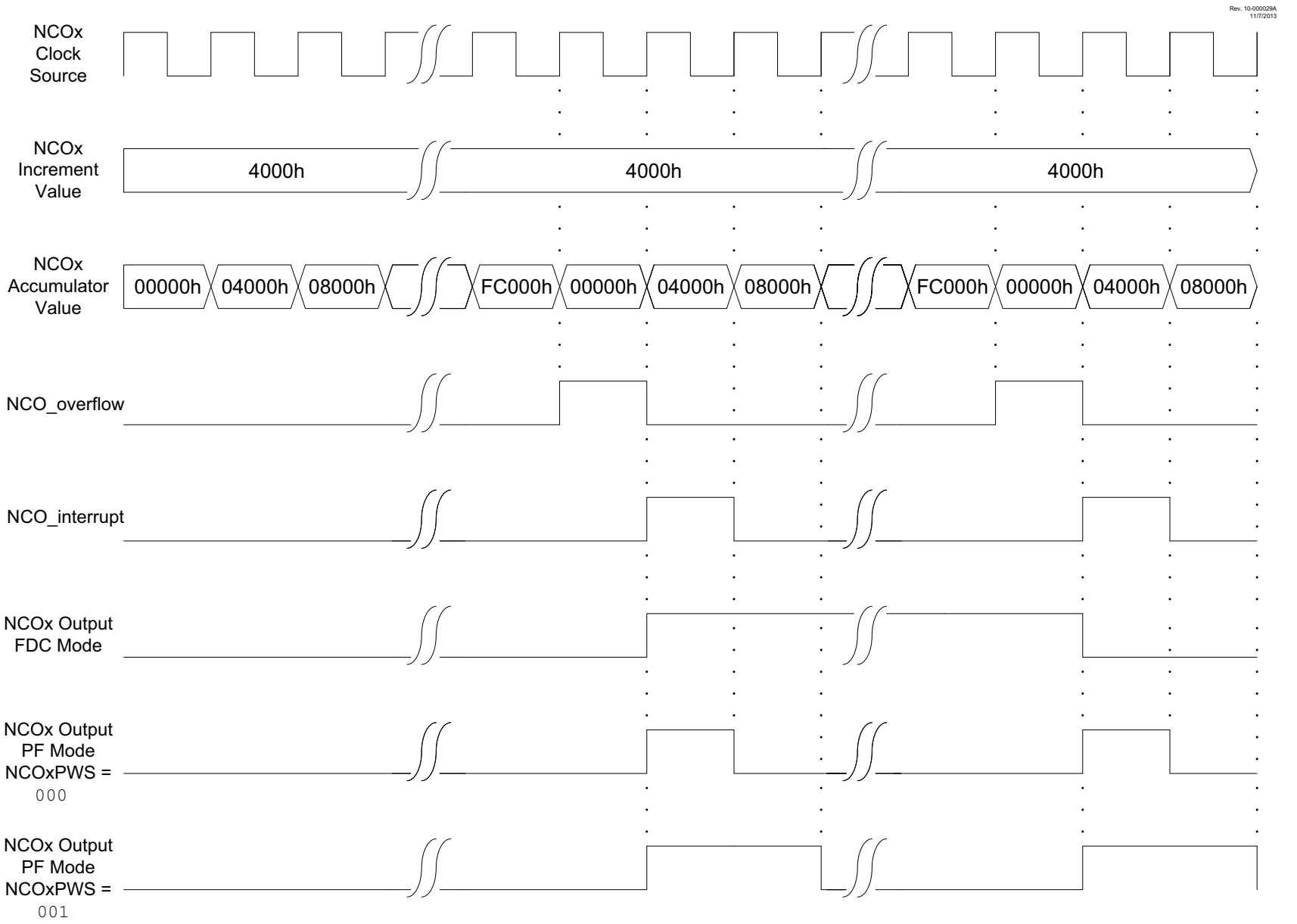
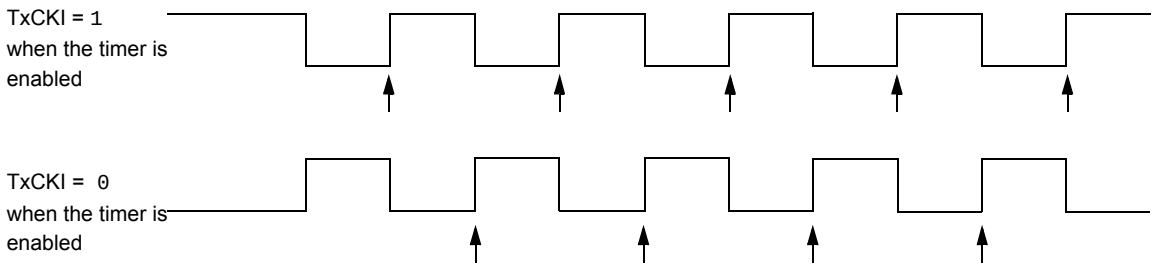


FIGURE 28-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

FIGURE 28-3: TIMER1 GATE ENABLE MODE

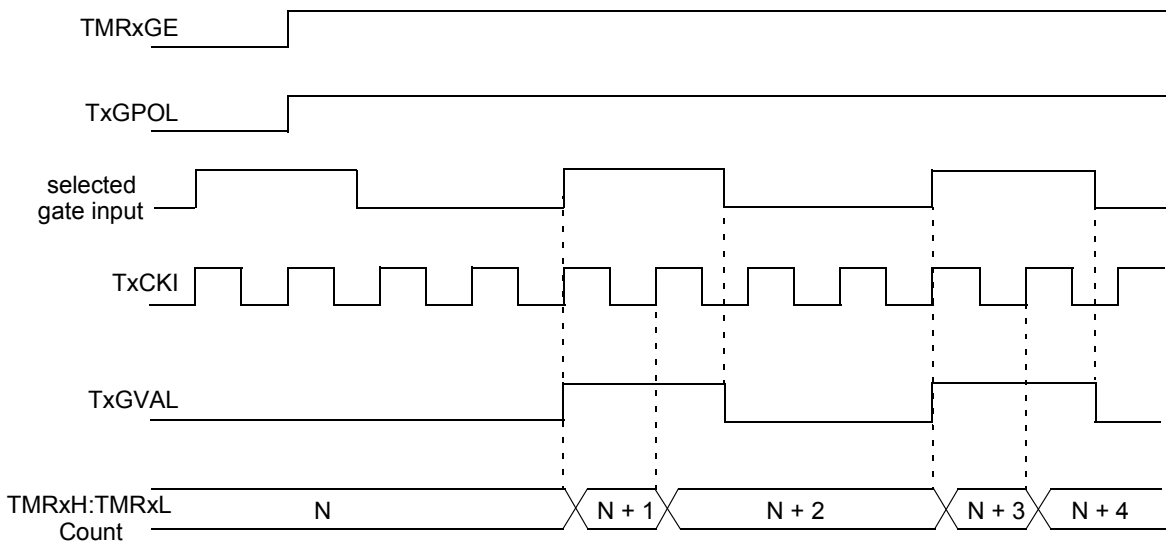


TABLE 29-1: TIMER2 OPERATING MODES

Mode	MODE<4:0>		Output Operation	Operation	Timer Control		
	<4:3>	<2:0>			Start	Reset	Stop
Free Running Period	00	000	Period Pulse	Software gate (Figure 29-4)	ON = 1	—	ON = 0
		001		Hardware gate, active-high (Figure 29-5)	ON = 1 and TMRx_ers = 1	—	ON = 0 or TMRx_ers = 0
		010		Hardware gate, active-low	ON = 1 and TMRx_ers = 0	—	ON = 0 or TMRx_ers = 1
		011	Period Pulse with Hardware Reset	Rising or falling edge Reset	ON = 1	TMRx_ers ↕	ON = 0
		100		Rising edge Reset (Figure 29-6)		TMRx_ers ↑	
		101		Falling edge Reset		TMRx_ers ↓	
		110		Low level Reset		TMRx_ers = 0	ON = 0 or TMRx_ers = 0
		111		High level Reset (Figure 29-7)		TMRx_ers = 1	ON = 0 or TMRx_ers = 1
One-shot	01	000	One-shot	Software start (Figure 29-8)	ON = 1	—	ON = 0 or Next clock after TMRx = PRx (**Note 2**)
		001	Edge triggered start (**Note 1**)	Rising edge start (Figure 29-9)	ON = 1 and TMRx_ers ↑	—	
		010		Falling edge start	ON = 1 and TMRx_ers ↓	—	
		011		Any edge start	ON = 1 and TMRx_ers ↕	—	
		100	Edge triggered start and hardware Reset (**Note 1**)	Rising edge start and Rising edge Reset (Figure 29-10)	ON = 1 and TMRx_ers ↑	TMRx_ers ↑	
		101		Falling edge start and Falling edge Reset	ON = 1 and TMRx_ers ↓	TMRx_ers ↓	
		110		Rising edge start and Low level Reset (Figure 29-11)	ON = 1 and TMRx_ers ↑	TMRx_ers = 0	
		111		Falling edge start and High level Reset	ON = 1 and TMRx_ers ↓	TMRx_ers = 1	
Mono-stable	10	000	Reserved				
		001	Edge triggered start (**Note 1**)	Rising edge start (Figure 29-12)	ON = 1 and TMRx_ers ↑	—	ON = 0 or Next clock after TMRx = PRx (**Note 3**)
		010		Falling edge start	ON = 1 and TMRx_ers ↓	—	
		011		Any edge start	ON = 1 and TMRx_ers ↕	—	
Reserved		100	Reserved				
Reserved		101	Reserved				
One-shot		110	Level triggered start and hardware Reset	High level start and Low level Reset (Figure 29-13)	ON = 1 and TMRx_ers = 1	TMRx_ers = 0	ON = 0 or Held in Reset (**Note 2**)
		111		Low level start & High level Reset	ON = 1 and TMRx_ers = 0	TMRx_ers = 1	
Reserved	11	xxx	Reserved				

Note 1: If ON = 0 then an edge is required to restart the timer after ON = 1.

2: When TMRx = PRx then the next clock clears ON and stops TMRx at 00h.

3: When TMRx = PRx then the next clock stops TMRx at 00h but does not clear ON.

29.5.8 LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

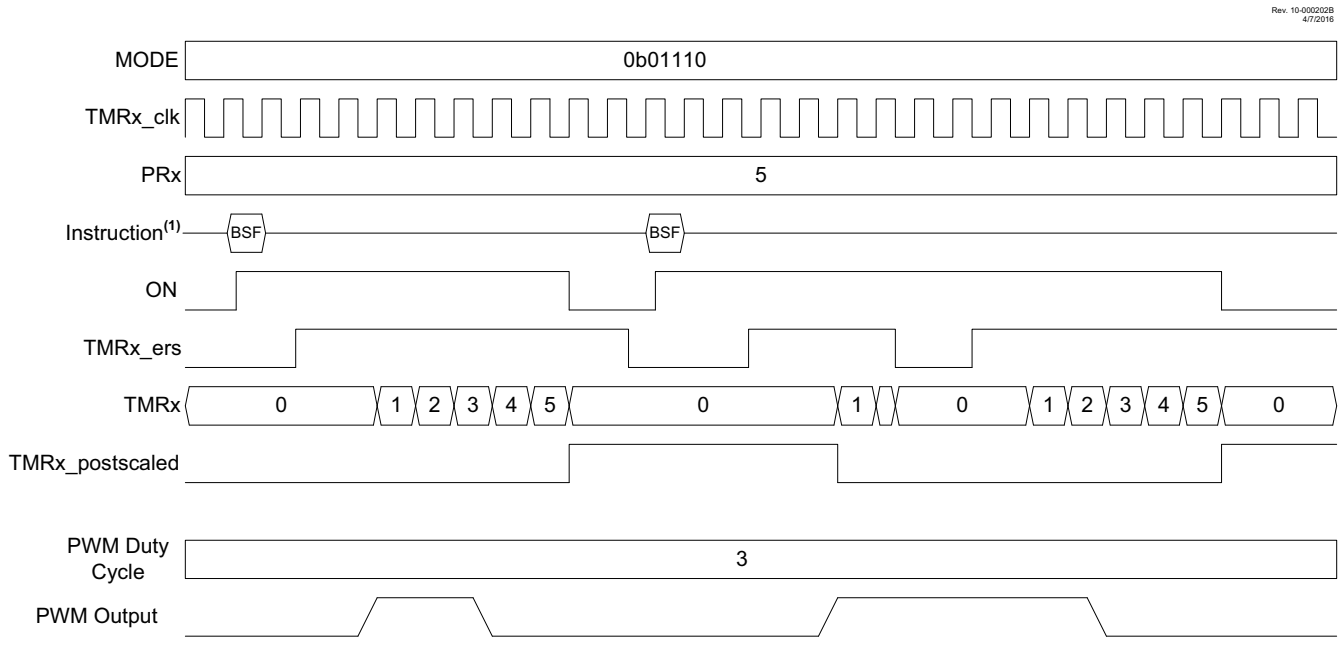
In Level -Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from Reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low Reset level (MODE<4:0> = `01110`)
- High Reset level (MODE<4:0> = `01111`)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control a new external signal edge is required after the ON bit is set to start the counter.

When Level-Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse width count. The PWM drive does not go active when the timer count clears at the PRx period count match.

FIGURE 29-11: LOW LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = `01110`)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

31.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level (Case 1).
b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1' (Case 2).

When the user releases SDA and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 31-36). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 31-37.

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 31-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

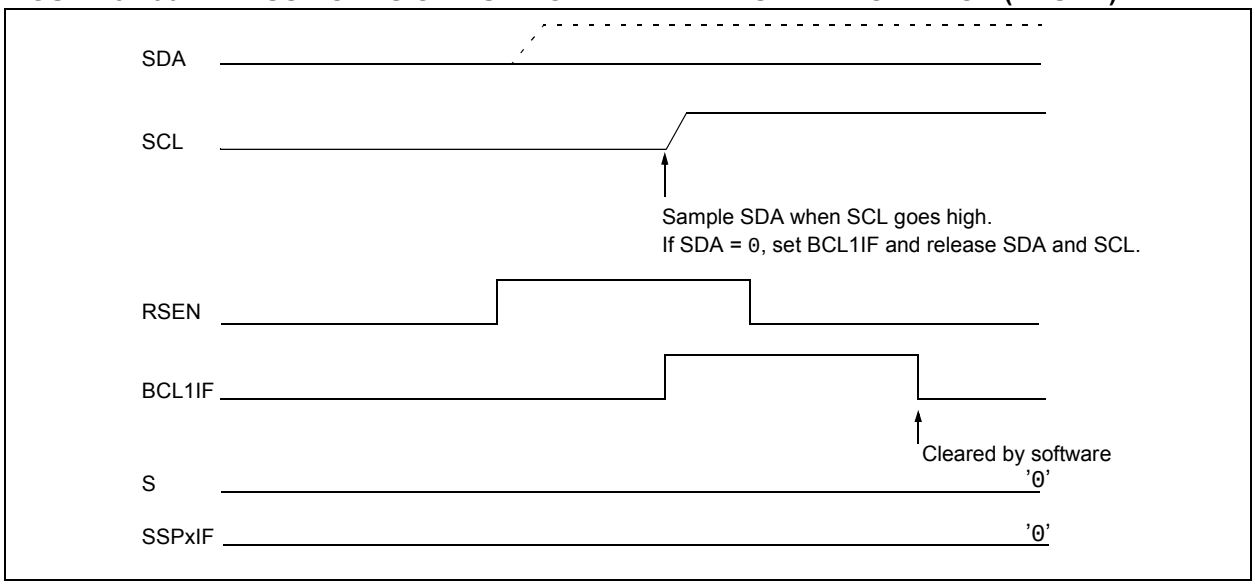


FIGURE 31-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)

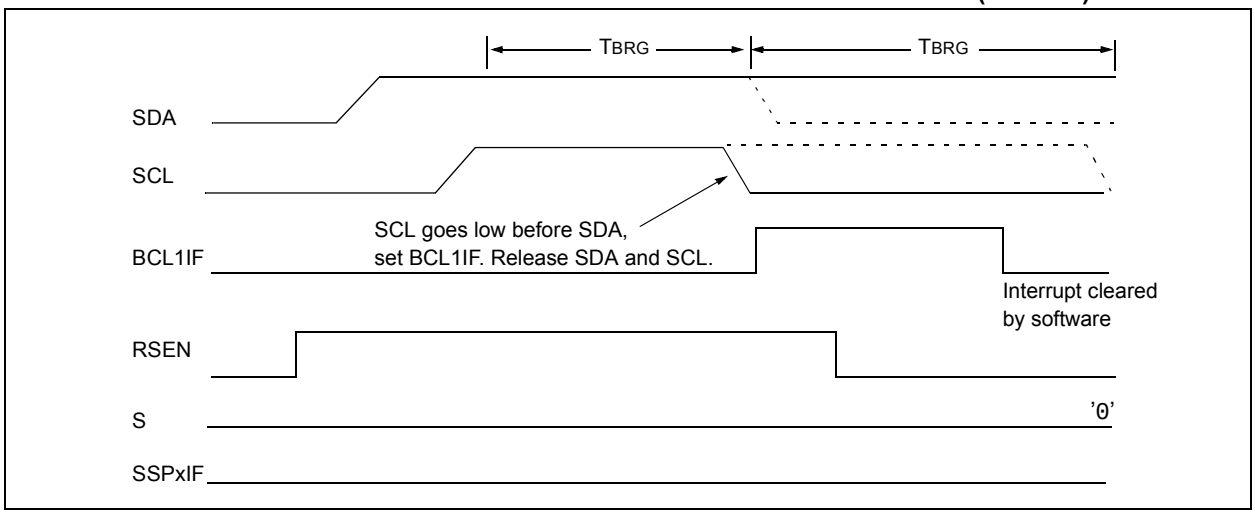
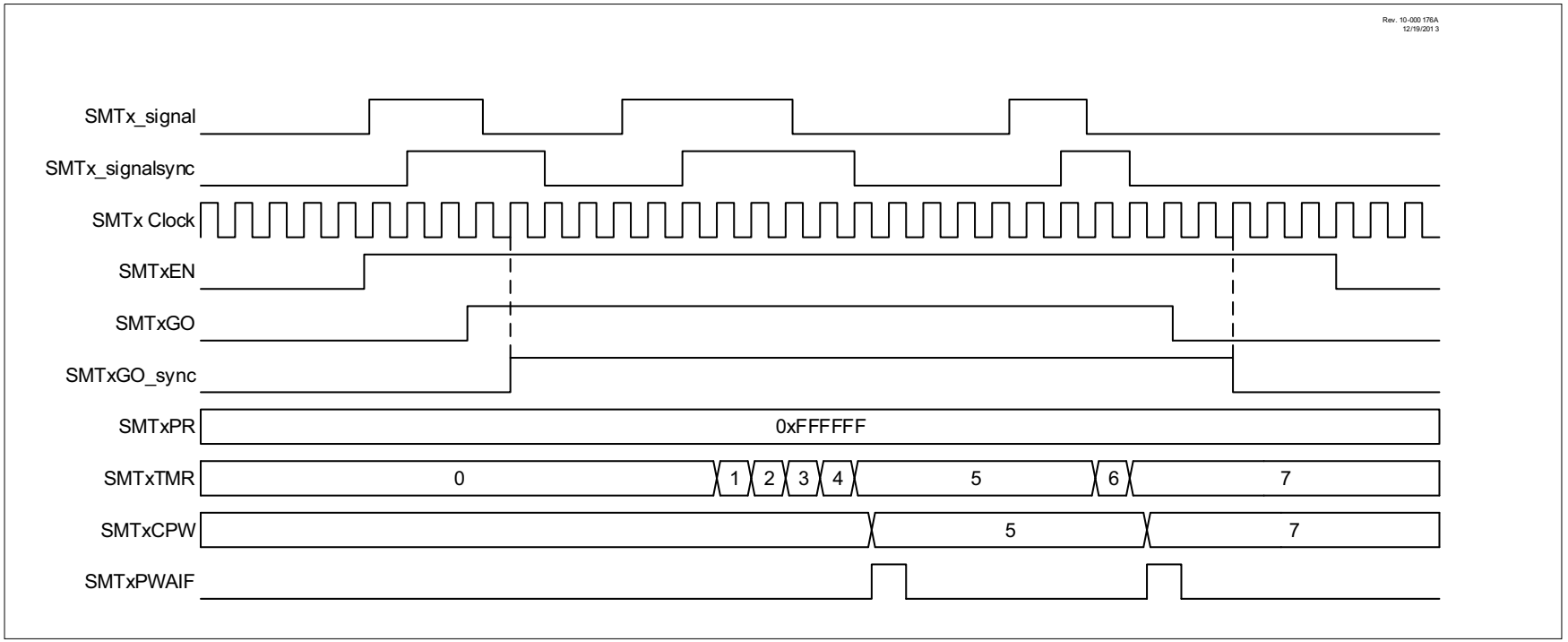


FIGURE 32-4: GATED TIMER MODE REPEAT ACQUISITION TIMING DIAGRAM



Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

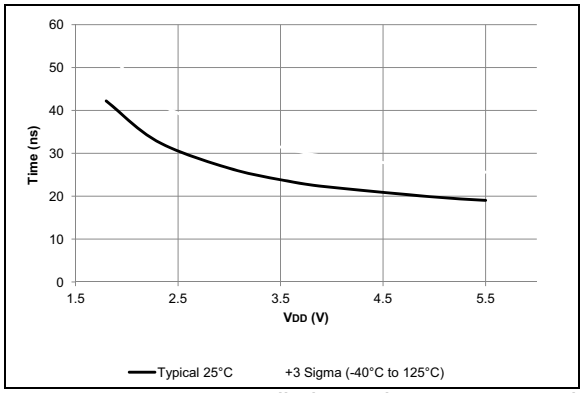


FIGURE 38-85: *Fall Time, Slew Rate Control Enabled.*

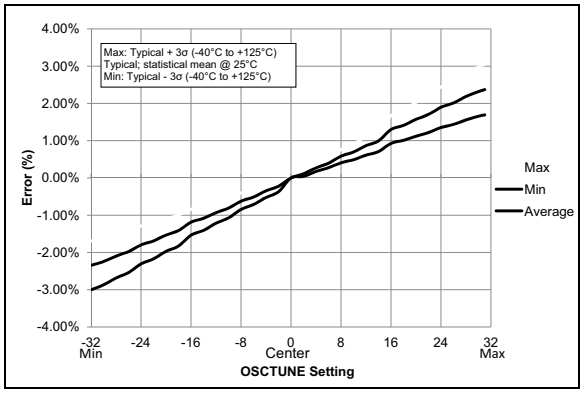


FIGURE 38-88: *OSCTUNE Center Frequency, PIC16LF18856/76 Only.*

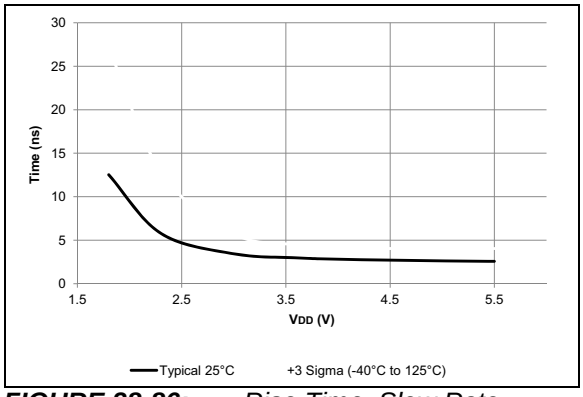


FIGURE 38-86: *Rise Time, Slew Rate Control Disabled.*

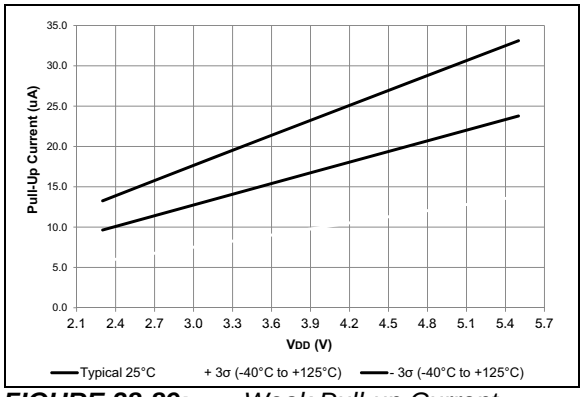


FIGURE 38-89: *Weak Pull-up Current, PIC16F18856/76 Only.*

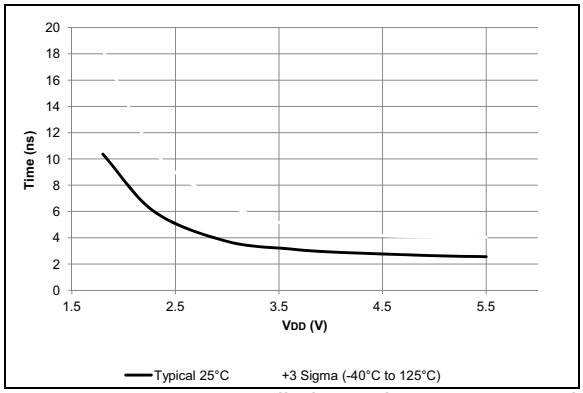


FIGURE 38-87: *Fall Time, Slew Rate Control Disabled.*

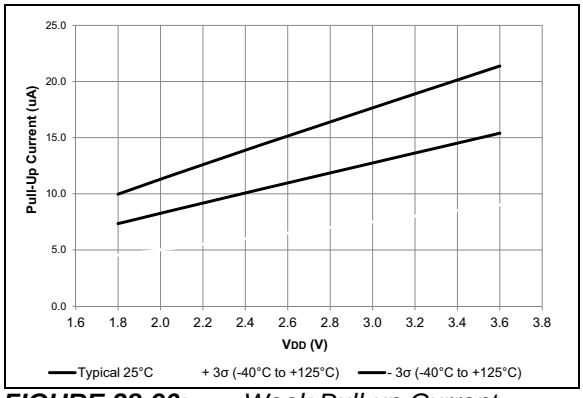
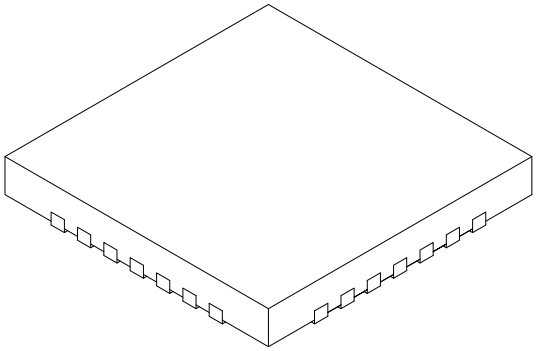


FIGURE 38-90: *Weak Pull-up Current, PIC16LF18856/76 Only.*

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.55	2.65	2.75
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.55	2.65	2.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-152A Sheet 2 of 2