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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18856-i-ss

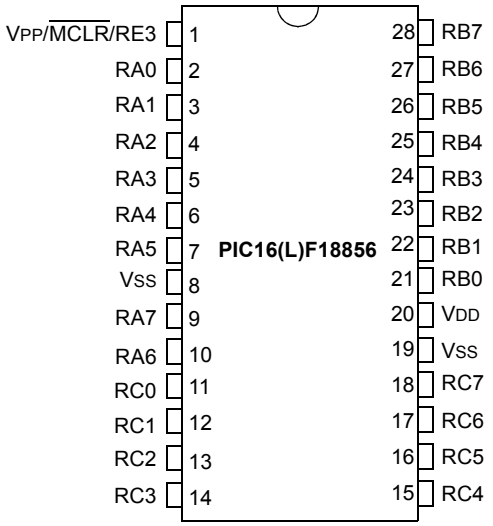
TABLE 1: PACKAGES

Packages	(S)PDIP	SOIC	SSOP	QFN (6x6)	UQFN (4x4)	TQFP	QFN (8x8)	UQFN (5x5)
PIC16(L)F18856	●	●	●	●	●			
PIC16(L)F18876	●					●	●	●

Note: Pin details are subject to change.

PIN DIAGRAMS

28-pin SPDIP, SOIC, SSOP



Note 1: See Table 2 for location of all peripheral functions.

2: All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

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Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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TABLE 3-8: PIC16(L)F18856/76 MEMORY MAP, BANK 28

Bank 28	
E0Ch	—
E0Dh	—
E0Eh	—
E0Fh	CLCDATA
E10h	CLC1CON
E11h	CLC1POL
E12h	CLC1SEL0
E13h	CLC1SEL1
E14h	CLC1SEL2
E15h	CLC1SEL3
E16h	CLC1GLS0
E17h	CLC1GLS1
E18h	CLC1GLS2
E19h	CLC1GLS3
E1Ah	CLC2CON
E1Bh	CLC2POL
E1Ch	CLC2SEL0
E1Dh	CLC2SEL1
E1Eh	CLC2SEL2
E1Fh	CLC2SEL3
E20h	CLC2GLS0
E21h	CLC2GLS1
E22h	CLC2GLS2
E23h	CLC2GLS3
E24h	CLC3CON
E25h	CLC3POL
E26h	CLC3SEL0
E27h	CLC3SEL1
E28h	CLC3SEL2
E29h	CLC3SEL3
E2Ah	CLC3GLS0
E2Bh	CLC3GLS1
E2Ch	CLC3GLS2
E2Dh	CLC3GLS3

Bank 28	
E2Eh	CLC4CON
E2Fh	CLC4POL
E30h	CLC4SEL0
E31h	CLC4SEL1
E32h	CLC4SEL2
E33h	CLC4SEL3
E34h	CLC4GLS0
E35h	CLC4GLS1
E36h	CLC4GLS2
E37h	CLC4GLS3
E38h — E6Fh	—

Legend: = Unimplemented data memory locations, read as ‘0’.

TABLE 3-9: PIC16(L)F18856/76 MEMORY MAP, BANK 29

	Bank 29
E8Ch	—
E8Dh	—
E8Eh	—
E8Fh	PPSLOCK
E90h	INTPPS
E91h	T0CKIPPS
E92h	T1CKIPPS
E93h	T1GPPS
E94h	T3CKIPPS
E95h	T3GPPS
E96h	T5CKIPPS
E97h	T5GPPS
E98h	—
E99h	—
E9Ah	—
E9Bh	—
E9Ch	T2AINPPS
E9Dh	T4AINPPS
E9Eh	T6AINPPS
E9Fh	—
EA0h	—
EA1h	CCP1PPS
EA2h	CCP2PPS
EA3h	CCP3PPS
EA4h	CCP4PPS
EA5h	CCP5PPS
EA6h	—
EA7h	—
EA8h	—
EA9h	SMT1WINPPS
EAAh	SMT1SIGPPS
EABh	SMT2WINPPS
EACh	SMT2SIGPPS
EADh	—
EAEh	—
EAFh	—
EB0h	—

	Bank 29
EB1h	CWG1PPS
EB2h	CWG2PPS
EB3h	CWG3PPS
EB4h	—
EB5h	—
EB6h	—
EB7h	—
EB8h	MDCARLPPS
EB9h	MDCARHPPS
EBAh	MDSRCPPS
EBBh	CLCIN0PPS
EBCh	CLCIN1PPS
EBDh	CLCIN2PPS
EBEh	CLCIN3PPS
EBFh	—
EC0h	—
EC1h	—
EC2h	—
EC3h	ADCACTPPS
EC4h	—
EC5h	SSP1CLKPPS
EC6h	SSP1DATPPS
EC7h	SSP1SSPPS
EC8h	SSP2CLKPPS
EC9h	SSP2DATPPS
ECAh	SSP2SSPPS
ECBh	RXPPS
ECCh	TXPPS
ECDh – EEFh	—

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18856	PIC16(L)F18876	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Banks 16													
CPU CORE REGISTERS; see Table 3-2 for specifics													
80Ch	WDTCON0			—	—	PS<4:0>					SEN	--qq qqq0	--qq qqq0
80Dh	WDTCON1			—	WDTCS<2:0>			—	WINDOW<2:0>			-qqq -qqq	-qqq -qqq
80Eh	WDTPSL			PSCNT<7:0>								0000 0000	0000 0000
80Fh	WDTPSH			PSCNT<7:0>								0000 0000	0000 0000
810h	WDTTMR			—	WDTTMR<3:0>				STATE	PSCNT<17:16>		-000 0000	-000 0000
811h	BORCON			SBOREN	—	—	—	—	—	—	BORRDY	1--- ---q	u--- ---u
812h	VREGCON(1)			—	—	—	—	—	—	VREGPM	Reserved	---- --01	---- --01
813h	PCON0			STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	0011 11qq	qqqq qquu
814h	CCDCON			CCDEN	—	—	—	—	—	CCDS<1:0>		0--- --xx	0--- --uu
815h	—	—		Unimplemented								—	—
816h	—	—		Unimplemented								—	—
817h	—	—		Unimplemented								—	—
818h	—	—		Unimplemented								—	—
819h	—	—		Unimplemented								—	—
81Ah	NVMADRL			NVMADR<7:0>								0000 0000	0000 0000
81Bh	NVMADRH			—(2)	NVMADR<14:8>							1000 0000	1000 0000
81Ch	NVMDATL			NVMDAT<7:0>								0000 0000	0000 0000
81Dh	NVMDATH			—	—	NVMDAT<13:8>						--00 0000	--00 0000
81Eh	NVMCON1			—	NVMREGS	LWLO	FREE	WRERR	WREN	WR	RD	-000 x000	-000 q000
81Fh	NVMCON2			NVMCON2<7:0>								0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

REGISTER 7-20: PIR8: PERIPHERAL INTERRUPT REQUEST REGISTER 8

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	SMT2PWAIF	SMT2PRAIF	SMT2IF	SMT1PWAIF	SMT1PRAIF	SMT1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7-6 **Unimplemented:** Read as '0'.

bit 5 **SMT2PWAIF:** SMT2 Pulse Width Acquisition Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **SMT2PRAIF:** SMT2 Period Acquisition Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **SMT2IF:** SMT2 Overflow Interrupt Flag bit
1 = An SMT overflow event has occurred (must be cleared in software)
0 = No overflow event detected

bit 2 **SMT1PWAIF:** SMT1 Pulse Width Acquisition Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **SMT1PRAIF:** SMT1 Period Acquisition Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **SMT1IF:** SMT1 Overflow Interrupt Flag bit
1 = An SMT overflow event has occurred (must be cleared in software)
0 = No overflow event detected

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 12-8: SLRCONA: PORTA SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRA7	SLRA6	SLRA5	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SLRA<7:0>:** PORTA Slew Rate Enable bits
For RA<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 12-9: INLVLA: PORTA INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **INLVLA<7:0>:** PORTA Input Level Select bits
For RA<7:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

12.14.8 CURRENT-CONTROLLED DRIVE MODE CONTROL

The CCDPE and CCDNE registers (Register 12-53 and Register 12-54) control the Current-Controlled Drive mode for both the positive-going and negative-going drivers. When a CCDPE[y] or CCDNE[y] bit is set and the CCDEN bit of the CCDCON register is set, the Current-Controlled mode is enabled for the corresponding port pin. When the CCDPE[y] or CCDNE[y] bit is clear, the Current-Controlled mode for the corresponding port pin is disabled. If the CCDPE[y] or CCDNE[y] bit is set and the CCDEN bit is clear, operation of the port pin is undefined (see **Section 12.1.1 "Current-Controlled Drive"** for current-controlled use precautions).

12.14.9 PORTE FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic. See **Section 13.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

12.14.10 PORTE FUNCTIONS AND OUTPUT PRIORITIES

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Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

REGISTER 12-47: LATE: PORTE DATA LATCH REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	—	LATE2	LATE1	LATE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **LATE<2:0>**: PORTE Output Latch Value bits(1)

Note 1: Writes to PORTE are actually written to the corresponding LATE register. Reads from the PORTE register is return of actual I/O pin values.

REGISTER 12-48: ANSELE: PORTE ANALOG SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	—	—	ANSE2	ANSE1	ANSE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **ANSE<2:0>**: Analog Select between Analog or Digital Function on pins RE<2:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 13-2: RxyPPS: PIN Rxy OUTPUT SOURCE SELECTION REGISTER

U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	RxyPPS<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RxyPPS<5:0>:** Pin Rxy Output Source Selection bits
See Table 13-2.

Note 1: TRIS control is overridden by the peripheral as required.

REGISTER 13-3: PPSLOCK: PPS LOCK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0
—	—	—	—	—	—	—	PPSLOCKED
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-1 **Unimplemented:** Read as ‘0’

bit 0 **PPSLOCKED:** PPS Locked bit
1= PPS is locked. PPS selections can not be changed.
0= PPS is not locked. PPS selections can be changed.

REGISTER 20-8: CWGxCLK: CWGx CLOCK SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0
—	—	—	—	—	—	—	CS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **CS:** CWGx Clock Selection bit
1 = HFINTOSC 16 MHz is selected
0 = FOSC is selected

REGISTER 20-9: CWGxISM: CWGx INPUT SELECTION REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	IS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **IS<3:0>:** CWGx Input Selection bits
1111 = LC4_out
1110 = LC3_out
1101 = LC2_out
1100 = LC1_out
1011 = DSM_out
1010 = C2OUT_sync
1001 = C1OUT_sync
1000 = NCO1_out
0111 = PWM7_out
0110 = PWM6_out
0101 = CCP5_out
0100 = CCP4_out
0011 = CCP3_out
0010 = CCP2_out
0001 = CCP1_out
0000 = CWGxINPPS

NOTES:

26.5 Carrier Source Polarity Select

The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high source is enabled by setting the MDCHPOL bit of the MDCON1 register. Inverting the signal for the carrier low source is enabled by setting the MDCLPOL bit of the MDCON1 register.

26.6 Programmable Modulator Data

The MDBIT of the MDCON0 register can be selected as the source for the modulator signal. This gives the user the ability to program the value used for modulation.

26.7 Modulated Output Polarity

The modulated output signal provided on the DSM pin can also be inverted. Inverting the modulated output signal is enabled by setting the MDOPOL bit of the MDCON0 register.

26.8 Slew Rate Control

The slew rate limitation on the output port pin can be disabled. The slew rate limitation can be removed by clearing the SLR bit of the SLRCON register associated with that pin. For example, clearing the slew rate limitation for pin RA5 would require clearing the SLRA5 bit of the SLRCONA register.

26.9 Operation in Sleep Mode

The DSM module is not affected by Sleep mode. The DSM can still operate during Sleep, if the Carrier and Modulator input sources are also still operable during Sleep.

26.10 Effects of a Reset

Upon any device Reset, the DSM module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

REGISTER 30-6: CCPTMRS1: CCP TIMERS CONTROL 1 REGISTER

U-0	U-0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1
—	—	P7TSEL<1:0>		P6TSEL<1:0>		C5TSEL<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
'1' = Bit is set	'0' = Bit is cleared	

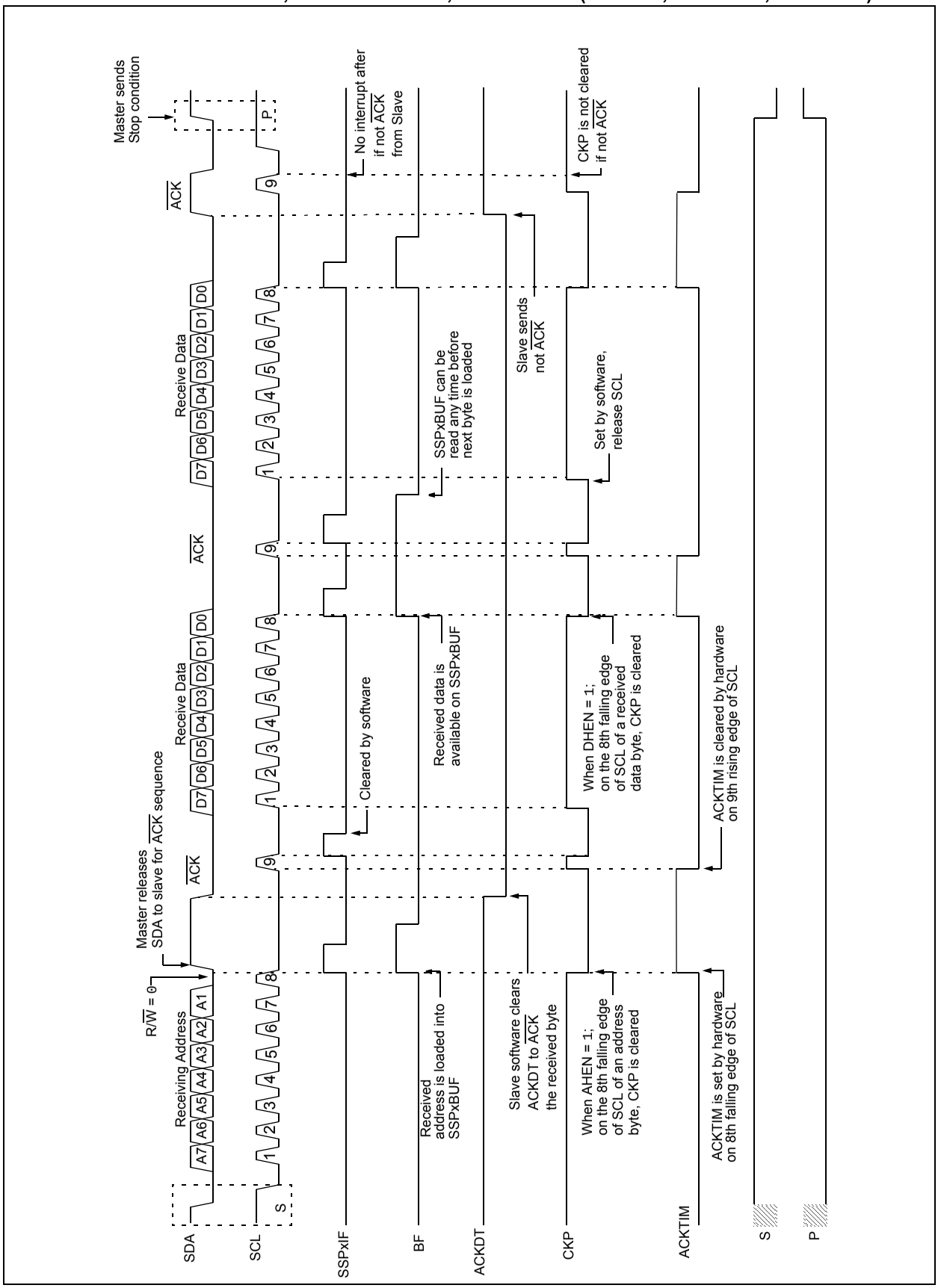
bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **P7TSEL<1:0>:** PWM7 Timer Selection
11 = PWM7 based on TMR6
10 = PWM7 based on TMR4
01 = PWM7 based on TMR2
00 = Reserved

bit 3-2 **P6TSEL<1:0>:** PWM6 Timer Selection
11 = PWM6 based on TMR6
10 = PWM6 based on TMR4
01 = PWM6 based on TMR2
00 = Reserved

bit 1-0 **C5TSEL<1:0>:** CCP5 Timer Selection
11 = CCP5 based on TMR5 (Capture/Compare) or TMR6 (PWM)
10 = CCP5 based on TMR3 (Capture/Compare) or TMR4 (PWM)
01 = CCP5 based on TMR1 (Capture/Compare) or TMR2 (PWM)
00 = Reserved

FIGURE 31-17: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 1, DHEN = 1)



REGISTER 31-4: SSPxCON3: SSPx CONTROL REGISTER 3

R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACKTIM(3)	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ACKTIM:** Acknowledge Time Status bit (I^2C mode only)(3)
1 = Indicates the I^2C bus is in an Acknowledge sequence, set on 8th falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9TH rising edge of SCL clock

bit 6 **PCIE**: Stop Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enable interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled(2)

bit 5 **SCIE**: Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enable interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled(2)

bit 4 **BOEN:** Buffer Overwrite Enable bit
In SPI Slave mode:(1)
1 = SSPxBUF updates every time that a new data byte is shifted in ignoring the BF bit
0 = If new byte is received with BF bit of the SSPxSTAT register already set, SSPOV bit of the SSPxCON1 register is set, and the buffer is not updated
In I^2C™ Master mode and SPI Master mode:
This bit is ignored.
In I^2C™ Slave mode:
1 = SSPxBUF is updated and $\overline{ACK}$ is generated for a received address/data byte, ignoring the state of the SSPOV bit only if the BF bit = 0.
0 = SSPxBUF is only updated when SSPOV is clear

bit 3 **SDAHT:** SDA Hold Time Selection bit (I^2C mode only)
1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL
0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL

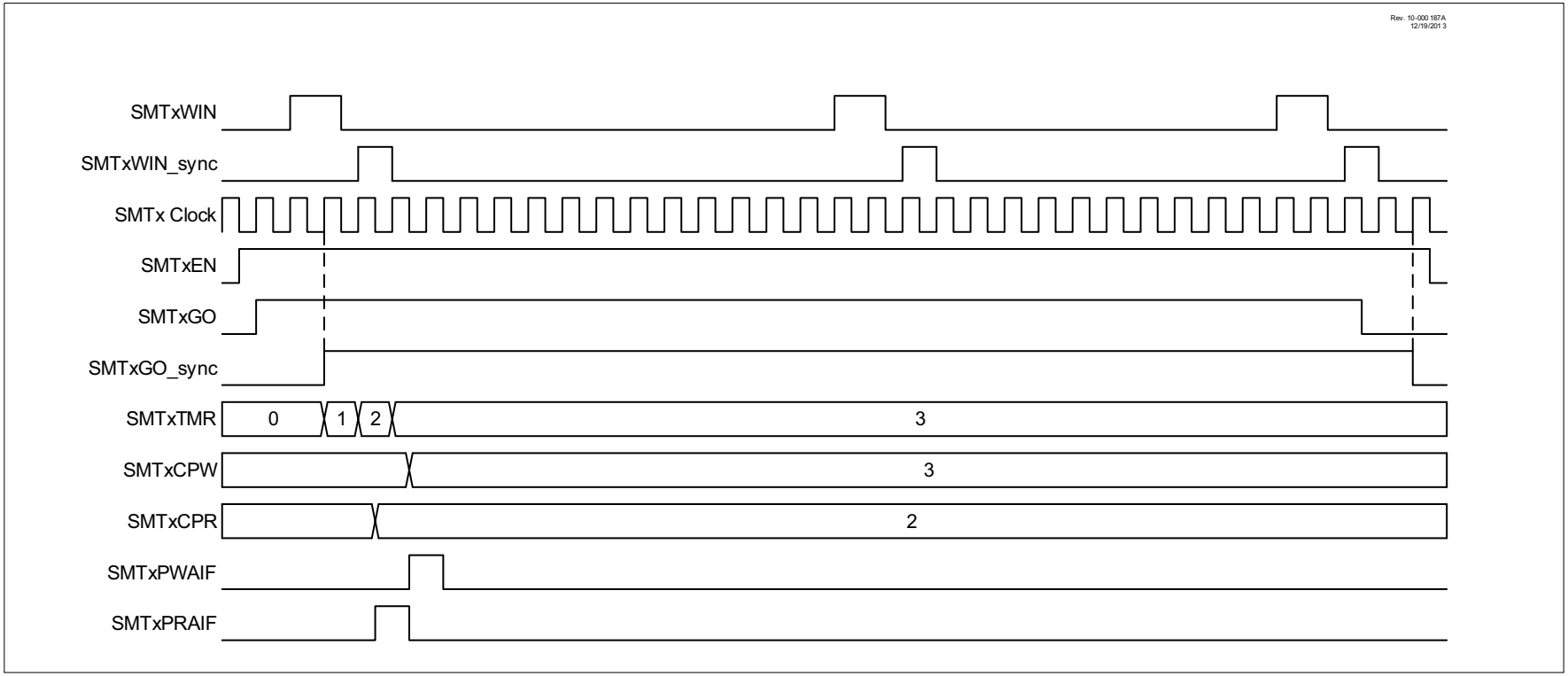
bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
If, on the rising edge of SCL, SDA is sampled low when the module is outputting a high state, the BCL1IF bit of the PIR3 register is set, and bus goes idle
1 = Enable slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the eighth falling edge of SCL for a matching received address byte; CKP bit of the SSPxCON1 register will be cleared and the SCL will be held low.
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the eighth falling edge of SCL for a received data byte; slave hardware clears the CKP bit of the SSPxCON1 register and SCL is held low.
0 = Data holding is disabled

Note 1: For daisy-chained SPI operation; allows the user to ignore all but the last received byte. SSPOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSPxBUF.
2: This bit has no effect in Slave modes that Start and Stop condition detection is explicitly listed as enabled.
3: The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is set.

FIGURE 32-17: CAPTURE MODE SINGLE ACQUISITION TIMING DIAGRAM



33.1.1.5 TSR Status

The TRMT bit of the TX1STA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note:	The TSR register is not mapped in data memory, so it is not available to the user.

33.1.1.6 Transmitting 9-Bit Characters

The EUSART supports 9-bit character transmissions. When the TX9 bit of the TX1STA register is set, the EUSART will shift nine bits out for each character transmitted. The TX9D bit of the TX1STA register is the ninth, and Most Significant data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TXREG. All nine bits of data will be transferred to the TSR shift register immediately after the TXREG is written.

A special 9-bit Address mode is available for use with multiple receivers. See **Section 33.1.2.7 "Address Detection"** for more information on the Address mode.

33.1.1.7 Asynchronous Transmission Set-up:

1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 33.3 "EUSART Baud Rate Generator (BRG)"**).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Set SCKP bit if inverted transmit is desired.
5. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
6. If interrupts are desired, set the TXIE interrupt enable bit of the PIE3 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
7. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
8. Load 8-bit data into the TXREG register. This will start the transmission.

FIGURE 33-3: ASYNCHRONOUS TRANSMISSION

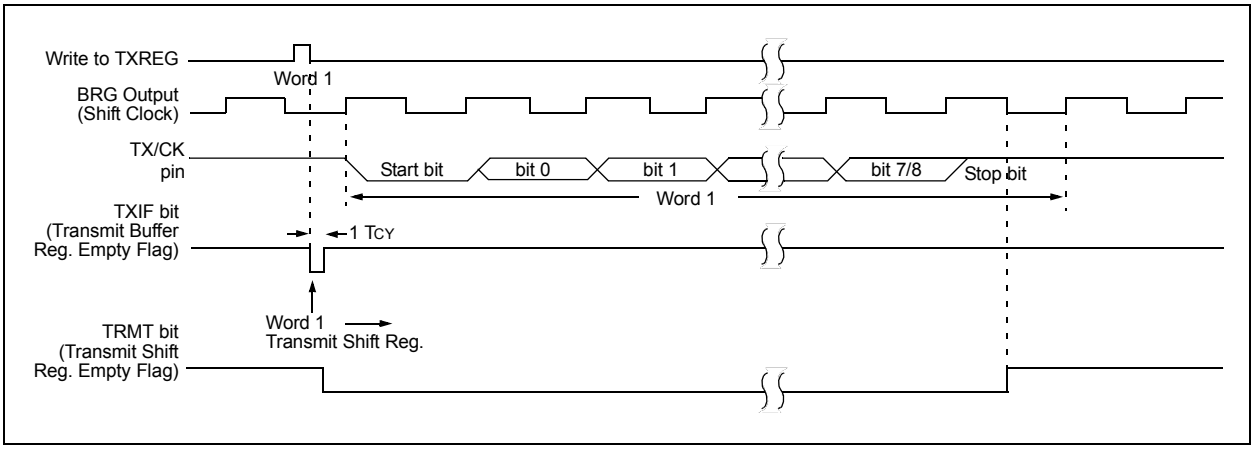
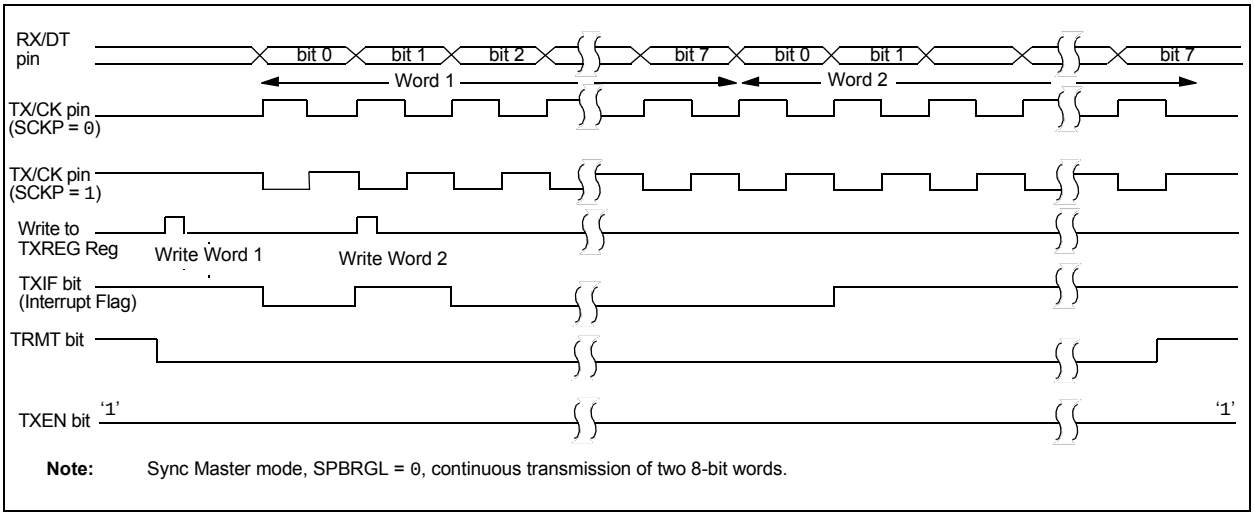
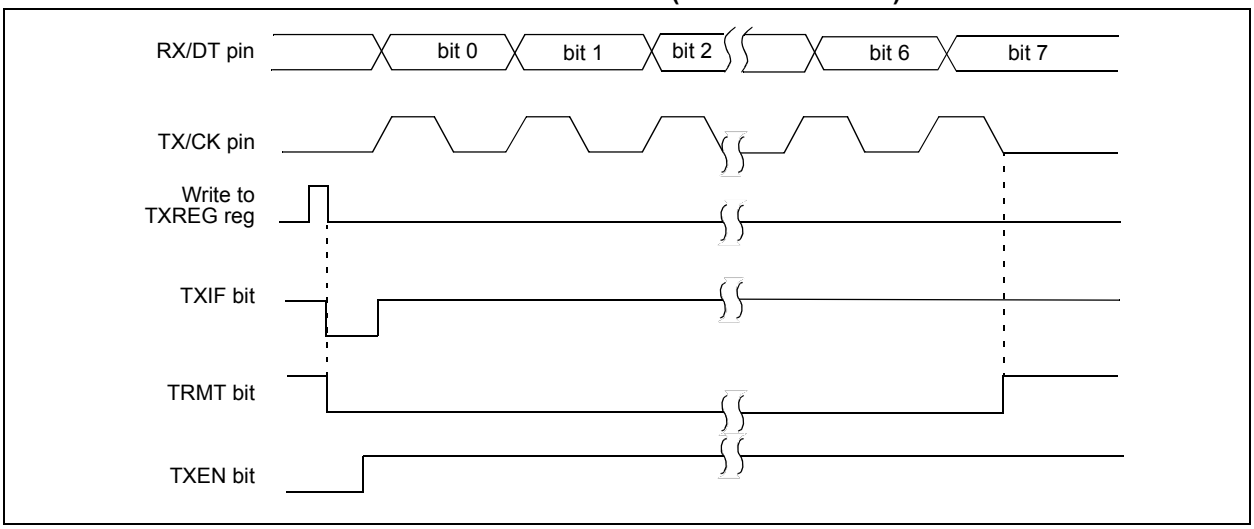


FIGURE 33-10: SYNCHRONOUS TRANSMISSION



Note: Sync Master mode, SPBRGL = 0, continuous transmission of two 8-bit words.

FIGURE 33-11: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



33.4.1.5 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RC1STA register) or the Continuous Receive Enable bit (CREN of the RC1STA register).

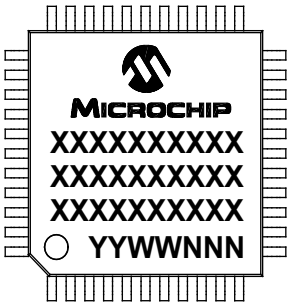
When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

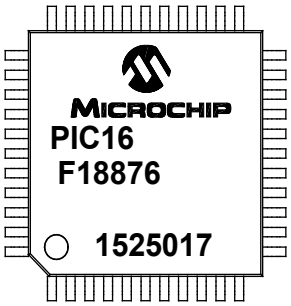
Note:	If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

40.1 Package Marking Information (Continued)

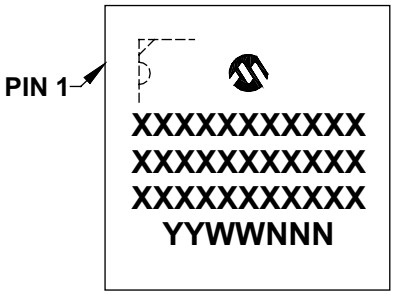
44-Lead TQFP (10x10x1 mm)



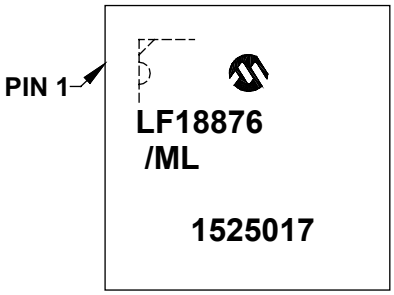
Example



44-Lead QFN (8x8x0.9 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.