Infineon Technologies - SAK-TC1767-256F133HR AD Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	133MHz
Connectivity	ASC, CANbus, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	88
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 4x10b, 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-tc1767-256f133hr-ad

2.2.2 System Features of the TC1767 device

The TC1767 has the following features:

Packages

- PG-LQFP-176-5 package, 0.5 mm pitch

Clock Frequencies

- Maximum CPU clock frequency: 133 MHz[1)]
- Maximum PCP clock frequency: 133 MHz[2)]
- Maximum SPB clock frequency: 80 MHz[3)]

1) For CPU frequencies > 80 MHz, 2:1 mode has to be enabled. CPU 2:1 mode means: $f_{SPB} = 0.5 * f_{CPU}$

2) For PCP frequencies > 80 MHz, 2:1 mode has to be enabled. PCP 2:1 mode means: $f_{SPB} = 0.5 * f_{PCP}$

3) CPU 1:1 Mode means: $f_{SPB} = f_{CPU}$. PCP 1:1 mode means: $f_{SPB} = f_{PCP}$

2.3.6.1 Boot ROM

The internal 16 Kbyte Boot ROM (BROM) is divided into two parts, used for:

- firmware (Boot ROM), and
- factory test routines (Test ROM).

The different sections of the firmware in Boot ROM provide startup and boot operations after reset. The TestROM is reserved for special routines, which are used for testing, stressing and qualification of the component.

2.3.6.2 Overlay RAM and Data Acquisition

The overlay memory OVRAM is provided in the PMU especially for redirection of data accesses to program memory to the OVRAM by using the data overlay function. The data overlay functionality itself is controlled in the DMI module.

For online data acquisition (OLDA) of application or calibration data a virtual 32 KB memory range is provided which can be accessed without error reporting. Accesses to this OLDA range can also be redirected to an overlay memory.

2.3.6.3 Emulation Memory Interface

In TC1767 Emulation Device, an Emulation Memory (EMEM) is provided, which can fully be used for calibration via program memory or OLDA overlay. The Emulation Memory interface shown in **Figure 3** is a 64-bit wide memory interface that controls the CPU-accesses to the Emulation Memory in the TC1767 Emulation Device. In the TC1767 production device, the EMEM interface is always disabled.

2.3.6.4 Tuning Protection

Tuning protection is required by the user to absolutely protect control data (e.g. for engine control), serial number and user software, stored in the Flash, from being manipulated, and to safely detect changed or disturbed data. For the internal Flash, these protection requirements are excellently fulfilled in the TC1767 with

- Flash read and write protection with user-specific protection levels, and with
- dedicated HW and firmware, supporting the internal Flash read protection, and with
- the Alternate Boot Mode.

Special tuning protection support is provided for external Flash, which must also be protected.

2.3.6.5 Program and Data Flash

The embedded Flash module of PMU0 includes 2 Mbyte of Flash memory for code or constant data (called Program Flash) and additionally 64 Kbyte of Flash memory used for emulation of EEPROM data (called Data Flash). The Program Flash is realized as

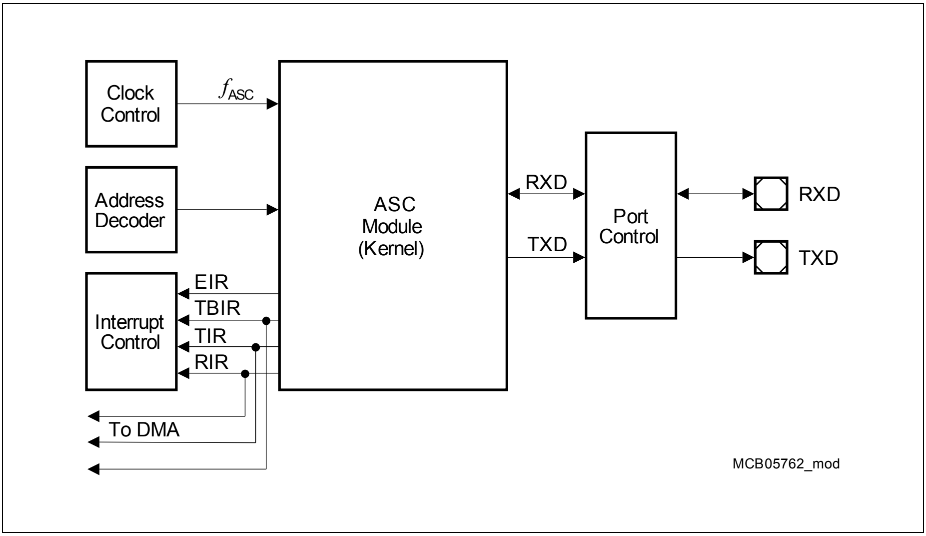

Figure 5 General Block Diagram of the ASC Interface

The ASC provides serial communication between the TC1767 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock that is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal, which can be accurately adjusted by a prescaler implemented as fractional divider.

  - f_{GPTA}/4 maximum input signal frequency in 2-sensor Mode, f_{GPTA}/6 maximum input signal frequency in 3-sensor Mode
- Duty Cycle Measurement (DCM)
  - Four independent units
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Clock Distribution Unit (CDU)
  - One unit
  - Provides nine clock output signals:
    f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
  - Two independent units
  - Two operating modes (Free-Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 units related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Local Timer Cell (LTC)
  - 64 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

Interrupt Sharing Unit

- 143 interrupt sources, generating up to 46 service requests

- Different Boot modes to use application software not yet programmed to the Flash.
- A total of four hardware breakpoints for the TriCore based on instruction address, data address or combination of both.
- Unlimited number of software breakpoints (DEBUG instruction) for TriCore and PCP .
- Debug event generated by access to a specific address via the system peripheral bus.
- Tool access to all SFRs and internal memories independent of the Cores.
- Two central Break Switches to collect debug events from all modules (TriCore, PCP, DMA, BCU, break input pins) and distribute them selectively to breakable modules (TriCore, PCP, break output pins).
- Central Suspend Switch to suspend parts of the system (TriCore, PCP, Peripherals) instead if breaking them as reaction to a debug event.
- Dedicated interrupt resources to handle debug events inside TriCore (breakpoint trap, software interrupt) and Cerberus (can trigger PCP), e.g. for implementing Monitor programs.
- Access to all OCDS Level 1 resources also for TriCore and PCP themselvesitself for debug tools integrated into the application code.
- Triggered Transfer of data in response to a debug event; if target is programmed to be a device interface simple variable tracing can be done.

Additionally, in depth performance analysis and profiling support is provided by the Emulation Device through MCDS Event Counters driven by a variety of trigger signals (e.g. cache hit, wait state, interrupt accepted).

2.5.2 Real Time Trace

For detailed tracing of the system's behavior a pin-compatible Emulation Device is available.[1)]

2.5.3 Calibration Support

Two main use cases are catered for by resources in addition the OCDS Level 1 infrastructure: Overlay of non-volatile on-chip memory and non-intrusive signaling:

- 8 KB SRAM for Overlay.
- Can be split into up to 16 blocks which can overlay independent regions of on-chip Data Flash.
- Changing the configuration is triggered by a single SFR access to maintain consistency.
- Overlay configuration switch does not require the TriCore to be stopped or suspended.

1) The OCDS L2 interface of AudoNG is not available.

- Invalidation of the Data Cache (maintaining write-back data) can be done concurrently with the same SFR.
- 256 KB additional Overlay RAM on Emulation Device.
- The 256 KB Trace memory of the Emulation Device can optionally be used for Overlay also.
- A dedicated trigger SFR with 32 independent status bits is provided to centrally post requests from application code to the host computer.
- The host is notified automatically when the trigger SFR is updated by the TriCore or PCP. No polling via a system bus is required.

2.5.4 Tool Interfaces

Three options exist for the communication channel between Tools (e.g. Debugger, Calibration Tool) and TC1767:

- Two wire DAP (Device Access Port) protocol for long connections or noisy environments.
- Four (or five) wire JTAG (IEEE 1149.1) for standardized manufacturing tests.
- CAN (plus software linked into the application code) for low bandwidth deeply embedded purposes.
- DAP and JTAG are clocked by the tool.
- Bit clock up to 40 MHz for JTAG, up to 80 MHz for DAP.
- Hot attach (i.e. physical disconnect/reconnect of the host connection without reset of the TC1767) for all interfaces.
- Infineon standard DAS (Device Access Server) implementation for seamless, transparent tool access over any supported interface.
- Lock mechanism to prevent unauthorized tool access to critical application code.

2.5.5 Self-Test Support

Some manufacturing tests can be invoked by the application (e.g. after power-on) if needed:

- Hardware-accelerated checksum calculation (e.g. for Flash content).

2.5.6 FAR Support

To efficiently locate and identify faults after integration of a TC1767 into a system special functions are available:

- Boundary Scan (IEEE 1149.1) via JTAG and DAP.
- SSCM (Single Scan Chain Mode[1)]) for structural scan testing of the chip itself.

1) This function requires access to some device pins (e.g. $\overline{\text{TESTMODE}}$) in addition to those needed for OCDS.

3.1.1 TC1767 Pin Configuration: PG-LQFP-176-5

This chapter shows the pin configuration of the package variant PG-LQFP-176-5[1].

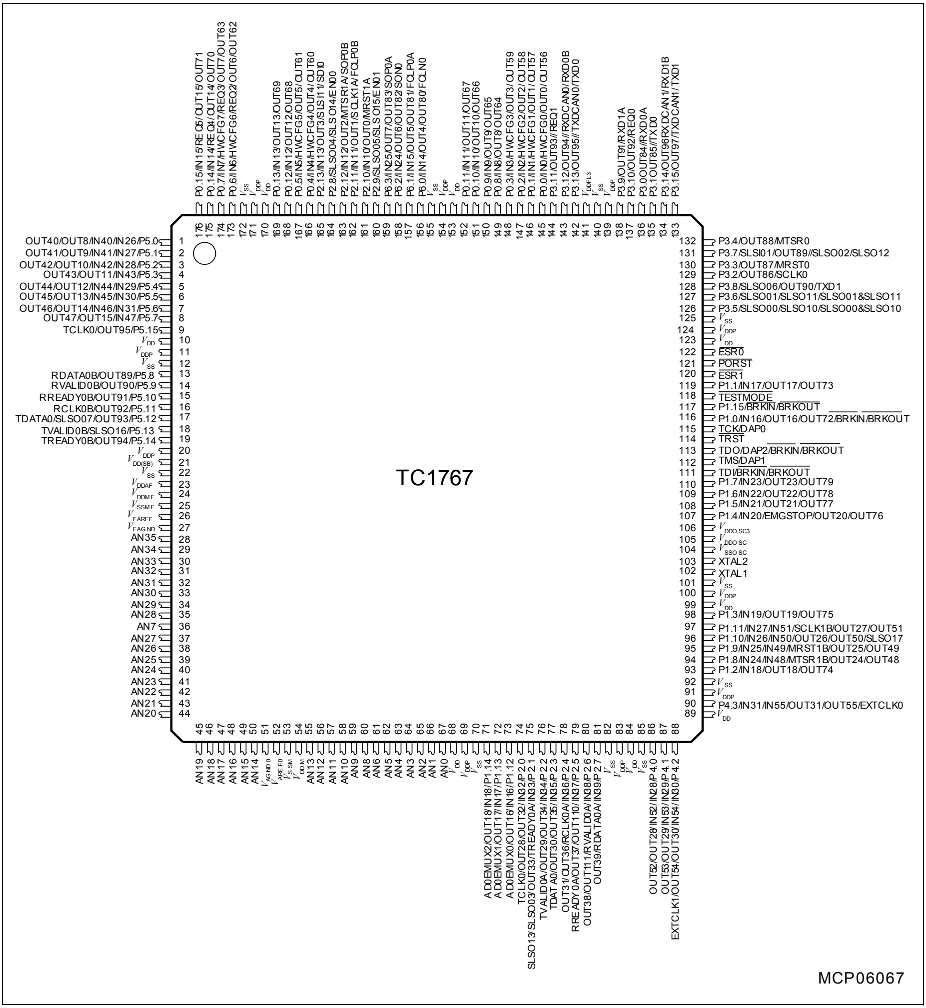

Figure 16 TC1767 Pinning for PG-LQFP-176-5

1) TC1767 ED: PG-LQFP-176-6

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1])

Pin	Symbol	Ctrl.	Type	Function
Port 0				
145	P0.0	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 0**
	IN0	I		**GPTA0 Input 0**
	IN0	I		**LTCA2 Input 0**
	HWCFG0	I		**Hardware Configuration Input 0**
	OUT0	O1		**GPTA0 Output 0**
	OUT56	O2		**GPTA0 Output 56**
	OUT0	O3		**LTCA2 Output 0**
146	P0.1	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 1**
	IN1	I		**GPTA0 Input 1**
	IN1	I		**LTCA2 Input 1**
	HWCFG1	I		**Hardware Configuration Input 1**
	OUT1	O1		**GPTA0 Output 1**
	OUT57	O2		**GPTA0 Output 57**
	OUT1	O3		**LTCA2 Output 1**
147	P0.2	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 2**
	IN2	I		**GPTA0 Input 2**
	IN2	I		**LTCA2 Input 2**
	HWCFG2	I		**Hardware Configuration Input 2**
	OUT2	O1		**GPTA0 Output 2**
	OUT58	O2		**GPTA0 Output 58**
	OUT2	O3		**LTCA2 Output 2**
148	P0.3	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 3**
	IN3	I		**GPTA0 Input 3**
	IN3	I		**LTCA2 Input 3**
	HWCFG3	I		**Hardware Configuration Input 3**
	OUT3	O1		**GPTA0 Output 3**
	OUT59	O2		**GPTA0 Output 59**
	OUT3	O3		**LTCA2 Output 3**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
166	P0.4	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 4**
	IN4	I		**GPTA0 Input 4**
	IN4	I		**LTCA2 Input 4**
	HWCFG4	I		**Hardware Configuration Input 4**
	OUT4	O1		**GPTA0 Output 4**
	OUT60	O2		**GPTA0 Output 60**
	OUT4	O3		**LTCA2 Output 4**
167	P0.5	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 5**
	IN5	I		**GPTA0 Input 5**
	IN5	I		**LTCA2 Input 5**
	HWCFG5	I		**Hardware Configuration Input 5**
	OUT5	O1		**GPTA0 Output 5**
	OUT61	O2		**GPTA0 Output 61**
	OUT5	O3		**LTCA2 Output 5**
173	P0.6	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 6**
	IN6	I		**GPTA0 Input 6**
	IN6	I		**LTCA2 Input 6**
	HWCFG6	I		**Hardware Configuration Input 6**
	REQ2	I		**External Request Input 2**
	OUT6	O1		**GPTA0 Output 6**
	OUT62	O2		**GPTA0 Output 62**
	OUT6	O3		**LTCA2 Output 6**
174	P0.7	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 7**
	IN7	I		**GPTA0 Input 7**
	IN7	I		**LTCA2 Input 7**
	HWCFG7	I		**Hardware Configuration Input 7**
	REQ3	I		**External Request Input 3**
	OUT7	O1		**GPTA0 Output 7**
	OUT63	O2		**GPTA0 Output 63**
	OUT7	O3		**LTCA2 Output 7**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
74	P2.0	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 0**
	IN32	I		**GPTA0 Input 32**
	OUT32	O1		**GPTA0 Output 32**
	TCLK0	O2		**MLI0 Transmitter Clock Output 0**
	OUT28	O3		**LTCA2 Output 28**
75	P2.1	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 1**
	IN33	I		**GPTA0 Input 33**
	TREADY0A	I		**MLI0 Transmitter Ready Input A**
	OUT33	O1		**GPTA0 Output 33**
	SLSO03	O2		**SSC0 Slave Select Output Line 3**
	SLSO13	O3		**SSC1 Slave Select Output Line 3**
76	P2.2	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 2**
	IN34	I		**GPTA0 Input 34**
	OUT34	O1		**GPTA0 Output 34**
	TVALID0	O2		**MLI0 Transmitter Valid Output**
	OUT29	O3		**LTCA2 Output 29**
77	P2.3	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 3**
	IN35	I		**GPTA0 Input 35**
	OUT35	O1		**GPTA0 Output 35**
	TDATA0	O2		**MLI0 Transmitter Data Output**
	OUT30	O3		**LTCA2 Output 30**
78	P2.4	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 4**
	IN36	I		**GPTA0 Input 36**
	RCLK0A	I		**MLI Receiver Clock Input A**
	OUT36	O1		**GPTA0 Output 36**
	OUT36	O2		**GPTA0 Output 36**
	OUT31	O3		**LTCA2 Output 31**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P4.1	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 1**
	IN29	I		**GPTA0 Input 29**
	IN53	I		**GPTA0 Input 53**
	OUT29	O1		**GPTA0 Output 29**
	OUT53	O2		**GPTA0 Output 53**
	Reserved	O3		-
88	P4.2	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 2**
	IN30	I		**GPTA0 Input 30**
	IN54	I		**GPTA0 Input 54**
	OUT30	O1		**GPTA0 Output 30**
	OUT54	O2		**GPTA0 Output 54**
	EXTCLK1	O3		**External Clock 1 Output**
90	P4.3	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 3**
	IN31	I		**GPTA0 Input 31**
	IN55	I		**GPTA0 Input 55**
	OUT31	O1		**GPTA0 Output 31**
	OUT55	O2		**GPTA0 Output 55**
	EXTCLK0	O3		**External Clock 0 Output**
Port 5				
1	P5.0	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 0**
	IN40	I		**GPTA0 Input 40**
	IN26	I		**LTCA2 Input 26**
	OUT40	O1		**GPTA0 Output 40**
	OUT8	O2		**LTCA2 Output 8**
	Reserved	O3		-

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2	P5.1	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 1**
	IN41	I		**GPTA0 Input 41**
	IN27	I		**LTCA2 Input 27**
	OUT41	O1		**GPTA0 Output 41**
	OUT9	O2		**LTCA2 Output 9**
	Reserved	O3		-
3	P5.2	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 2**
	IN42	I		**GPTA0 Input 42**
	IN28	I		**LTCA2 Input 28**
	OUT42	O1		**GPTA0 Output 42**
	OUT10	O2		**LTCA2 Output 10**
	Reserved	O3		-
4	P5.3	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 3**
	IN43	I		**GPTA0 Input 43**
	OUT43	O1		**GPTA0 Output 43**
	OUT11	O2		**LTCA2 Output 11**
	Reserved	O3		-
5	P5.4	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 4**
	IN44	I		**GPTA0 Input 44**
	IN29	I		**LTCA2 Input 29**
	OUT44	O1		**GPTA0 Output 44**
	OUT12	O2		**LTCA2 Output 12**
	Reserved	O3		-
6	P5.5	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 5**
	IN45	I		**GPTA0 Input 45**
	IN30	I		**LTCA2 Input 30**
	OUT45	O1		**GPTA0 Output 45**
	OUT13	O2		**LTCA2 Output 13**
	Reserved	O3		-

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
10, 21[3], 68, 84, 89, 99, 123, 153, 170	V_{DD}	-	-	**Digital Core Power Supply (1.5V)**
11, 20, 69, 83, 91, 100, 124, 139, 154, 171	V_{DDP}	-	-	**Port Power Supply (3.3V)**
12, 22, 70, 82, 85, 92, 101, 125, 140, 155, 172	V_{SS}	-	-	**Digital Ground**
105	V_{DDOSC}	-	-	**Main Oscillator and PLL Power Supply (1.5V)**
106	V_{DDOSC3}	-	-	**Main Oscillator Power Supply (3.3V)**
104	V_{SSOSC}	-	-	**Main Oscillator and PLL Ground**
141	V_{DDFL3}	-	-	**Power Supply for Flash (3.3V)**
102	XTAL1	I		**Main Oscillator Input**
103	XTAL2	O		**Main Oscillator Output**

5 Electrical Parameters

5.1 General Parameters

5.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1767 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1767 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1767 designed in.

Table 13 Conversion Time (Operating Conditions apply)

Parameter	Symbol		Value	Unit	Note
Conversion time with post-calibration	t_C	CC	$2 \times T_{ADC} + (4 + STC + n) \times T_{ADCI}$	µs	n = 8, 10, 12 for n - bit conversion $T_{ADC} = 1 / f_{ADC}$ $T_{ADCI} = 1 / f_{ADCI}$
Conversion time without post-calibration			$2 \times T_{ADC} + (2 + STC + n) \times T_{ADCI}$		

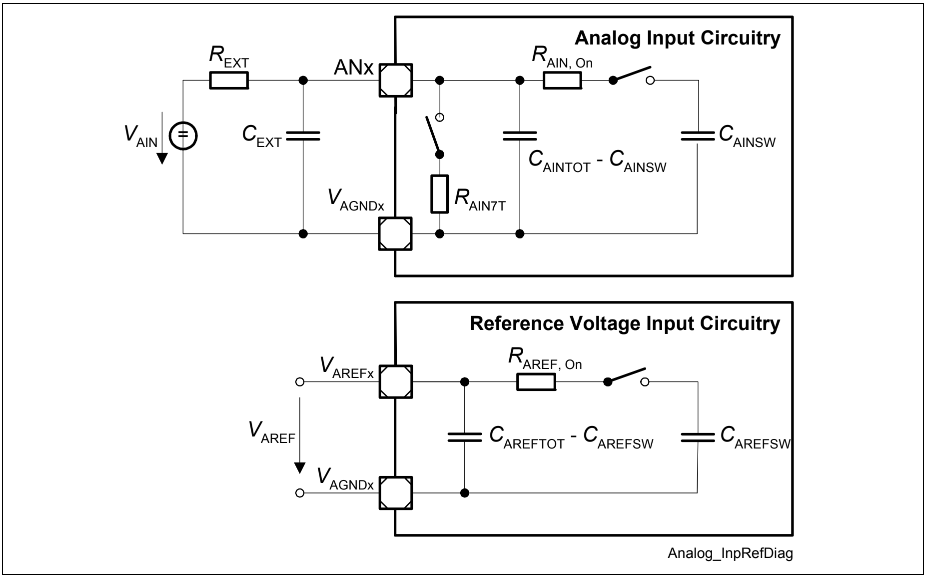

Figure 18 ADC0/ADC1 Input Circuits

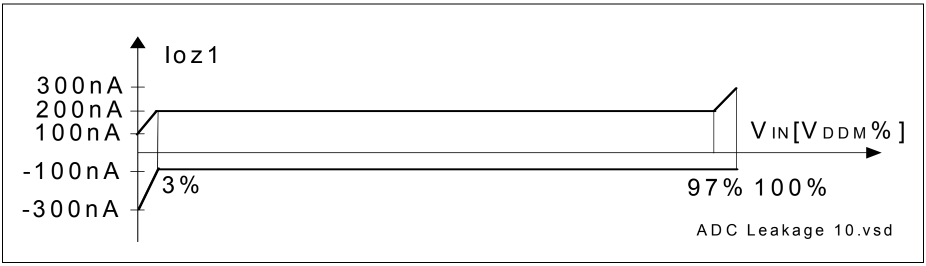

Figure 19 ADC0/ADC1Analog Inputs Leakage

3. The $\overline{\text{PORST}}$ signal may be deactivated after all V_{DD5}, $V_{DD3.3}$, $V_{DD1.5}$, and V_{AREF} power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
4. At normal power down the $\overline{\text{PORST}}$ signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
5. At power fail the $\overline{\text{PORST}}$ signal must be activated at latest when any 3.3 V or 1.5 V power supply voltage falls 12% below the nominal level. The same limit of 3.3 V-12% applies to the 5 V power supply too. If, under these conditions, the PORST is activated during a Flash write, only the memory row that was the target of the write at the moment of the power loss will contain unreliable content. In order to ensure clean power-down behavior, the $\overline{\text{PORST}}$ signal should be activated as close as possible to the normal operating voltage range.
6. In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rules number 2 and 4.
7. Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
8. Aditionally, regarding the ADC reference voltage V_{AREF}:
   – V_{AREF} must power-up at the same time or later than V_{DDM}, and
   – V_{AREF} must power-down eather earlier or at latest to satisfy the condition $V_{AREF} < V_{DDM} + 0.5$ V. This is required in order to prevent discharge of V_{AREF} filter capacitance through the ESD diodes through the V_{DDM} power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

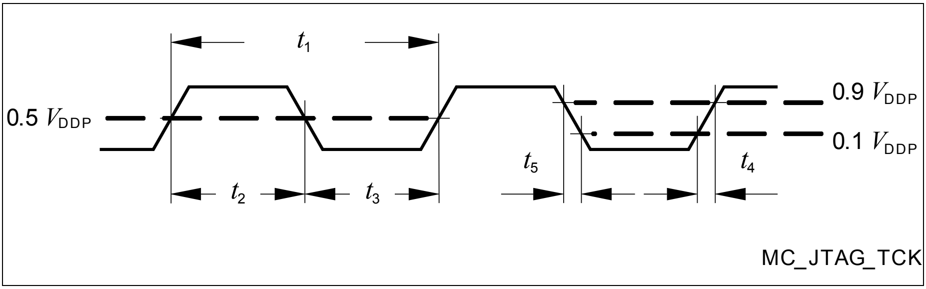

Figure 27 Test Clock Timing (TCK)

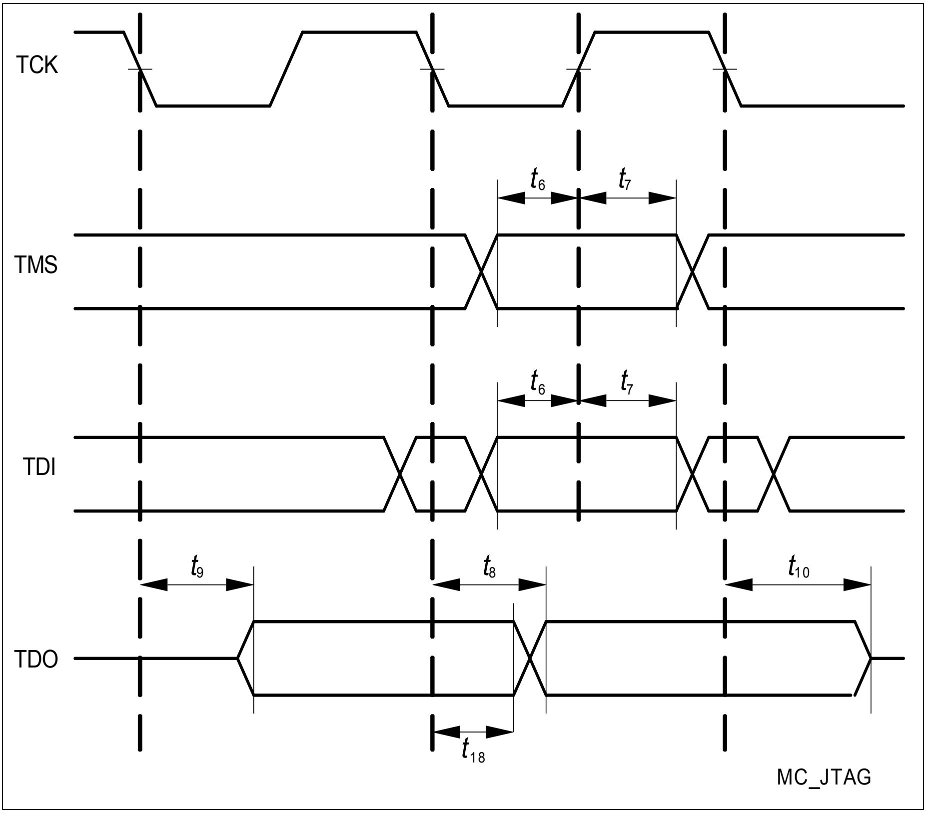

Figure 28 JTAG Timing

5.3.7 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 22 DAP Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	12.5	–	–	ns	–
DAP0 high time	t_{12} SR	4	–	–	ns	–
DAP0 low time	t_{13} SR	4	–	–	ns	–
DAP0 clock rise time	t_{14} SR	–	–	2	ns	–
DAP0 clock fall time	t_{15} SR	–	–	2	ns	–
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	–
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	–
DAP1 valid per DAP0 clock period[1]	t_{19} SR	8	–	–	ns	80 MHz, C_L = 20 pF
	t_{19} SR	10	–	–	ns	40 MHz, C_L = 50 pF

1) The Host has to find a suitable sampling point by analyzing the sync telegram response.

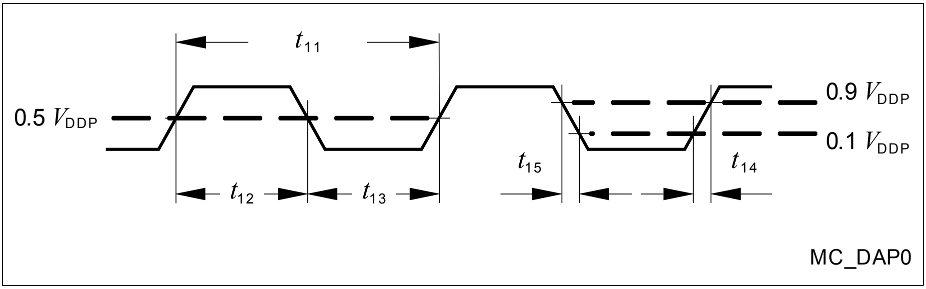

Figure 29 Test Clock Timing (DAP0)

7) The RCLK max. input rise/fall times are best case parameters for f_{SYS} = 80 MHz. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

5.3.8.2 Micro Second Channel (MSC) Interface Timing

Table 24 MSC Interface Timing (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
FCLP clock period[1)2)]	t_{40}	CC	$2 \times T_{MSC}$[3)]	–	–	ns	–
SOP/ENx outputs delay from FCLP rising edge	t_{45}	CC	-10		10	ns	–
SDI bit time	t_{46}	CC	$8 \times T_{MSC}$		–	ns	–
SDI rise time	t_{48}	SR			100	ns	–
SDI fall time	t_{49}	SR			100	ns	–

1) FCLP signal rise/fall times are the same as the A2 Pads rise/fall times.

2) FCLP signal high and low can be minimum $1 \times T_{MSC}$.

3) $T_{MSCmin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 80 MHz, t_{40} = 25 ns

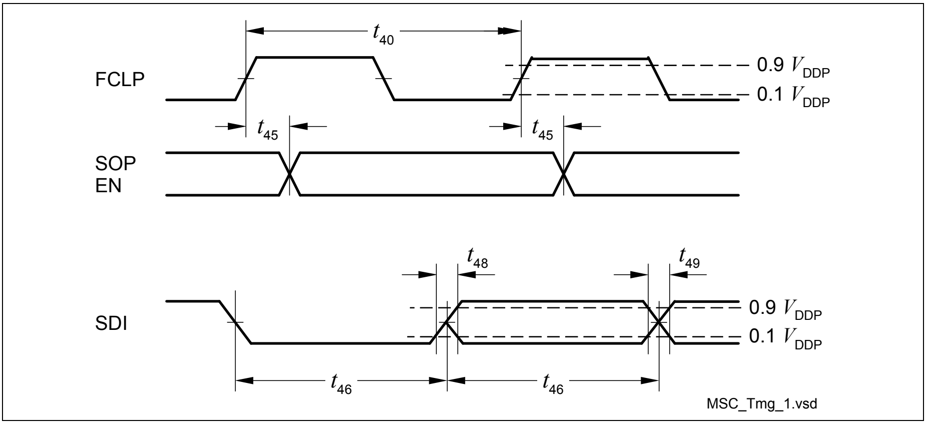

Figure 33 MSC Interface Timing

Note: Sample the data at SOP with the falling edge of FCLP in the target device.

5.3.8.3 SSC Master / Slave Mode Timing

5.4.3 Flash Memory Parameters

The data retention time of the TC1767's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 27 Flash Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Program Flash Retention Time, Physical Sector[1)2)]	t_{RET}	CC	20	–	–	years	Max. 1000 erase/program cycles
Program Flash Retention Time Logical Sector[1)2)]	t_{RETL}	CC	20	–	–	years	Max. 100 erase/program cycles
Data Flash Endurance per 32 KB Sector	N_E	CC	30 000	–	–	cycles	Max. data retention time 5 years
Data Flash Endurance, EEPROM Emulation (4 × 16 KB)	N_{E8}	CC	120000	–	–	cycles	Max. data retention time 5 years
Programming Time per Page[3)]	t_{PR}	CC	–	–	5	ms	–
Program Flash Erase Time per 256-KB Sector	t_{ERP}	CC	–	–	5	s	f_{CPU} = 133 MHz
Data Flash Erase Time for 2 x 32-KB Sector	t_{ERD}	CC	–	–	2.5	s	f_{CPU} = 133 MHz
Wake-up time	t_{WU}	CC	–	–	$4000/f_{CPU}$ +180	µs	–

1) Storage and inactive time included.

2) At average weighted junction temperature T_j = 100°C, or
the retention time at average weighted temperature of T_j = 110°C is minimum 10 years, or
the retention time at average weighted temperature of T_j = 150°C is minimum 0.7 years.

3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5 ms.