Infineon Technologies - TC1767256F133HLADKXUMA1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	133MHz
Connectivity	ASC, CANbus, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	88
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 4x10b, 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1767256f133hladkxuma1

Edition 2012-07

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

1 Summary of Features

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 133 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 8 Kbyte Parameter Memory (PRAM)
  - 16 Kbyte Code Memory (CMEM)
  - 133 MHz operation at full temperature range
- Multiple on-chip memories
  - 72 Kbyte Data Memory (LDRAM)
  - 24 Kbyte Code Scratchpad Memory (SPRAM)
  - 2 Mbyte Program Flash Memory (PFlash)
  - 64 Kbyte Data Flash Memory (DFlash, represents 16 Kbyte EEPROM)
  - Instruction Cache: up to 8 Kbyte (ICACHE, configurable)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 8-Channel DMA Controller
- Sophisticated interrupt system with 2 × 255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Two High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 2 CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - One General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 32 analog input lines for ADC

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1767 please refer to the **"Product Catalog Microcontrollers"**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1767 Derivative Synopsis

Derivative	Ambient Temperature Range	CPU frequency	Wire Bond Material
SAK-TC1767-256F133HL	T_A = -40°C to +125°C	133 MHz	Gold
SAK-TC1767-256F80HL	T_A = -40°C to +125°C	80 MHz	Gold
SAK-TC1767-256F133HR	T_A = -40°C to +125°C	133 MHz	Copper

register names contain a module name prefix, separated by an underscore character "_" from the actual register name (for example, "ASC0_CON", where "ASC0" is the module name prefix, and "CON" is the kernel register name). In chapters describing the kernels of the peripheral modules, the registers are mainly referenced with their kernel register names. The peripheral module implementation sections mainly refer to the actual register names with module prefixes.

- Variables used to describe sets of processing units or registers appear in mixed upper and lower cases. For example, register name "MSGCFGn" refers to multiple "MSGCFG" registers with variable n. The bounds of the variables are always given where the register expression is first used (for example, "n = 0-31"), and are repeated as needed in the rest of the text.
- The default radix is decimal. Hexadecimal constants are suffixed with a subscript letter "H", as in 100_H. Binary constants are suffixed with a subscript letter "B", as in: 111_B.
- When the extent of register fields, groups register bits, or groups of pins are collectively named in the body of the document, they are represented as "NAME[A:B]", which defines a range for the named group from B to A. Individual bits, signals, or pins are given as "NAME[C]" where the range of the variable C is given in the text. For example: CFG[2:0] and SRPN[0].
- Units are abbreviated as follows:
  - **MHz** = Megahertz
  - **µs** = Microseconds
  - **kBaud, kbit** = 1000 characters/bits per second
  - **MBaud, Mbit** = 1,000,000 characters/bits per second
  - **Kbyte, KB** = 1024 bytes of memory
  - **Mbyte, MB** = 1048576 bytes of memory

    In general, the k prefix scales a unit by 1000 whereas the K prefix scales a unit by 1024. Hence, the Kbyte unit scales the expression preceding it by 1024. The kBaud unit scales the expression preceding it by 1000. The M prefix scales by 1,000,000 or 1048576, and µ scales by .000001. For example, 1 Kbyte is 1024 bytes, 1 Mbyte is 1024 × 1024 bytes, 1 kBaud/kbit are 1000 characters/bits per second, 1 MBaud/Mbit are 1000000 characters/bits per second, and 1 MHz is 1,000,000 Hz.
- Data format quantities are defined as follows:
  - **Byte** = 8-bit quantity
  - **Half-word** = 16-bit quantity
  - **Word** = 32-bit quantity
  - **Double-word** = 64-bit quantity

NC	Non Connect
NMI	Non-Maskable Interrupt
OCDS	On-Chip Debug Support
OVRAM	Overlay Memory
PCP	Peripheral Control Processor
PMU	Program Memory Unit
PLL	Phase Locked Loop
PFLASH	Program Flash Memory
PMI	Program Memory Interface
PMU	Program Memory Unit
PRAM	PCP Parameter RAM
RAM	Random Access Memory
RISC	Reduced Instruction Set Computing
SBCU	System Peripheral Bus Control Unit
SCU	System Control Unit
SFR	Special Function Register
SPB	System Peripheral Bus
SPRAM	Scratch-Pad RAM
SRAM	Static Data Memory
SRN	Service Request Node
SSC	Synchronous Serial Controller
STM	System Timer
WDT	Watchdog Timer

2.2.2 System Features of the TC1767 device

The TC1767 has the following features:

Packages

- PG-LQFP-176-5 package, 0.5 mm pitch

Clock Frequencies

- Maximum CPU clock frequency: 133 MHz[1)]
- Maximum PCP clock frequency: 133 MHz[2)]
- Maximum SPB clock frequency: 80 MHz[3)]

1) For CPU frequencies > 80 MHz, 2:1 mode has to be enabled. CPU 2:1 mode means: $f_{SPB} = 0.5 * f_{CPU}$
2) For PCP frequencies > 80 MHz, 2:1 mode has to be enabled. PCP 2:1 mode means: $f_{SPB} = 0.5 * f_{PCP}$
3) CPU 1:1 Mode means: $f_{SPB} = f_{CPU}$. PCP 1:1 mode means: $f_{SPB} = f_{PCP}$

2.3.4 System Control Unit

The following SCU introduction gives an overview about the TC1767 System Control Unit (SCU).

2.3.4.1 Clock Generation Unit

The Clock Generation Unit (CGU) allows a very flexible clock generation for the TC1767. During user program execution the frequency can be programmed for an optimal ratio between performance and power consumption.

2.3.4.2 Features of the Watchdog Timer

The main features of the WDT are summarized here.

- 16-bit Watchdog counter
- Selectable input frequency: $f_{FPI}/256$ or $f_{FPI}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Prewarning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated Password Access mechanism with fixed and user-definable password fields
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled
- Double Reset Detection: If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1767 is held in reset until a system / class 0 reset occurs.

2.3.4.3 Reset Operation

The following reset request triggers are available:

- 1 External power-on hardware reset request trigger; $\overline{\text{PORST}}$, (cold reset)
- 2 External System Request reset triggers; $\overline{\text{ESR0}}$ and $\overline{\text{ESR1}}$ (warm reset)
- Watchdog Timer (WDT) reset request trigger, (warm reset)
- Software reset (SW), (warm reset)
- Debug (OCDS) reset request trigger, (warm reset)
- JTAG reset (special reset)
- Resets via the JTAG interface

Note: The JTAG and OCDS resets are described in the OCDS chapter.

There are two basic types of reset request triggers:

  - f_{GPTA}/4 maximum input signal frequency in 2-sensor Mode, f_{GPTA}/6 maximum input signal frequency in 3-sensor Mode
- Duty Cycle Measurement (DCM)
  - Four independent units
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Clock Distribution Unit (CDU)
  - One unit
  - Provides nine clock output signals: f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
  - Two independent units
  - Two operating modes (Free-Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 units related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Local Timer Cell (LTC)
  - 64 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

Interrupt Sharing Unit

- 143 interrupt sources, generating up to 46 service requests

- Invalidation of the Data Cache (maintaining write-back data) can be done concurrently with the same SFR.
- 256 KB additional Overlay RAM on Emulation Device.
- The 256 KB Trace memory of the Emulation Device can optionally be used for Overlay also.
- A dedicated trigger SFR with 32 independent status bits is provided to centrally post requests from application code to the host computer.
- The host is notified automatically when the trigger SFR is updated by the TriCore or PCP. No polling via a system bus is required.

2.5.4 Tool Interfaces

Three options exist for the communication channel between Tools (e.g. Debugger, Calibration Tool) and TC1767:

- Two wire DAP (Device Access Port) protocol for long connections or noisy environments.
- Four (or five) wire JTAG (IEEE 1149.1) for standardized manufacturing tests.
- CAN (plus software linked into the application code) for low bandwidth deeply embedded purposes.
- DAP and JTAG are clocked by the tool.
- Bit clock up to 40 MHz for JTAG, up to 80 MHz for DAP.
- Hot attach (i.e. physical disconnect/reconnect of the host connection without reset of the TC1767) for all interfaces.
- Infineon standard DAS (Device Access Server) implementation for seamless, transparent tool access over any supported interface.
- Lock mechanism to prevent unauthorized tool access to critical application code.

2.5.5 Self-Test Support

Some manufacturing tests can be invoked by the application (e.g. after power-on) if needed:

- Hardware-accelerated checksum calculation (e.g. for Flash content).

2.5.6 FAR Support

To efficiently locate and identify faults after integration of a TC1767 into a system special functions are available:

- Boundary Scan (IEEE 1149.1) via JTAG and DAP.
- SSCM (Single Scan Chain Mode[1)]) for structural scan testing of the chip itself.

1) This function requires access to some device pins (e.g. $\overline{\text{TESTMODE}}$) in addition to those needed for OCDS.

3 Pinning

3.1 TC1767 Pin Definition and Functions

Figure 15 shows the Logic Symbol of the device.

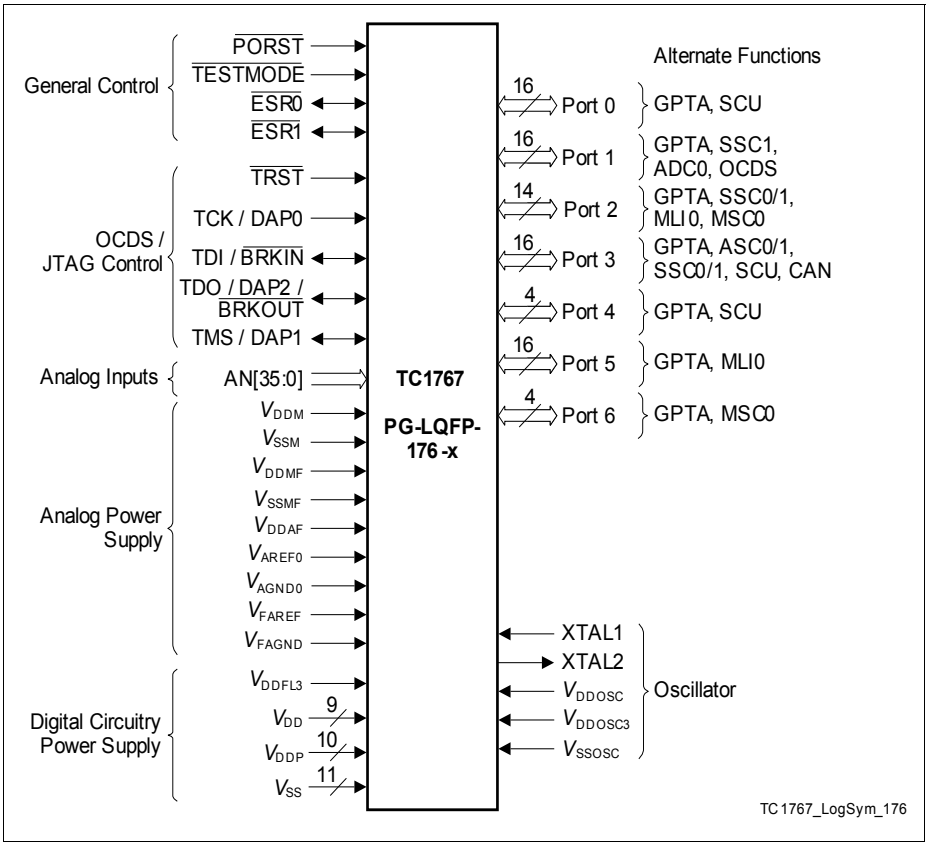

Figure 15 TC1767 Logic Symbol for the package variant PG-LQFP-176-5.

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
161	P2.10	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 10**
	MRST1A	I		**SSC1 Master Receive Input A**
	IN10	I		**LTCA2 Input 10**
	MRST1A	O1		**SSC1 Slave Transmit Output**
	OUT0	O2		**LTCA2 Output 0**
	Reserved	O3		**-**
162	P2.11	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 11**
	SCLK1A	I		**SSC1 Clock Input A**
	IN11	I		**LTCA2 Input 11**
	SCLK1A	O1		**SSC1 Clock Output A**
	OUT1	O2		**LTCA2 Output 1**
	FCLP0B	O3		**MSC0 Clock Output Positive B**
163	P2.12	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 12**
	MTSR1A	I		**SSC1 Slave Receive Input A**
	IN12	I		**LTCA2 Input 12**
	MTSR1A	O1		**SSC1 Master Transmit Output A**
	OUT2	O2		**LTCA2 Output 2**
	SOP0B	O3		**MSC0 Serial Data Output Positive B**
165	P2.13	I/O0	A1/ PU	**Port 2 General Purpose I/O Line 13**
	SLSI11	I		**SSC1 Slave Select Input 1**
	SDI0	I		**MSC0 Serial Data Input**
	IN13	I		**LTCA2 Input 13**
	OUT3	O1		**LTCA2 Output 3**
	Reserved	O2		**-**
	Reserved	O3		**-**
Port 3				

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
143	P3.12	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 12**
	RXDCAN0	I		**CAN Node 0 Receiver Input**
	RXD0B	I		**ASC0 Receiver Input B**
	RXD0B	O1		**ASC0 Receiver Output B (Synchronous Mode)**
	RXD0B	O2		**ASC0 Receiver Output B (Synchronous Mode)**
	OUT94	O3		**GPTA0 Output 94**
142	P3.13	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 13**
	TXDCAN0	O1		**CAN Node 0 Transmitter Output**
	TXD0	O2		**ASC0 Transmit Output**
	OUT95	O3		**GPTA0 Output 95**
134	P3.14	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 14**
	RXDCAN1	I		**CAN Node 1 Receiver Input**
	RXD1B	I		**ASC1 Receiver Input B**
	RXD1B	O1		**ASC1 Receiver Output B (Synchronous Mode)**
	RXD1B	O2		**ASC1 Receiver Output B (Synchronous Mode)**
	OUT96	O3		**GPTA0 Output 96**
133	P3.15	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 15**
	TXDCAN1	O1		**CAN Node 1 Transmitter Output**
	TXD1	O2		**ASC1 Transmit Output**
	OUT97	O3		**GPTA0 Output 97**
Port 4				
86	P4.0	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 0**
	IN28	I		**GPTA0 Input 28**
	IN52	I		**GPTA0 Input 52**
	OUT28	O1		**GPTA0 Output 28**
	OUT52	O2		**GPTA0 Output 52**
	Reserved	O3		**-**

5.1.3 Absolute Maximum Ratings

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions (V_{IN} > related V_{DD} or V_{IN} < V_{SS}) the voltage on the related V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 8 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient temperature	T_A	SR	-40	–	125	°C	Under bias
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	Under bias
Voltage at 1.5 V power supply pins with respect to V_{SS} 1)	V_{DD}	SR	–	–	2.25	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS} 2)	V_{DDP}	SR	–	–	3.75	V	–
Voltage at 5 V power supply pins with respect to V_{SS}	V_{DDM}	SR	–	–	5.5	V	–
Voltage on any Class A input pin and dedicated input pins with respect to V_{SS}	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{AGND}	V_{AIN} V_{AREFx}	SR	-0.5	–	V_{DDM} + 0.5	V	–
Voltage on any Class D analog input pin with respect to V_{SSAF}, if the FADC is switched through to the pin.	V_{AINF} V_{FAREF}	SR	-0.5	–	V_{DDM} + 0.5	V	–

1) Applicable for V_{DD}, V_{DDOSC}, V_{DDPLL}, and V_{DDAF}.

2) Applicable for V_{DDP}, $V_{DDFL3,}$ and V_{DDMF}.

Table 12 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Offset error[9)5)]	EA_{OFF} CC	–	±1.0	±4.0	LSB	12-bit conversion without noise[8)10)]
Input leakage current at analog inputs of ADC0/1 [11) 12) 13)]	I_{OZ1} CC	-300	–	100	nA	(0% V_{DDM}) < V_{IN} < (3% V_{DDM})
		-100	–	200	nA	(3% V_{DDM}) < V_{IN} < (97% V_{DDM})
		-100	–	300	nA	(97% V_{DDM}) < V_{IN} < (100% V_{DDM})
Input leakage current at $V_{AREF0/1}$, per module	I_{OZ2} CC	–	–	±1.5	µA	0 V < V_{AREF} < V_{DDM}, no conversion running
Input current at $V_{AREF0/1}$[14)], per module	I_{AREF} CC	–	35	75	µA rms	0 V < V_{AREF} < V_{DDM}[15)]
Total capacitance of the voltage reference inputs[16)14)]	$C_{AREFTOT}$ CC	–	20	40	pF	8)
Switched capacitance at the positive reference voltage input[14)]	C_{AREFSW} CC	–	15	30	pF	8)17)
Resistance of the reference voltage input path[16)]	R_{AREF} CC	–	500	1000	Ω	500 Ohm increased for AN[1:0] used as reference input[8)]
Total capacitance of the analog inputs[16)]	C_{AINTOT} CC	–	25	30	pF	1)8)

12) Only one of these parameters is tested, the other is verified by design characterization.

13) The leakage current decreases typically 30% for junction temperature decrease of 10°C.

14) Applies to AINx, when used as auxiliary reference inputs.

15) I_{AREF_MAX} is valid for the minimum specified conversion time. The current flowing during an ADC conversion with a duration of up to t_C = 25µs can be calculated with the formula $I_{AREF\_MAX} = Q_{CONV}/t_C$. Every conversion needs a total charge of Q_{CONV} = 150pC from V_{AREF}.
All ADC conversions with a duration longer than t_C = 25µs consume an I_{AREF_MAX} = 6µA.

16) For the definition of the parameters see also **Figure 18**.

17) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this smaller capacitances are successively switched to the reference voltage.

18) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements the voltage measured at AINx can deviate from V_{AREF}/2, and is typically 1.35V.

19) R_{AIN7T} = 1400 Ohm maximum and 830 Ohm typical in the V_{DDM} = 3.3V± 5% range.

20) The DC current at the pin is limited to 3 mA for the operational lifetime.

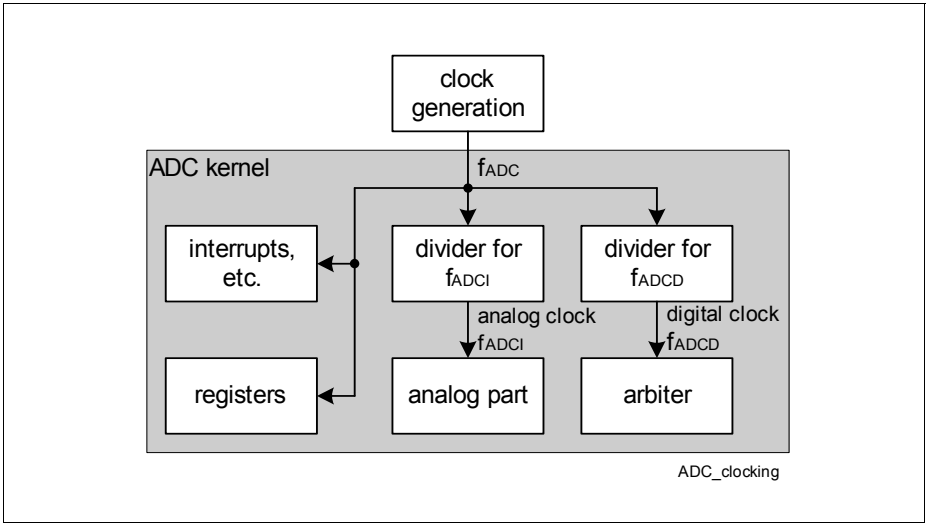

Figure 17 ADC0/ADC1 Clock Circuit

5.3 AC Parameters

All AC parameters are defined with the temperature compensation disabled. That means, keeping the pads constantly at maximum strength.

5.3.1 Testing Waveforms

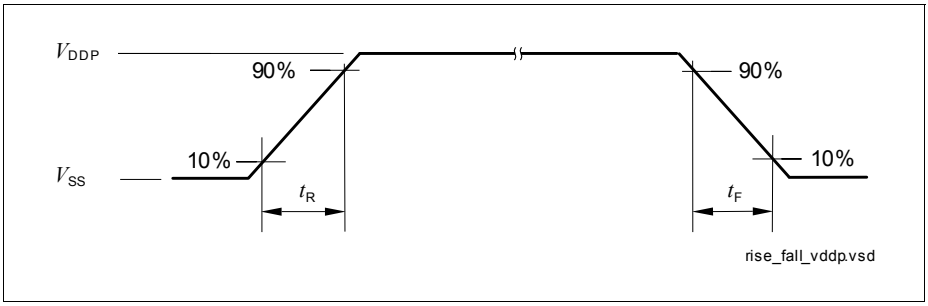

Figure 21 Rise/Fall Time Parameters

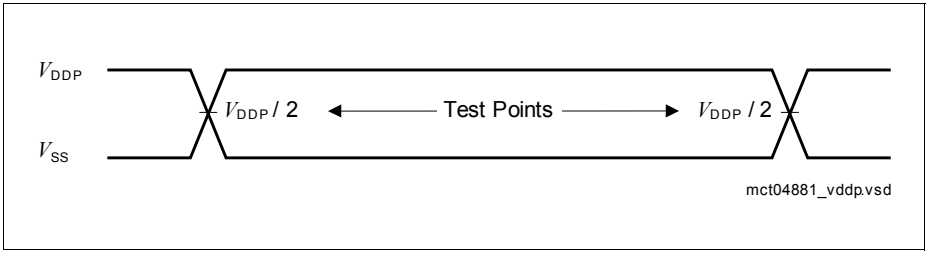

Figure 22 Testing Waveform, Output Delay

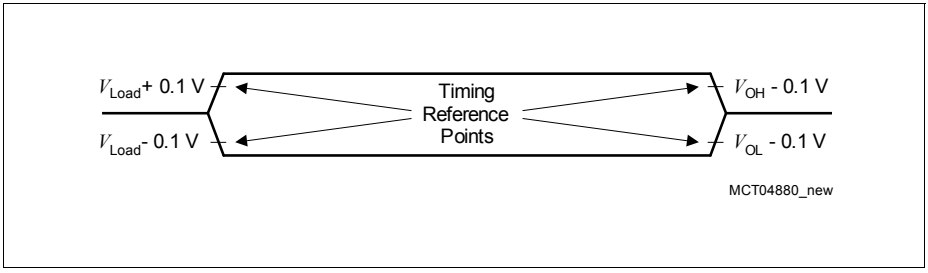

Figure 23 Testing Waveform, Output High Impedance

With rising number m of clock cycles the maximum jitter increases linearly up to a value of m that is defined by the K2-factor of the PLL. Beyond this value of m the maximum accumulated jitter remains at a constant value. Further, a lower LMB-Bus clock frequency f_{LMB} results in a higher absolute maximum jitter value.

Figure 26 gives the jitter curves for several K2 / f_{LMB} combinations.

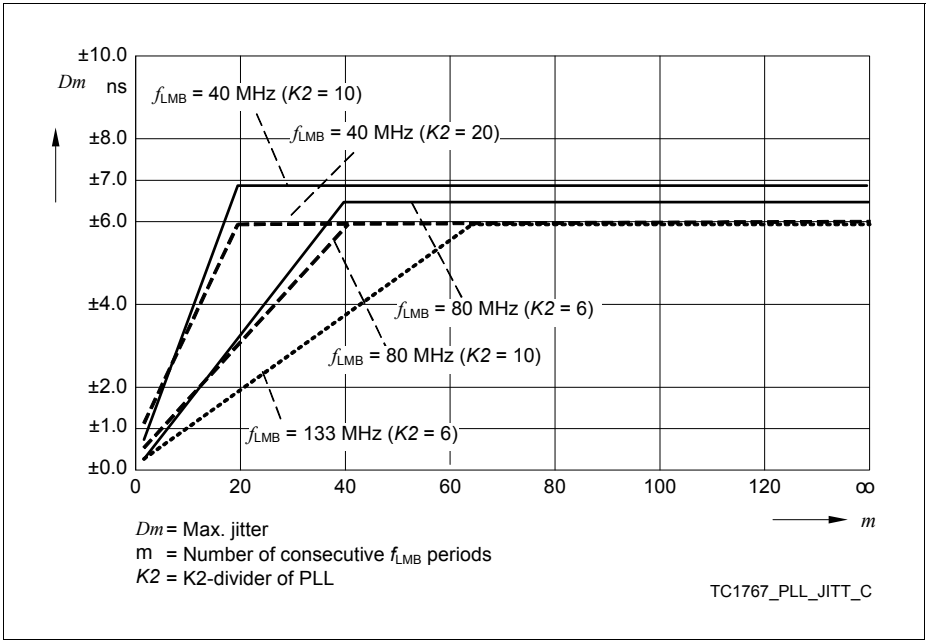

Figure 26 Approximated Maximum Accumulated PLL Jitter for Typical LMB-Bus Clock Frequencies f_{LMB}

Note: The specified PLL jitter values are valid if the capacitive load per output pin does not exceed C_L = 20 pF with the maximum driver and sharp edge. In case of applications with many pins with high loads, driver strengths and toggle rates the specified jitter values could be exceeded.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDOSC3} at pin 106 and V_{SSOSC} at pin 104, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.

The maximum peak-to peak noise on the pad supply votage, measured between V_{DDOSC} at pin 105 and V_{SSOSC} at pin 104, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.

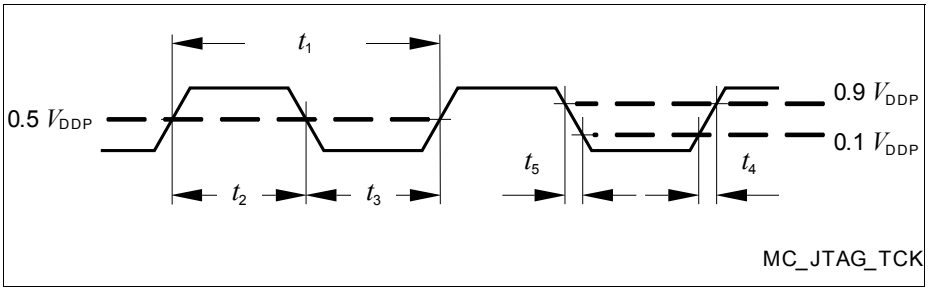

Figure 27 Test Clock Timing (TCK)

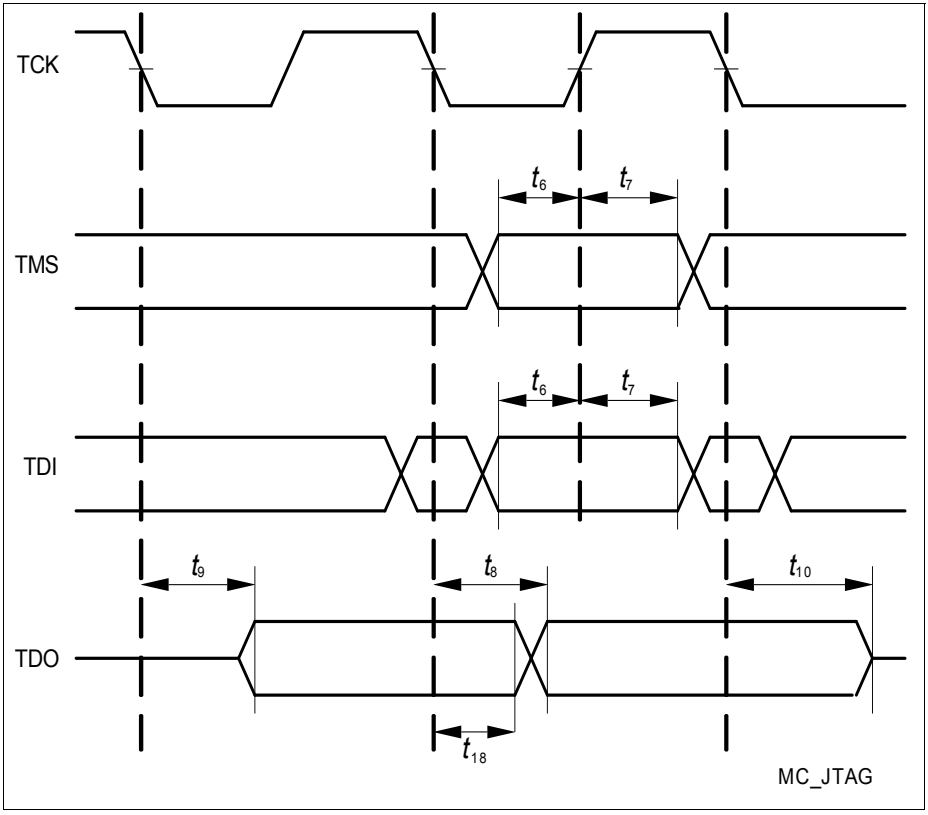

Figure 28 JTAG Timing

5.3.7 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 22 DAP Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	12.5	–	–	ns	–
DAP0 high time	t_{12} SR	4	–	–	ns	–
DAP0 low time	t_{13} SR	4	–	–	ns	–
DAP0 clock rise time	t_{14} SR	–	–	2	ns	–
DAP0 clock fall time	t_{15} SR	–	–	2	ns	–
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	–
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	–
DAP1 valid per DAP0 clock period[1)]	t_{19} SR	8	–	–	ns	80 MHz, C_L = 20 pF
	t_{19} SR	10	–	–	ns	40 MHz, C_L = 50 pF

1) The Host has to find a suitable sampling point by analyzing the sync telegram response.

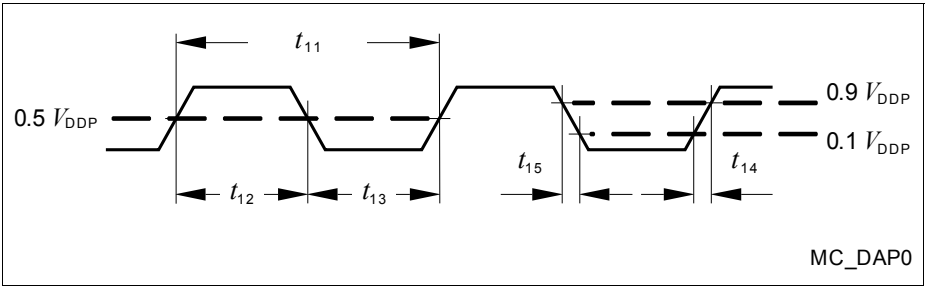

Figure 29 Test Clock Timing (DAP0)

7) The RCLK max. input rise/fall times are best case parameters for f_{SYS} = 80 MHz. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

5.3.8.2 Micro Second Channel (MSC) Interface Timing

Table 24 MSC Interface Timing (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
FCLP clock period[1)2)]	t_{40}	CC	2 × T_{MSC}[3)]	–	–	ns	–
SOP/ENx outputs delay from FCLP rising edge	t_{45}	CC	-10		10	ns	–
SDI bit time	t_{46}	CC	8 × T_{MSC}		–	ns	–
SDI rise time	t_{48}	SR			100	ns	–
SDI fall time	t_{49}	SR			100	ns	–

1) FCLP signal rise/fall times are the same as the A2 Pads rise/fall times.

2) FCLP signal high and low can be minimum 1 × T_{MSC}.

3) T_{MSCmin} = T_{SYS} = 1/f_{SYS}. When f_{SYS} = 80 MHz, t_{40} = 25 ns

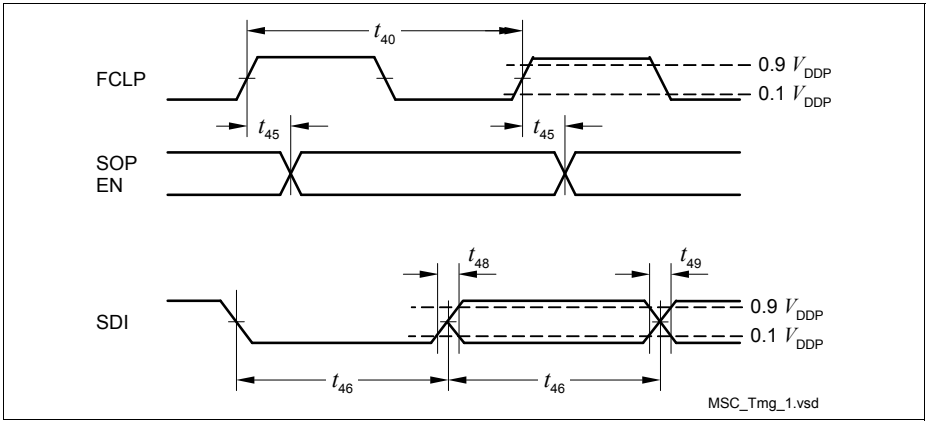

Figure 33 MSC Interface Timing

Note: Sample the data at SOP with the falling edge of FCLP in the target device.

5.3.8.3 SSC Master / Slave Mode Timing