# Infineon Technologies - TC1767256F133HRADKFQMA1 Datasheet

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | TriCore™ |
| Core Size | 32-Bit Single-Core |
| Speed | 133MHz |
| Connectivity | ASC, CANbus, MLI, MSC, SSC |
| Peripherals | DMA, POR, WDT |
| Number of I/O | 88 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.42V ~ 1.58V |
| Data Converters | A/D 4x10b, 32x12b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | PG-LQFP-176-5 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/tc1767256f133hradkfqma1 |

# 2 Introduction

This Data Sheet describes the Infineon TC1767, a 32-bit microcontroller DSP, based on the Infineon TriCore Architecture.

## 2.1 About this Document

This document is designed to be read primarily by design engineers and software engineers who need a detailed description of the interactions of the TC1767 functional units, registers, instructions, and exceptions.

This TC1767 Data Sheet describes the features of the TC1767 with respect to the TriCore Architecture. Where the TC1767 directly implements TriCore architectural functions, this manual simply refers to those functions as features of the TC1767. In all cases where this manual describes a TC1767 feature without referring to the TriCore Architecture, this means that the TC1767 is a direct implementation of the TriCore Architecture.

Where the TC1767 implements a subset of TriCore architectural features, this manual describes the TC1767 implementation, and then describes how it differs from the TriCore Architecture. Such differences between the TC1767 and the TriCore Architecture are documented in the section covering each such subject.

### 2.1.1 Related Documentations

A complete description of the TriCore architecture is found in the document entitled “TriCore Architecture Manual”. The architecture of the TC1767 is described separately this way because of the configurable nature of the TriCore specification: Different versions of the architecture may contain a different mix of systems components. The TriCore architecture, however, remains constant across all derivative designs in order to preserve compatibility.

This Data Sheets together with the “TriCore Architecture Manual” are required to understand the complete TC1767 micro controller functionality.

### 2.1.2 Text Conventions

This document uses the following text conventions for named components of the TC1767:

- Functional units of the TC1767 are given in plain UPPER CASE. For example: “The SSC supports full-duplex and half-duplex synchronous communication”.
- Pins using negative logic are indicated by an overline. For example: “The external reset pin, $\overline{\text{ESR0}}$, has a dual function.”.
- Bit fields and bits in registers are in general referenced as “Module_Register name.Bit field” or “Module_Register name.Bit”. For example: “The Current CPU Priority Number bit field CPU_ICR.CCPN is cleared”. Most of the

## 2.2 System Architecture of the TC1767

The TC1767 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1767 include:

- Program Memory Unit – instruction memory and instruction cache
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

TC1767 clock frequencies:

- Maximum CPU clock frequency: 133 MHz[1)]
- Maximum PCP clock frequency: 133 MHz[2)]
- Maximum SPB frequency: 80 MHz[3)]

The TC1767 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor, a DMA controller and several on-chip peripherals. The TC1767 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1767 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1767, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1767 ports are reserved for these peripheral units to communicate with the external world.

1) For CPU frequencies > 80 MHz, 2:1 mode has to be enabled. CPU 2:1 mode means: $f_{SPB} = 0.5 * f_{CPU}$

2) For PCP frequencies > 80 MHz, 2:1 mode has to be enabled. PCP 2:1 mode means: $f_{SPB} = 0.5 * f_{PCP}$

3) CPU 1:1 Mode means: $f_{SPB} = f_{CPU}$. PCP 1:1 mode means: $f_{SPB} = f_{PCP}$

### 2.3.6 Program Memory Unit (PMU)

The devices of the AudoF family contain at least one Program Memory Unit. This is named “PMU0”. Some devices contain additional PMUs which are named “PMU1”, …

In the TC1767, the PMU0 contains the following submodules:

- The Flash command and fetch control interface for Program Flash and Data Flash.
- The Overlay RAM interface with Online Data Acquisition (OLDA) support.
- The Boot ROM interface.
- The Emulation Memory interface.
- The Local Memory Bus LMB slave interface.

Following memories are controlled by and belong to the PMU0:

- 2 Mbyte of Program Flash memory (PFlash)
- 64 Kbyte of Data Flash memory (DFlash, represents 16 Kbyte EEPROM)
- 16 Kbyte of Boot ROM (BROM)
- 8 Kbyte Overlay RAM (OVRAM)

The following figure shows the block diagram of the PMU0:

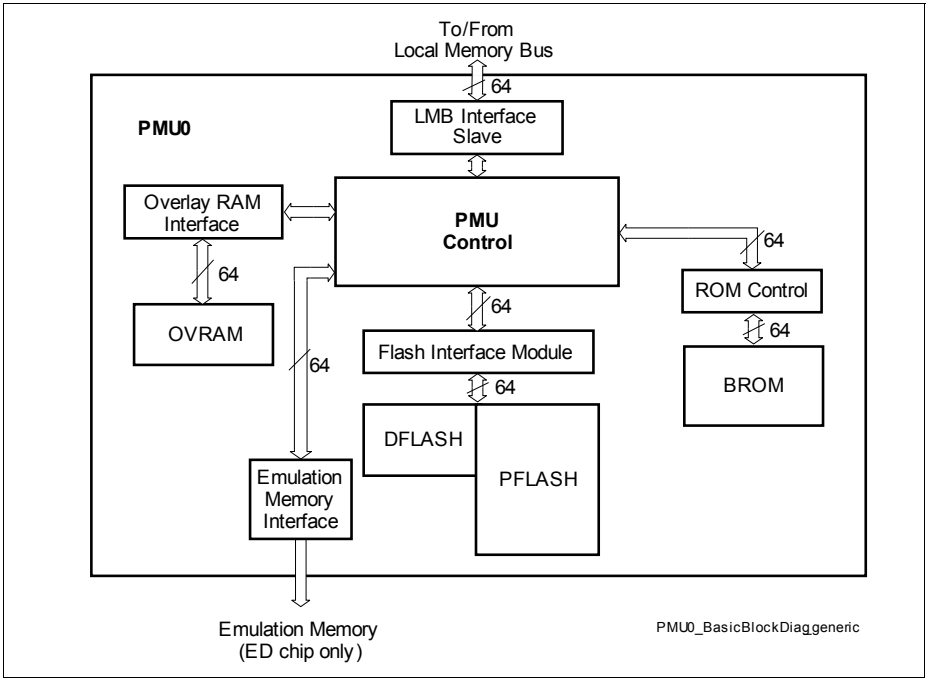


**Figure 3 PMU0 Basic Block Diagram**

### 2.4.4 MultiCAN Controller

The MultiCAN module provides two independent CAN nodes in the PG-LQFP-176-5 package, representing two serial communication interfaces. The number of available message objects is 64.

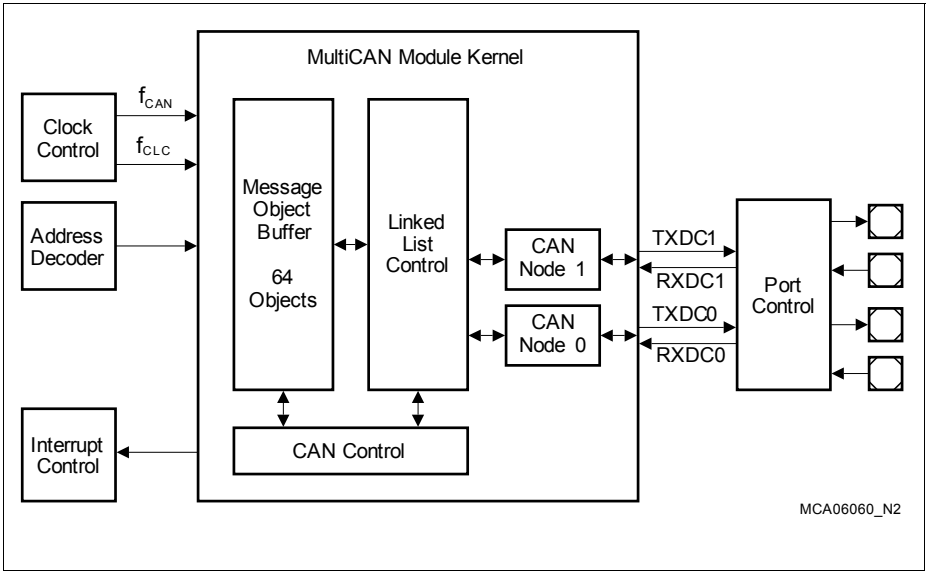


**Figure 8 Overview of the MultiCAN Module**

The MultiCAN module contains two independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All two CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to the message object list of the CAN node, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

  - $f_{GPTA}$/4 maximum input signal frequency in 2-sensor Mode, $f_{GPTA}$/6 maximum input signal frequency in 3-sensor Mode
- Duty Cycle Measurement (DCM)
  - Four independent units
  - 0 - 100% margin and time-out handling
  - $f_{GPTA}$ maximum resolution
  - $f_{GPTA}$/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - $f_{GPTA}$ maximum resolution
  - $f_{GPTA}$/2 maximum input signal frequency
- Clock Distribution Unit (CDU)
  - One unit
  - Provides nine clock output signals: $f_{GPTA}$, divided $f_{GPTA}$ clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

**Signal Generation Unit**

- Global Timers (GT)
  - Two independent units
  - Two operating modes (Free-Running Timer and Reload Timer)
  - 24-bit data width
  - $f_{GPTA}$ maximum resolution
  - $f_{GPTA}$/2 maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 units related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - $f_{GPTA}$ maximum resolution
  - $f_{GPTA}$/2 maximum input signal frequency
- Local Timer Cell (LTC)
  - 64 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - $f_{GPTA}$ maximum resolution
  - $f_{GPTA}$/2 maximum input signal frequency

**Interrupt Sharing Unit**

- 143 interrupt sources, generating up to 46 service requests

### 2.4.7.2 FADC Short Description

**General Features**

- Extreme fast conversion, 21 cycles of $f_{FADC}$ clock (262.5 ns @ $f_{FADC}$ = 80 MHz)
- 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- Successive approximation conversion method
- Each differential input channel can also be used as single-ended input
- Offset calibration support for each channel
- Programmable gain of 1, 2, 4, or 8 for each channel
- Free-running (Channel Timers) or triggered conversion modes
- Trigger and gating control for external signals
- Built-in Channel Timers for internal triggering
- Channel timer request periods independently selectable for each channel
- Selectable, programmable digital anti-aliasing and data reduction filter block with four independent filter units

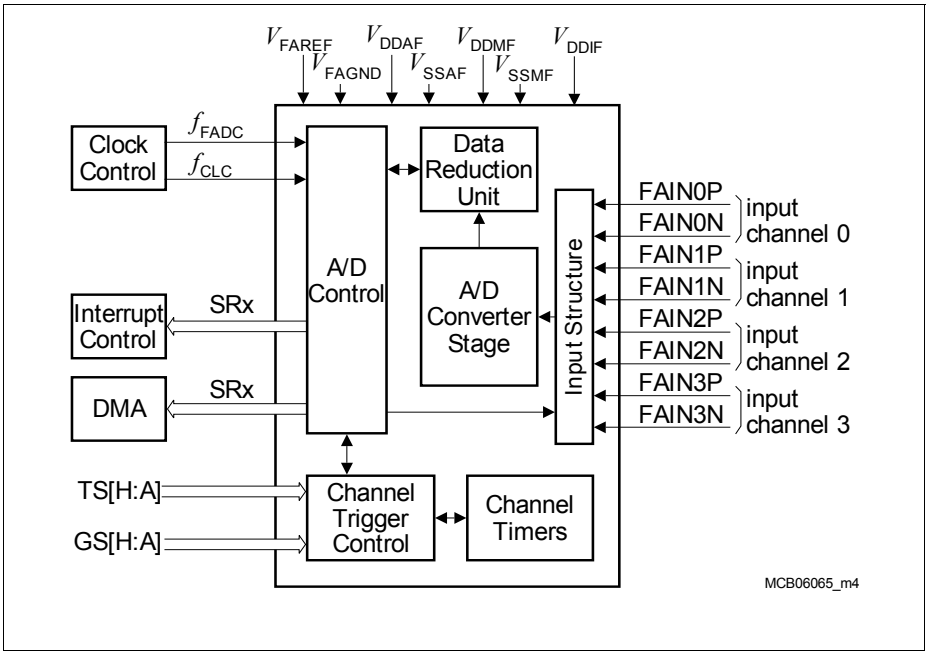


**Figure 13 Block Diagram of the FADC Module with 4 Input Channels**

As shown in **Figure 13**, the main FADC functional blocks are:

- An Input Structure containing the differential inputs and impedance control.

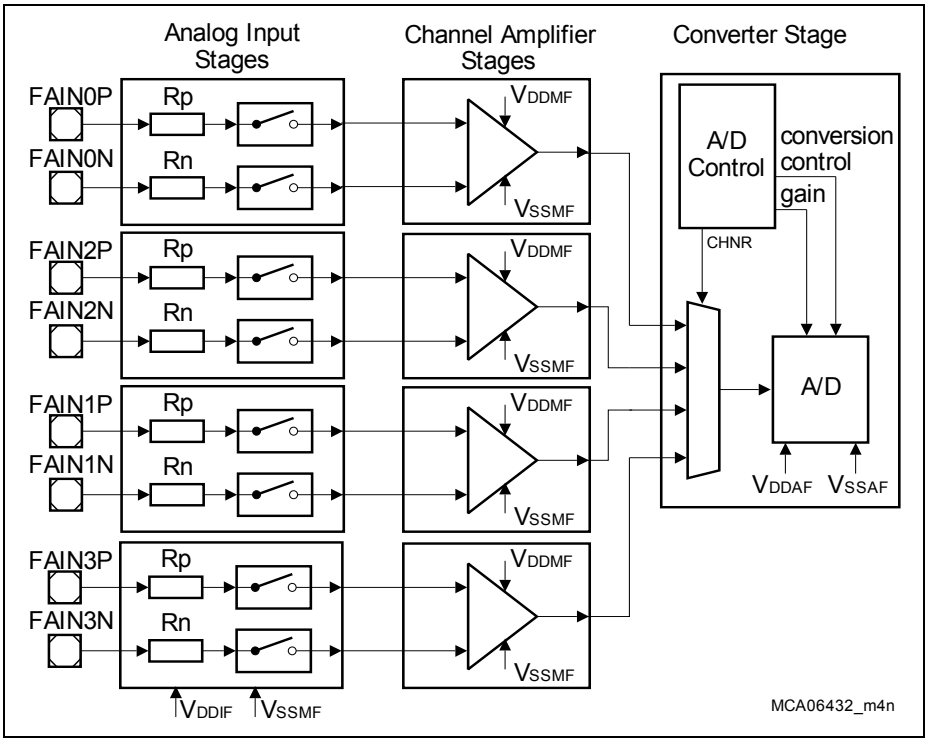


**Figure 14 FADC Input Structure in TC1767**

## 2.5 On-Chip Debug Support (OCDS)

The TC1767 contains resources for different kinds of “debugging”, covering needs from software development to real-time-tuning. These resources are either embedded in specific modules (e.g. breakpoint logic of the TriCore) or part of a central peripheral (known as CERBERUS).

### 2.5.1 On-Chip Debug Support

The classic software debug approach (start/stop, single-stepping) is supported by several features labelled “OCDS Level 1”:

- Run/stop and single-step execution independently for TriCore and PCP.
- Means to request all kinds of reset without usage of sideband pins.
- Halt-after-Reset for repeatable debug sessions.

**Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1])**

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| **Port 0** | | | | |
| 145 | P0.0 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 0** |
| | IN0 | I | | **GPTA0 Input 0** |
| | IN0 | I | | **LTCA2 Input 0** |
| | HWCFG0 | I | | **Hardware Configuration Input 0** |
| | OUT0 | O1 | | **GPTA0 Output 0** |
| | OUT56 | O2 | | **GPTA0 Output 56** |
| | OUT0 | O3 | | **LTCA2 Output 0** |
| 146 | P0.1 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 1** |
| | IN1 | I | | **GPTA0 Input 1** |
| | IN1 | I | | **LTCA2 Input 1** |
| | HWCFG1 | I | | **Hardware Configuration Input 1** |
| | OUT1 | O1 | | **GPTA0 Output 1** |
| | OUT57 | O2 | | **GPTA0 Output 57** |
| | OUT1 | O3 | | **LTCA2 Output 1** |
| 147 | P0.2 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 2** |
| | IN2 | I | | **GPTA0 Input 2** |
| | IN2 | I | | **LTCA2 Input 2** |
| | HWCFG2 | I | | **Hardware Configuration Input 2** |
| | OUT2 | O1 | | **GPTA0 Output 2** |
| | OUT58 | O2 | | **GPTA0 Output 58** |
| | OUT2 | O3 | | **LTCA2 Output 2** |
| 148 | P0.3 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 3** |
| | IN3 | I | | **GPTA0 Input 3** |
| | IN3 | I | | **LTCA2 Input 3** |
| | HWCFG3 | I | | **Hardware Configuration Input 3** |
| | OUT3 | O1 | | **GPTA0 Output 3** |
| | OUT59 | O2 | | **GPTA0 Output 59** |
| | OUT3 | O3 | | **LTCA2 Output 3** |

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 97 | P1.11 | I/O0 | A2/ PU | **Port 1 General Purpose I/O Line 11** |
| | IN27 | I | | **GPTA0 Input 27** |
| | IN51 | I | | **GPTA0 Input 51** |
| | SCLK1B | I | | **SSC1 Clock Input B** |
| | OUT27 | O1 | | **GPTA0 Output 27** |
| | OUT51 | O2 | | **GPTA0 Output 51** |
| | SCLK1B | O3 | | **SSC1 Clock Output B** |
| 73 | P1.12 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 12** |
| | IN16 | I | | **LTCA2 Input 16** |
| | AD0EMUX0 | O1 | | **ADC0 External Multiplexer Control Output 0** |
| | AD0EMUX0 | O2 | | **ADC0 External Multiplexer Control Output 0** |
| | OUT16 | O3 | | **LTCA2 Output 16** |
| 72 | P1.13 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 13** |
| | IN17 | I | | **LTCA2 Input 17** |
| | AD0EMUX1 | O1 | | **ADC0 External Multiplexer Control Output 1** |
| | AD0EMUX1 | O2 | | **ADC0 External Multiplexer Control Output 1** |
| | OUT17 | O3 | | **LTCA2 Output 17** |
| 71 | P1.14 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 14** |
| | IN18 | I | | **LTCA2 Input 18** |
| | AD0EMUX2 | O1 | | **ADC0 External Multiplexer Control Output 2** |
| | AD0EMUX2 | O2 | | **ADC0 External Multiplexer Control Output 2** |
| | OUT18 | O3 | | **LTCA2 Output 18** |
| 117 | P1.15 | I/O0 | A2/ PU | **Port 1 General Purpose I/O Line 15** |
| | $\overline{\text{BRKIN}}$ | I | | **Break Input** |
| | Reserved | O1 | | **-** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| | $\overline{\text{BRKOUT}}$ | O | | **Break Output (controlled by OCDS module)** |

**Port 2**

**Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)**

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 74 | P2.0 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 0** |
| | IN32 | I | | **GPTA0 Input 32** |
| | OUT32 | O1 | | **GPTA0 Output 32** |
| | TCLK0 | O2 | | **MLI0 Transmitter Clock Output 0** |
| | OUT28 | O3 | | **LTCA2 Output 28** |
| 75 | P2.1 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 1** |
| | IN33 | I | | **GPTA0 Input 33** |
| | TREADY0A | I | | **MLI0 Transmitter Ready Input A** |
| | OUT33 | O1 | | **GPTA0 Output 33** |
| | SLSO03 | O2 | | **SSC0 Slave Select Output Line 3** |
| | SLSO13 | O3 | | **SSC1 Slave Select Output Line 3** |
| 76 | P2.2 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 2** |
| | IN34 | I | | **GPTA0 Input 34** |
| | OUT34 | O1 | | **GPTA0 Output 34** |
| | TVALID0 | O2 | | **MLI0 Transmitter Valid Output** |
| | OUT29 | O3 | | **LTCA2 Output 29** |
| 77 | P2.3 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 3** |
| | IN35 | I | | **GPTA0 Input 35** |
| | OUT35 | O1 | | **GPTA0 Output 35** |
| | TDATA0 | O2 | | **MLI0 Transmitter Data Output** |
| | OUT30 | O3 | | **LTCA2 Output 30** |
| 78 | P2.4 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 4** |
| | IN36 | I | | **GPTA0 Input 36** |
| | RCLK0A | I | | **MLI Receiver Clock Input A** |
| | OUT36 | O1 | | **GPTA0 Output 36** |
| | OUT36 | O2 | | **GPTA0 Output 36** |
| | OUT31 | O3 | | **LTCA2 Output 31** |

### 5.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1767. All parameters specified in the following table refer to these operating conditions, unless otherwise noted.

**Table 9 Operating Condition Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Digital supply voltage[1] | $V_{DD}$ SR<br>$V_{DDOSC}$ SR | 1.42 | – | 1.58[2] | V | – |
| | $V_{DDP}$ SR<br>$V_{DDOSC3}$ SR | 3.13 | – | 3.47[3] | V | For Class A pins (3.3 V ± 5%) |
| | $V_{DDFL3}$ SR | 3.13 | – | 3.47[3] | V | – |
| Analog supply voltages | $V_{DDMF}$ SR | 3.13 | – | 3.47[3] | V | FADC |
| | $V_{DDAF}$ SR | 1.42 | – | 1.58[2] | V | FADC |
| | $V_{DDM}$ SR | 4.75 | – | 5.25 | V | For Class $D_E$ pins, ADC |
| Digital ground voltage | $V_{SS}$ SR | 0 | – | – | V | – |
| Ambient temperature under bias | $T_A$ SR | – | -40 | 125 | °C | – |
| Analog supply voltages | – | – | – | – | – | See separate specification Page 88, Page 93 |
| Overload current at class D pins | $I_{OV}$ | -1 | – | 3 | mA | [4] |
| Sum of overload current at class D pins | $\Sigma\|I_{OV}\|$ | – | – | 10 | mA | per single ADC |
| Overload coupling factor for analog inputs[5] | $K_{OVAP}$ | – | – | $5\times10^{-5}$ | | $0 < I_{OV} < 3$ mA |
| | $K_{OVAN}$ | – | – | $5\times10^{-4}$ | | $-1$ mA $< I_{OV} < 0$ |
| CPU & LMB Bus Frequency | $f_{CPU}$ SR | – | – | 133<br>80 | MHz | Derivative dependent |
| PCP Frequency | $f_{PCP}$ SR | – | – | 133<br>80 | MHz | [6]Derivative dependent |
| FPI Bus Frequency | $f_{SYS}$ SR | – | – | 80 | MHz | [6] |
| Short circuit current | $I_{SC}$ SR | -5 | – | +5 | mA | [7] |

## 5.2 DC Parameters

### 5.2.1 Input/Output Pins

**Table 11 Input/Output DC-Characteristics** (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **General Parameters** | | | | | | |
| Pull-up current[1] | $\lvert I_{PUH}\rvert$ CC | 10 | – | 100 | µA | $V_{IN} < V_{IHAmin}$; class A1/A2/F/Input pads. |
| Pull-down current[1] | $\lvert I_{PDL}\rvert$ CC | 10 | – | 150 | µA | $V_{IN} > V_{ILAmax}$; class A1/A2/F/Input pads. |
| Pin capacitance[1] (Digital I/O) | $C_{IO}$ CC | – | – | 10 | pF | $f$ = 1 MHz $T_A$ = 25 °C |
| **Input only Pads ($V_{DDP}$ = 3.13 to 3.47 V = 3.3 V ± 5%)** | | | | | | |
| Input low voltage | $V_{ILI}$ SR | -0.3 | – | 0.36 × $V_{DDP}$ | V | – |
| Input high voltage | $V_{IHI}$ SR | 0.62 × $V_{DDP}$ | – | $V_{DDP}$+ 0.3 or max. 3.6 | V | Whatever is lower |
| Ratio $V_{IL}/V_{IH}$ | CC | 0.58 | – | – | – | – |
| Input high voltage $\overline{TRST}$, TCK | $V_{IHJ}$ SR | 0.64 × $V_{DDP}$ | – | $V_{DDP}$+ 0.3 or max. 3.6 | V | Whatever is lower |
| Input hysteresis | HYSI CC | 0.1 × $V_{DDP}$ | – | – | V | [4] |
| Input leakage current[2] | $I_{OZI}$ CC | – | – | ±3000 ±6000 | nA | (($V_{DDP}$/2)-1) < $V_{IN}$ < (($V_{DDP}$/2)+1) Otherwise |
| Spike filter always blocked pulse duration | $t_{SF1}$ CC | – | – | 10 | ns | |

### 5.2.2 Analog to Digital Converters (ADC0/ADC1)

All ADC parameters are optimized for and valid in the range of $V_{DDM}$ = 5V ± 5%.

**Table 12 ADC Characteristics** (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Analog supply voltage | $V_{DDM}$ | SR | 4.75 | 5 | 5.25 | V | – |
| | | | 3.13 | 3.3 | 3.47[1)] | V | – |
| | $V_{DD}$ | SR | 1.42 | 1.5 | 1.58[2)] | V | Power supply for ADC digital part, internal supply |
| Analog ground voltage | $V_{SSM}$ | SR | -0.1 | – | 0.1 | V | – |
| Analog reference voltage[14)] | $V_{AREFx}$ | SR | $V_{AGNDx}$+1 V | $V_{DDM}$ | $V_{DDM}$+ 0.05 [1)3)4)] | V | – |
| Analog reference ground[14)] | $V_{AGNDx}$ | SR | $V_{SSMx}$ - 0.05V | 0 | $V_{AREF}$ - 1V | V | – |
| Analog input voltage range | $V_{AIN}$ | SR | $V_{AGNDx}$ | – | $V_{AREFx}$ | V | – |
| Analog reference voltage range[5)14)] | $V_{AREFx}$- $V_{AGNDx}$ | SR | $V_{DDM}$/2 | – | $V_{DDM}$ + 0.05 | V | – |
| Converter Clock | $f_{ADC}$ | SR | 1 | – | 80 | MHz | – |
| Internal ADC clocks | $f_{ADCI}$ | CC | 0.5 | – | 10 | MHz | – |
| Sample time | $t_S$ | CC | 2 | – | 257 | $T_{ADCI}$ | – |
| Total unadjusted error[5)] | TUE[6)] | CC | – | – | ±4 | LSB | 12-bit conversion, without noise[7)8)] |
| | | | – | – | ±2 | LSB | 10-bit conversion[8)] |
| | | | – | – | ±1 | LSB | 8-bit conversion[8)] |
| DNL error[9) 5)] | $EA_{DNL}$ | CC | – | ±1.5 | ±3.0 | LSB | 12-bit conversion without noise[8)10)] |
| INL error[9)5)] | $EA_{INL}$ | CC | – | ±1.5 | ±3.0 | LSB | 12-bit conversion without noise[8)10)] |
| Gain error[9)5)] | $EA_{GAIN}$ | CC | – | ±0.5 | ±3.5 | LSB | 12-bit conversion without noise[8)10)] |

### 5.2.6 Power Supply Current

The default test conditions (differences explicitly specified) are:
$V_{DD}$ = 1.58 V, $V_{DDP}$ = 3.47 V, $T_j$=150°C. All other operating conditions apply.

**Table 17 Power Supply Currents, Maximum Power Consumption**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Core active mode supply current [1) 2)] | $I_{DD}$ | CC | – | – | 330 | mA | $f_{CPU}$=133 MHz $f_{CPU}/f_{SYS}$ = 2:1 |
| Realistic core active mode supply current [3)4)] | | | – | – | 230 | mA | $V_{DD}$ = 1.53 V, $T_J$ = 150°C |
| FADC 3.3 V analog supply current | $I_{DDMF}$ | CC | – | – | 10 | mA | – |
| FADC 1.5 V analog supply current | $I_{DDAF}$ | CC | – | – | 10 | mA | – [4)] |
| Flash memory 3.3 V supply current | $I_{DDFL3R}$ | CC | – | – | 60 | mA | continuously reading the Flash memory [5)] |
| | $I_{DDFL3E}$ | CC | – | – | 61 | mA | Flash memory erase-verify[6)] |
| Oscillator 1.5 V supply | $I_{DDOSC}$ | CC | – | – | 3 | mA | – [4)] |
| Oscillator 3.3 V supply | $I_{DDOSC3}$ | CC | – | – | 10 | mA | – [4)] |
| LVDS 3.3 V supply | $I_{LVDS}$ | | – | – | 15 | mA | in total for two pairs |
| Pad currents,sum of $V_{DDP}$ 3.3 V supplies | $I_{DDP}$ | CC | – | – | 16 | mA | – [4) 7)] |
| | $I_{DDP\_FP}$ | CC | – | – | 34 | mA | $I_{DDP}$ including Data Flash programming current [4) 8)] |
| ADC 5 V power supply | $I_{DDM}$ | CC | – | 2 | 3 | mA | ADC0 / 1 |
| Maximum Average Power Dissipation[1)] | $P_D$ | SR | – | 820 | 990 | mW | worst case $T_A$ = 125°C, $P_D \times R_{\Theta JA}$ < 25°C |

1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each custom application will most probably be lower than this value, but must be evaluated separately..

2) The $I_{DD}$ maximum value is 275 mA at $f_{CPU}$ = 80 MHz, constant $T_J$ = 150°C, for the Infineon Max Power Loop. The dependency in this range is, at constant junction temperature, linear.
$f_{CPU}/f_{SYS}$ = 1:1 mode.

### 5.3.2 Output Rise/Fall Times

**Table 18 Output Rise/Fall Times** (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Class A1 Pads** | | | | | | |
| Rise/fall times[1)] | $t_{RA1}$, $t_{FA1}$ | – | – | 50 | ns | Regular (medium) driver, 50 pF |
| | | | | 140 | | Regular (medium) driver, 150 pF |
| | | | | 18000 | | Regular (medium) driver, 20 nF |
| | | | | 150 | | Weak driver, 20 pF |
| | | | | 550 | | Weak driver, 150 pF |
| | | | | 65000 | | Weak driver, 20 000 pF |
| **Class A2 Pads** | | | | | | |
| Rise/fall times [1)] | $t_{RA2}$, $t_{FA2}$ | – | – | 3.7 | ns | Strong driver, sharp edge, 50 pF |
| | | | | 7.5 | | Strong driver, sharp edge, 100pF |
| | | | | 7 | | Strong driver, med. edge, 50 pF |
| | | | | 18 | | Strong driver, soft edge, 50 pF |
| | | | | 50 | | Medium driver, 50 pF |
| | | | | 140 | | Medium driver, 150 pF |
| | | | | 18000 | | Medium driver, 20 000 pF |
| | | | | 150 | | Weak driver, 20 pF |
| | | | | 550 | | Weak driver, 150 pF |
| | | | | 65000 | | Weak driver, 20 000 pF |
| **Class F Pads** | | | | | | |
| Rise/fall times | $t_{RF1}$, $t_{FF1}$ | – | – | 2 | ns | LVDS Mode |
| Rise/fall times | $t_{RF2}$, $t_{FF2}$ | – | – | 60 | ns | CMOS Mode, 50 pF |

1) Not all parameters are subject to production test, but verified by design/characterization and test correlation.

### 5.3.3 Power Sequencing

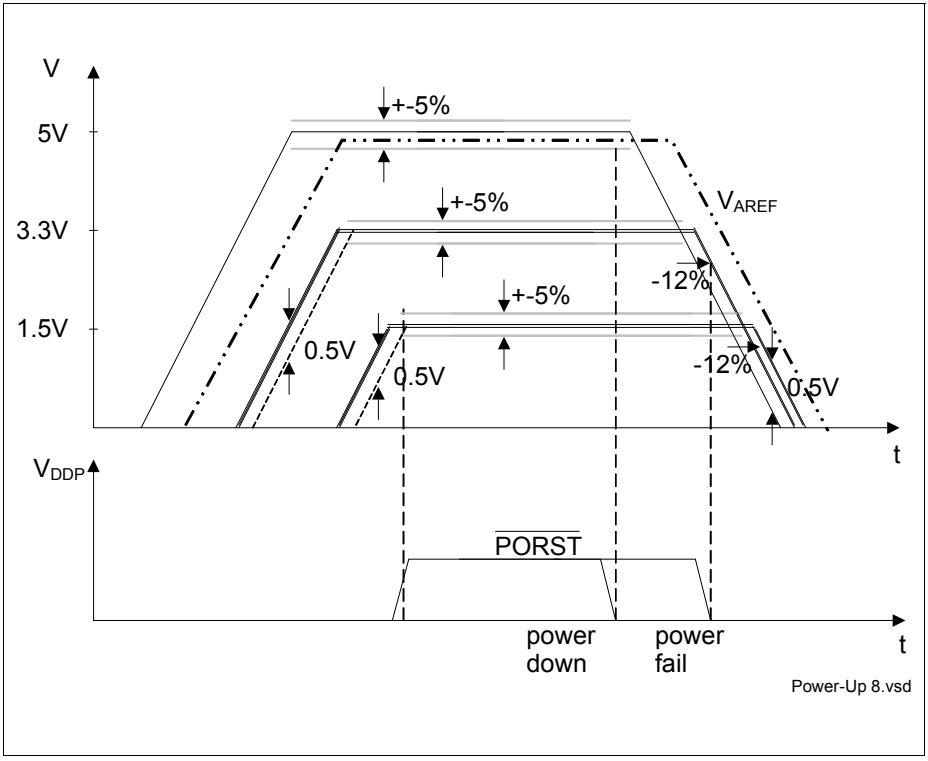


**Figure 24 5 V / 3.3 V / 1.5 V Power-Up/Down Sequence**

The following list of rules applies to the power-up/down sequence:

- All ground pins $V_{SS}$ must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.

1. At any moment,
   each power supply must be higher than any lower_power_supply - 0.5 V, or:
   $V_{DD5} > V_{DD3.3} - 0.5$ V; $V_{DD5} > V_{DD1.5} - 0.5$ V; $V_{DD3.3} > V_{DD1.5} - 0.5$ V, see **Figure 24**.
2. During power-up and power-down, the voltage difference between the power supply pins of the same voltage (3.3 V, 1.5 V, and 5 V) with different names (for example $V_{DDP}$, $V_{DDFL3}$ ...), that are internaly connected via diodes must be lower than 100 mV. On the other hand, all power supply pins with the same name (for example all $V_{DDP}$ ), are internaly directly connected. It is recommended that the power pins of the same voltage are driven by a single power supply.

With rising number $m$ of clock cycles the maximum jitter increases linearly up to a value of $m$ that is defined by the K2-factor of the PLL. Beyond this value of $m$ the maximum accumulated jitter remains at a constant value. Further, a lower LMB-Bus clock frequency $f_{LMB}$ results in a higher absolute maximum jitter value.

**Figure 26** gives the jitter curves for several K2 / $f_{LMB}$ combinations.

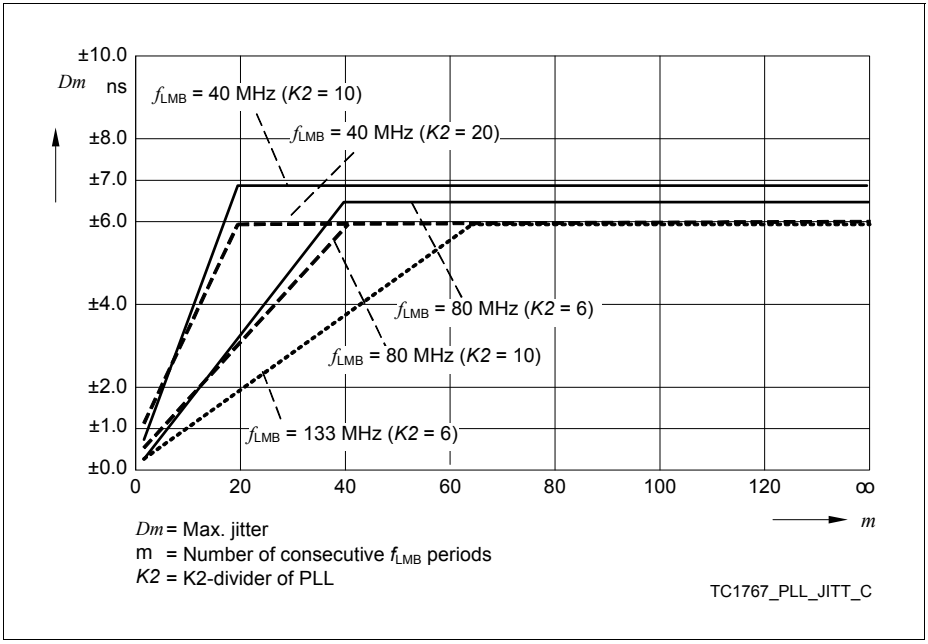


**Figure 26 Approximated Maximum Accumulated PLL Jitter for Typical LMB-Bus Clock Frequencies $f_{LMB}$**

*Note: The specified PLL jitter values are valid if the capacitive load per output pin does not exceed $C_L$ = 20 pF with the maximum driver and sharp edge. In case of applications with many pins with high loads, driver strengths and toggle rates the specified jitter values could be exceeded.*

*Note: The maximum peak-to-peak noise on the pad supply voltage, measured between $V_{DDOSC3}$ at pin 106 and $V_{SSOSC}$ at pin 104, is limited to a peak-to-peak voltage of $V_{PP}$ = 100 mV for noise frequencies below 300 KHz and $V_{PP}$ = 40 mV for noise frequencies above 300 KHz.*

*The maximum peak-to peak noise on the pad supply votage, measured between $V_{DDOSC}$ at pin 105 and $V_{SSOSC}$ at pin 104, is limited to a peak-to-peak voltage of $V_{PP}$ = 100 mV for noise frequencies below 300 KHz and $V_{PP}$ = 40 mV for noise frequencies above 300 KHz.*

**Table 23 MLI Transmitter/Receiver Timing**
(Operating Conditions apply), $C_L$ = 50 pF

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| **MLI Transmitter Timing** | | | | | | | |
| TCLK clock period | $t_{10}$ | CC | $2 \times T_{MLI}$ | – | – | ns | 1) |
| TCLK high time | $t_{11}$ | CC | $0.45 \times t_{10}$ | $0.5 \times t_{10}$ | $0.55 \times t_{10}$ | ns | 2)3) |
| TCLK low time | $t_{12}$ | CC | $0.45 \times t_{10}$ | $0.5 \times t_{10}$ | $0.55 \times t_{10}$ | ns | 2)3) |
| TCLK rise time | $t_{13}$ | CC | – | – | 4) | ns | – |
| TCLK fall time | $t_{14}$ | CC | – | – | 4) | ns | – |
| TDATA/TVALID output delay time | $t_{15}$ | CC | -3 | – | 4.4 | ns | – |
| TREADY setup time to TCLK rising edge | $t_{16}$ | SR | 18 | – | – | ns | – |
| TREADY hold time from TCLK rising edge | $t_{17}$ | SR | 0 | – | – | ns | – |
| **MLI Receiver Timing** | | | | | | | |
| RCLK clock period | $t_{20}$ | SR | $1 \times T_{MLI}$ | – | – | ns | 1) |
| RCLK high time | $t_{21}$ | SR | – | $0.5 \times t_{20}$ | – | ns | 5)6) |
| RCLK low time | $t_{22}$ | SR | – | $0.5 \times t_{20}$ | – | ns | 5)6) |
| RCLK rise time | $t_{23}$ | SR | – | – | 4 | ns | 7) |
| RCLK fall time | $t_{24}$ | SR | – | – | 4 | ns | 7) |
| RDATA/RVALID setup time to RCLK falling edge | $t_{25}$ | SR | 4.2 | – | – | ns | – |
| RDATA/RVALID hold time from RCLK rising edge | $t_{26}$ | SR | 2.2 | – | – | ns | – |
| RREADY output delay time | $t_{27}$ | CC | 0 | – | 16 | ns | – |

1) $T_{MLImin.} = T_{SYS} = 1/f_{SYS}$. When $f_{SYS}$ = 80 MHz, $t_{10}$ = 25 ns and $t_{20}$ = 12.5 ns.

2) The following formula is valid: $t_{11} + t_{12} = t_{10}$

3) The min./max. TCLK low/high times $t_{11}/t_{12}$ include the PLL jitter of $f_{SYS}$. Fractional divider settings must be regarded additionally to $t_{11}/t_{12}$.

4) For high-speed MLI interface, strong driver sharp edge selection (class A2 pad) is recommended for TCLK.

5) The following formula is valid: $t_{21} + t_{22} = t_{20}$

6) The min. and max. value of is parameter can be adjusted by considering the other receiver timing parameters.

## 5.4 Package and Reliability

### 5.4.1 Package Parameters

**Table 26 Thermal Parameters** (Operating Conditions apply)

| Device | Package | $R_{\Theta JCT}$ 1) | $R_{\Theta JCB}$ 1) | $R_{\Theta JLeads}$ 1) | Unit | Note |
|---|---|---|---|---|---|---|
| TC1767 | PG-LQFP-176-5 | 6.5 | 5.5 | 23 | K/W | |

1) The top and bottom thermal resistances between the case and the ambient ($R_{TCAT}$, $R_{TCAB}$) are to be combined with the thermal resistances between the junction and the case given above ($R_{TJCT}$, $R_{TJCB}$), in order to calculate the total thermal resistance between the junction and the ambient ($R_{TJA}$). The thermal resistances between the case and the ambient ($R_{TCAT}$, $R_{TCAB}$) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the $R_{TJA}$ is the total thermal resistance between the junction and the ambient. This total junction ambient resistance $R_{TJA}$ can be obtained from the upper four partial thermal resistances.
Thermal resistances as measured by the ‘cold plate method’ (MIL SPEC-883 Method 1012.1).

### 5.4.4 Quality Declarations

**Table 28 Quality Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operation Lifetime[1] | $t_{OP}$ | – | – | 24000 | hours | –[2) 3)] |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ | – | – | 2000 | V | Conforming to JESD22-A114-B |
| ESD susceptibility of the LVDS pins | $V_{HBM1}$ | – | – | 500 | V | – |
| ESD susceptibility according to Charged Device Model (CDM) | $V_{CDM}$ | – | – | 500 | V | Conforming to JESD22-C101-C |
| Moisture Sensitivity Level | MSL | – | – | 3 | – | Conforming to Jedec J-STD-020C for 240°C |

1) This lifetime refers only to the time when the device is powered on.

2) For worst-case temperature profile equivalent to:
2000 hours at $T_j$ = 150°C
16000 hours at $T_j$ = 125°C
6000 hours at $T_j$ = 110°C

3) This 30000 hours worst-case temperature profile is also covered:
300 hours at $T_j$ = 150°C
1000 hours at $T_j$ = 140°C
1700 hours at $T_j$ = 130°C
24000 hours at $T_j$ = 120°C
3000 hours at $T_j$ = 110°C