Infineon Technologies - TC1767256F133HRADKXUMA1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	133MHz
Connectivity	ASC, CANbus, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	88
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 4x10b, 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1767256f133hradkxuma1

1 Summary of Features

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 133 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 8 Kbyte Parameter Memory (PRAM)
  - 16 Kbyte Code Memory (CMEM)
  - 133 MHz operation at full temperature range
- Multiple on-chip memories
  - 72 Kbyte Data Memory (LDRAM)
  - 24 Kbyte Code Scratchpad Memory (SPRAM)
  - 2 Mbyte Program Flash Memory (PFlash)
  - 64 Kbyte Data Flash Memory (DFlash, represents 16 Kbyte EEPROM)
  - Instruction Cache: up to 8 Kbyte (ICACHE, configurable)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 8-Channel DMA Controller
- Sophisticated interrupt system with 2 × 255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Two High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 2 CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - One General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 32 analog input lines for ADC

2.1.3 Reserved, Undefined, and Unimplemented Terminology

In tables where register bit fields are defined, the following conventions are used to indicate undefined and unimplemented function. Furthermore, types of bits and bit fields are defined using the abbreviations as shown in **Table 2**.

Table 2 Bit Function Terminology

Function of Bits	Description
Unimplemented, Reserved	Register bit fields named **0** indicate unimplemented functions with the following behavior. • Reading these bit fields returns 0. • These bit fields should be written with 0 if the bit field is defined as r or rh. • These bit fields have to be written with 0 if the bit field is defined as rw. These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.
rw	The bit or bit field can be read and written.
rwh	As rw, but bit or bit field can be also set or reset by hardware.
r	The bit or bit field can only be read (read-only).
w	The bit or bit field can only be written (write-only). A read to this register will always give a default value back.
rh	This bit or bit field can be modified by hardware (read-hardware, typical example: status flags). A read of this bit or bit field give the actual status of this bit or bit field back. Writing to this bit or bit field has no effect to the setting of this bit or bit field.
s	Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten by software, they can be switched again into their reset state only by a reset operation. Software cannot switch this type of bit into its reset state by writing the register. This attribute can be combined to “rws” or “rwhs”.
f	Bits with this attribute are readable only when they are accessed by an instruction fetch. Normal data read operations will return other values.

2.1.4 Register Access Modes

Read and write access to registers and memory locations are sometimes restricted. In memory and register access tables, the terms as defined in **Table 3** are used.

  - 72 Kbyte Local Data RAM (LDRAM)
  - 0 Kbyte Data Cache (DACHE)
- On-chip SRAMs with parity error detection

2.2.3.2 High-performance 32-bit Peripheral Control Processor

The PCP is a flexible Peripheral Control Processor optimized for interrupt handling and thus unloading the CPU.

Features

- Data move between any two memory or I/O locations
- Data move with predefined limit supported
- Read-Modify-Write capabilities
- Full computation capabilities including basic MUL/DIV
- Read/move data and accumulate it to previously read data
- Read two data values and perform arithmetic or logical operation and store result
- Bit-handling capabilities (testing, setting, clearing)
- Flow control instructions (conditional/unconditional jumps, breakpoint)
- Dedicated Interrupt System
- PCP SRAMs with parity error detection
- PCP/FPI clock mode 1:1 and 2:1 available

Integrated PCP related On-Chip Memories

- 16 Kbyte Code Memory (CMEM)
- 8 Kbyte Parameter Memory (PRAM)
-

2.3 On Chip System Units

The TC1767 micro controller offers several versatile on-chip system peripheral units such as DMA controller, embedded Flash module, interrupt system and ports.

2.3.1 Flexible Interrupt System

The TC1767 includes a programmable interrupt system with the following features:

Features

- Fast interrupt response
- Hardware arbitration
- Independent interrupt systems for CPU and PCP
- Programmable service request nodes (SRNs)
- Each SRN can be mapped to the CPU or PCPinterrupt system

2.3.3 System Timer

The TC1767's STM is designed for global system timing applications requiring both high precision and long range.

Features

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible interrupt generation based on compare match with partial STM content
- Driven by maximum 80 MHz (= f_{SYS}, default after reset = $f_{SYS}/2$)
- Counting starts automatically after a reset operation
- STM registers are reset by an application reset if bit ARSTDIS.STMDIS is cleared. If bit ARSTDIS.STMDIS is set, the STM is not reset.
- STM can be halted in debug/suspend mode

Special STM register semantics provide synchronous views of the entire 56-bit counter, or 32-bit subsets at different levels of resolution.

The maximum clock period is $2^{56} \times f_{STM}$. At f_{STM} = 80 MHz, for example, the STM counts 28.56 years before overflowing. Thus, it is capable of continuously timing the entire expected product life time of a system without overflowing.

In case of a power-on reset, a watchdog reset, or a software reset, the STM is reset. After one of these reset conditions, the STM is enabled and immediately starts counting up. It is not possible to affect the content of the timer during normal operation of the TC1767. The timer registers can only be read but not written to.

The STM can be optionally disabled for power-saving purposes, or suspended for debugging purposes via its clock control register. In suspend mode of the TC1767 (initiated by writing an appropriate value to STM_CLC register), the STM clock is stopped but all registers are still readable.

Due to the 56-bit width of the STM, it is not possible to read its entire content with one instruction. It needs to be read with two load instructions. Since the timer would continue to count between the two load operations, there is a chance that the two values read are not consistent (due to possible overflow from the low part of the timer to the high part between the two read operations). To enable a synchronous and consistent reading of the STM content, a capture register (STM_CAP) is implemented. It latches the content of the high part of the STM each time when one of the registers STM_TIM0 to STM_TIM5 is read. Thus, STM_CAP holds the upper value of the timer at exactly the same time when the lower part is read. The second read operation would then read the content of the STM_CAP to get the complete timer value.

The content of the 56-bit System Timer can be compared against the content of two compare values stored in the STM_CMP0 and STM_CMP1 registers. Interrupts can be

- Trigger sources that do not depend on a clock, such as the $\overline{\text{PORST}}$. This trigger force the device into an asynchronous reset assertion independently of any clock. The activation of an asynchronous reset is asynchronous to the system clock, whereas its de-assertion is synchronized.
- Trigger sources that need a clock in order to be asserted, such as the input signals $\overline{\text{ESR0}}$, and $\overline{\text{ESR1}}$, the WDT trigger, the parity trigger, or the SW trigger.

2.3.4.4 External Interface

The SCU provides interface pads for system purpose. Various functions are covered by these pins. Due to the different tasks some of the pads can not be shared with other functions but most of them can be shared with other functions. The following functions are covered by the SCU controlled pads:

- Reset request triggers
- Reset indication
- Trap request triggers
- Interrupt request triggers
- Non SCU module triggers

The first three points are covered by the ESR pads and the last two points by the ERU pads.

2.3.4.5 Die Temperature Measurement

The Die Temperature Sensor (DTS) generates a measurement result that indicates directly the current temperature. The result of the measurement can be read via an DTS register.

2.3.5 General Purpose I/O Ports and Peripheral I/O Lines

The TC1767 includes a flexible Ports structure with the following features:

Features

- Digital General-Purpose Input/Output (GPIO) port lines
- Input/output functionality individually programmable for each port line
- Programmable input characteristics (pull-up, pull-down, no pull device)
- Programmable output driver strength for EMI minimization (weak, medium, strong)
- Programmable output characteristics (push-pull, open drain)
- Programmable alternate output functions
- Output lines of each port can be updated port-wise or set/reset/toggled bit-wise

Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: Idle low or idle high state for the shift clock
  - Programmable clock/data phase: Data shift with leading or trailing edge of the shift clock
- Baud rate generation
  - Master Mode: 40.0 Mbit/s to 610.36 bit/s (@ 80 MHz module clock)
  - Slave Mode: 20 Mbit/s to 610.36 bit/s (@ 80 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Flexible SSC pin configuration
- Seven slave select inputs $\overline{\text{SLSI}}$[7:1] in Slave Mode
- Eight programmable slave select outputs SLSO in Master Mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control

The bit timings for the CAN nodes are derived from the module timer clock (f_{CAN}) and are programmable up to a data rate of 1 Mbit/s. External bus transceivers are connected to a CAN node via a pair of receive and transmit pins.

Features

- Compliant with ISO 11898
- CAN functionality according to CAN specification V2.0 B active
- Dedicated control registers for each CAN node
- Data transfer rates up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Advanced CAN bus bit timing analysis and baud rate detection for each CAN node via a frame counter
- Full-CAN functionality: A set of 64 message objects can be individually
  - Allocated (assigned) to any CAN node
  - Configured as transmit or receive object
  - Setup to handle frames with 11-bit or 29-bit identifier
  - Identified by a timestamp via a frame counter
  - Configured to remote monitoring mode
- Advanced Acceptance Filtering
  - Each message object provides an individual acceptance mask to filter incoming frames.
  - A message object can be configured to accept standard or extended frames or to accept both standard and extended frames.
  - Message objects can be grouped into four priority classes for transmission and reception.
  - The selection of the message to be transmitted first can be based on frame identifier, IDE bit and RTR bit according to CAN arbitration rules, or on its order in the list.
- Advanced message object functionality
  - Message objects can be combined to build FIFO message buffers of arbitrary size, limited only by the total number of message objects.
  - Message objects can be linked to form a gateway that automatically transfers frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways can be defined.
- Advanced data management
  - The message objects are organized in double-chained lists.
  - List reorganizations can be performed at any time, even during full operation of the CAN nodes.
  - A powerful, command-driven list controller manages the organization of the list structure and ensures consistency of the list.
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.

2.4.5 Micro Link Interface

This TC1767 contains one Micro Link Interface, MLI0.

The Micro Link Interface (MLI) is a fast synchronous serial interface to exchange data between microcontrollers or other devices, such as stand-alone peripheral components. **Figure 9** shows how two microcontrollers are typically connected together via their MLI interfaces.

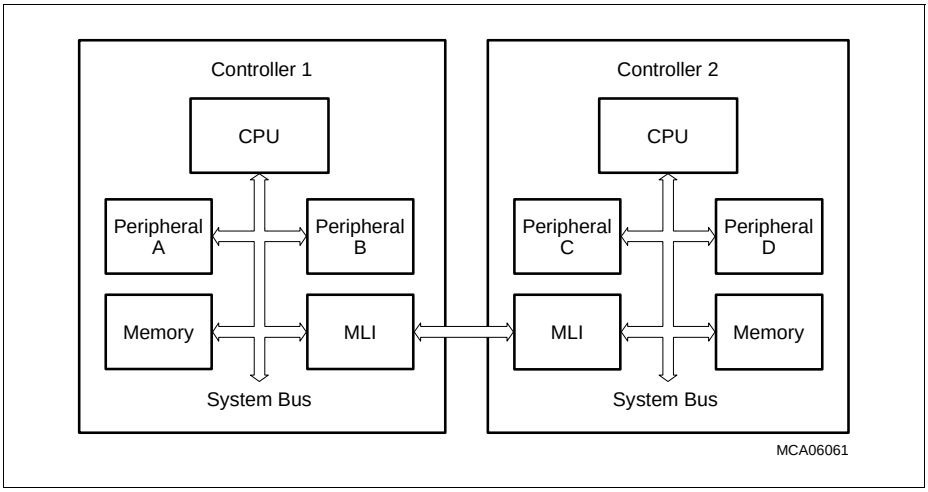

Figure 9 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between an MLI transmitter and an MLI receiver
- Different system clock speeds supported in MLI transmitter and MLI receiver due to full handshake protocol (4 lines between a transmitter and a receiver)
- Fully transparent read/write access supported (= remote programming)
- Complete address range of target device available
- Specific frame protocol to transfer commands, addresses and data
- Error detection by parity bit
- 32-bit, 16-bit, or 8-bit data transfers supported
- Programmable baud rate: $f_{MLI}/2$ (max. $f_{MLI} = f_{SYS}$)
- Address range protection scheme to block unauthorized accesses
- Multiple receiving devices supported

- Multiplexer test mode (channel 7 input can be connected to ground via a resistor for test purposes during run time by specific control bit)
- Power saving mechanisms

Features of the digital part of each ADC kernel:

- Independent result registers (16 independent registers)
- 5 conversion request sources (e.g. for external events, auto-scan, programmable sequence, etc.)
- Synchronization of the ADC kernels for concurrent conversion starts
- Control an external analog multiplexer, respecting the additional set up time
- Programmable sampling times for different channels
- Possibility to cancel running conversions on demand with automatic restart
- Flexible interrupt generation (possibility of DMA support)
- Limit checking to reduce interrupt load
- Programmable data reduction filter by adding conversion results
- Support of conversion data FIFO
- Support of suspend and power down modes
- Individually programmable reference selection for each channel (with exception of dedicated channels always referring to V_{AREF})

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
166	P0.4	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 4**
	IN4	I		**GPTA0 Input 4**
	IN4	I		**LTCA2 Input 4**
	HWCFG4	I		**Hardware Configuration Input 4**
	OUT4	O1		**GPTA0 Output 4**
	OUT60	O2		**GPTA0 Output 60**
	OUT4	O3		**LTCA2 Output 4**
167	P0.5	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 5**
	IN5	I		**GPTA0 Input 5**
	IN5	I		**LTCA2 Input 5**
	HWCFG5	I		**Hardware Configuration Input 5**
	OUT5	O1		**GPTA0 Output 5**
	OUT61	O2		**GPTA0 Output 61**
	OUT5	O3		**LTCA2 Output 5**
173	P0.6	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 6**
	IN6	I		**GPTA0 Input 6**
	IN6	I		**LTCA2 Input 6**
	HWCFG6	I		**Hardware Configuration Input 6**
	REQ2	I		**External Request Input 2**
	OUT6	O1		**GPTA0 Output 6**
	OUT62	O2		**GPTA0 Output 62**
	OUT6	O3		**LTCA2 Output 6**
174	P0.7	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 7**
	IN7	I		**GPTA0 Input 7**
	IN7	I		**LTCA2 Input 7**
	HWCFG7	I		**Hardware Configuration Input 7**
	REQ3	I		**External Request Input 3**
	OUT7	O1		**GPTA0 Output 7**
	OUT63	O2		**GPTA0 Output 63**
	OUT7	O3		**LTCA2 Output 7**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
149	P0.8	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 8**
	IN8	I		**GPTA0 Input 8**
	IN8	I		**LTCA2 Input 8**
	OUT8	O1		**GPTA0 Output 8**
	OUT64	O2		**GPTA0 Output 64**
	OUT8	O3		**LTCA2 Output 8**
150	P0.9	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 9**
	IN9	I		**GPTA0 Input 9**
	IN9	I		**LTCA2 Input 9**
	OUT9	O1		**GPTA0 Output 9**
	OUT65	O2		**GPTA0 Output 65**
	OUT9	O3		**LTCA2 Output 9**
151	P0.10	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 10**
	IN10	I		**GPTA0 Input 10**
	OUT10	O1		**GPTA0 Output 10**
	OUT66	O2		**GPTA0 Output 66**
	OUT10	O3		**LTCA2 Output 10**
152	P0.11	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 11**
	IN11	I		**GPTA0 Input 11**
	OUT11	O1		**GPTA0 Output 11**
	OUT67	O2		**GPTA0 Output 67**
	OUT11	O3		**LTCA2 Output 11**
168	P0.12	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 12**
	IN12	I		**GPTA0 Input 12**
	OUT12	O1		**GPTA0 Output 12**
	OUT68	O2		**GPTA0 Output 68**
	OUT12	O3		**LTCA2 Output 12**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
110	P1.7	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 7**
	IN23	I		**GPTA0 Input 23**
	IN23	I		**LTCA2 Input 23**
	OUT23	O1		**GPTA0 Output 23**
	OUT79	O2		**GPTA0 Output 79**
	OUT23	O3		**LTCA2 Output 23**
94	P1.8	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 8**
	IN24	I		**GPTA0 Input 24**
	IN48	I		**GPTA0 Input 48**
	MTSR1B	I		**SSC1 Slave Receive Input B (Slave Mode)**
	OUT24	O1		**GPTA0 Output 24**
	OUT48	O2		**GPTA0 Output 48**
	MTSR1B	O3		**SSC1 Master Transmit Output B (Master Mode)**
95	P1.9	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 9**
	IN25	I		**GPTA0 Input 25**
	IN49	I		**GPTA0 Input 49**
	MRST1B	I		**SSC1 Master Receive Input B (Master Mode)**
	OUT25	O1		**GPTA0 Output 25**
	OUT49	O2		**GPTA0 Output 49**
	MRST1B	O3		**SSC1 Slave Transmit Output B (Slave Mode)**
96	P1.10	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 10**
	IN26	I		**GPTA0 Input 26**
	IN50	I		**GPTA0 Input 50**
	OUT26	O1		**GPTA0 Output 26**
	OUT50	O2		**GPTA0 Output 50**
	SLSO17	O3		**SSC1 Slave Select Output 7**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
74	P2.0	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 0**
	IN32	I		**GPTA0 Input 32**
	OUT32	O1		**GPTA0 Output 32**
	TCLK0	O2		**MLI0 Transmitter Clock Output 0**
	OUT28	O3		**LTCA2 Output 28**
75	P2.1	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 1**
	IN33	I		**GPTA0 Input 33**
	TREADY0A	I		**MLI0 Transmitter Ready Input A**
	OUT33	O1		**GPTA0 Output 33**
	SLSO03	O2		**SSC0 Slave Select Output Line 3**
	SLSO13	O3		**SSC1 Slave Select Output Line 3**
76	P2.2	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 2**
	IN34	I		**GPTA0 Input 34**
	OUT34	O1		**GPTA0 Output 34**
	TVALID0	O2		**MLI0 Transmitter Valid Output**
	OUT29	O3		**LTCA2 Output 29**
77	P2.3	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 3**
	IN35	I		**GPTA0 Input 35**
	OUT35	O1		**GPTA0 Output 35**
	TDATA0	O2		**MLI0 Transmitter Data Output**
	OUT30	O3		**LTCA2 Output 30**
78	P2.4	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 4**
	IN36	I		**GPTA0 Input 36**
	RCLK0A	I		**MLI Receiver Clock Input A**
	OUT36	O1		**GPTA0 Output 36**
	OUT36	O2		**GPTA0 Output 36**
	OUT31	O3		**LTCA2 Output 31**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
45	AN19	I	D	**Analog Input 19**
44	AN20	I	D	**Analog Input 20**
43	AN21	I	D	**Analog Input 21**
42	AN22	I	D	**Analog Input 22**
41	AN23	I	D	**Analog Input 23**
40	AN24	I	D	**Analog Input 24**
39	AN25	I	D	**Analog Input 25**
38	AN26	I	D	**Analog Input 26**
37	AN27	I	D	**Analog Input 27**
35	AN28	I	D	**Analog Input 28**
34	AN29	I	D	**Analog Input 29**
33	AN30	I	D	**Analog Input 30**
32	AN31	I	D	**Analog Input 31**
31	AN32	I	D	**Analog Input 32**
30	AN33	I	D	**Analog Input 33**
29	AN34	I	D	**Analog Input 34**
28	AN35	I	D	**Analog Input 35**
54	V_{DDM}	-	-	**ADC Analog Part Power Supply (3.3V - 5V)**
53	V_{SSM}	-	-	**ADC Analog Part Ground**
52,	V_{AREF0}	-	-	**ADC0 Reference Voltage**
	V_{AREF1}	-	-	**ADC1 Reference Voltage**
51	V_{AGND0}	-	-	**ADC Reference Ground**
24	V_{DDMF}	-	-	**FADC Analog Part Power Supply (3.3V)[2]**
23	V_{DDAF}	-	-	**FADC Analog Part Logic Power Supply (1.5V)**
25,	V_{SSMF}	-	-	**FADC Analog Part Ground**
	V_{SSAF}	-	-	**FADC Analog Part Ground**
26	V_{FAREF}	-	-	**FADC Reference Voltage**
27	V_{FAGND}	-	-	**FADC Reference Ground**

5.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1767. All parameters specified in the following table refer to these operating conditions, unless otherwise noted.

Table 9 Operating Condition Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage[1]	V_{DD} SR V_{DDOSC} SR	1.42	–	1.58[2]	V	–
	V_{DDP} SR V_{DDOSC3} SR	3.13	–	3.47[3]	V	For Class A pins (3.3 V ± 5%)
	V_{DDFL3} SR	3.13	–	3.47[3]	V	–
Analog supply voltages	V_{DDMF} SR	3.13	–	3.47[3]	V	FADC
	V_{DDAF} SR	1.42	–	1.58[2]	V	FADC
	V_{DDM} SR	4.75	–	5.25	V	For Class D_E pins, ADC
Digital ground voltage	V_{SS} SR	0	–	–	V	–
Ambient temperature under bias	T_A SR	–	-40	125	°C	–
Analog supply voltages	–	–	–	–	–	See separate specification Page 88, Page 93
Overload current at class D pins	I_{OV}	-1	–	3	mA	[4]
Sum of overload current at class D pins	$\Sigma\|I_{OV}\|$	–	–	10	mA	per single ADC
Overload coupling factor for analog inputs[5]	K_{OVAP}	–	–	5×10^{-5}		$0 < I_{OV} < 3$ mA
	K_{OVAN}	–	–	5×10^{-4}		-1 mA $< I_{OV} < 0$
CPU & LMB Bus Frequency	f_{CPU} SR	–	–	133 80	MHz	Derivative dependent
PCP Frequency	f_{PCP} SR	–	–	133 80	MHz	[6]Derivative dependent
FPI Bus Frequency	f_{SYS} SR	–	–	80	MHz	[6]
Short circuit current	I_{SC} SR	-5	–	+5	mA	[7]

Table 12 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Offset error[9)5)]	EA_{OFF} CC	–	±1.0	±4.0	LSB	12-bit conversion without noise[8)10)]
Input leakage current at analog inputs of ADC0/1 [11) 12) 13)]	I_{OZ1} CC	-300	–	100	nA	(0% V_{DDM}) < V_{IN} < (3% V_{DDM})
		-100	–	200	nA	(3% V_{DDM}) < V_{IN} < (97% V_{DDM})
		-100	–	300	nA	(97% V_{DDM}) < V_{IN} < (100% V_{DDM})
Input leakage current at $V_{AREF0/1}$, per module	I_{OZ2} CC	–	–	±1.5	µA	0 V < V_{AREF} < V_{DDM}, no conversion running
Input current at $V_{AREF0/1}$[14)], per module	I_{AREF} CC	–	35	75	µA rms	0 V < V_{AREF} < V_{DDM}[15)]
Total capacitance of the voltage reference inputs[16)14)]	$C_{AREFTOT}$ CC	–	20	40	pF	8)
Switched capacitance at the positive reference voltage input[14)]	C_{AREFSW} CC	–	15	30	pF	8)17)
Resistance of the reference voltage input path[16)]	R_{AREF} CC	–	500	1000	Ω	500 Ohm increased for AN[1:0] used as reference input[8)]
Total capacitance of the analog inputs[16)]	C_{AINTOT} CC	–	25	30	pF	1)8)

Table 13 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Value	Unit	Note
Conversion time with post-calibration	t_C CC	$2 \times T_{ADC} + (4 + STC + n) \times T_{ADCI}$	µs	n = 8, 10, 12 for n - bit conversion $T_{ADC} = 1 / f_{ADC}$ $T_{ADCI} = 1 / f_{ADCI}$
Conversion time without post-calibration		$2 \times T_{ADC} + (2 + STC + n) \times T_{ADCI}$		

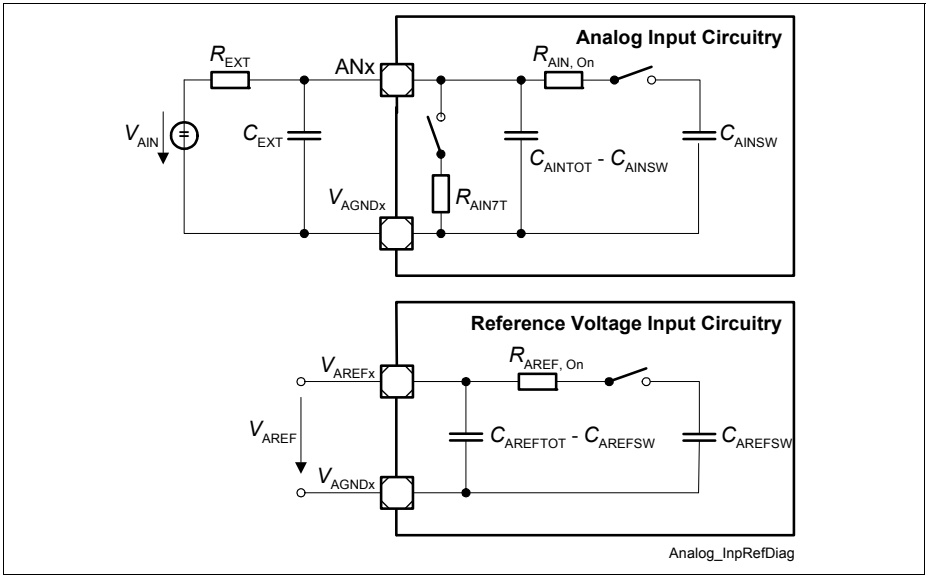

Figure 18 ADC0/ADC1 Input Circuits

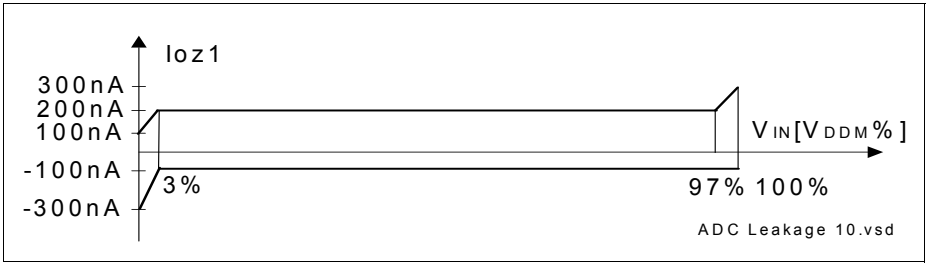

Figure 19 ADC0/ADC1Analog Inputs Leakage

5.3.7 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 22 DAP Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	12.5	–	–	ns	–
DAP0 high time	t_{12} SR	4	–	–	ns	–
DAP0 low time	t_{13} SR	4	–	–	ns	–
DAP0 clock rise time	t_{14} SR	–	–	2	ns	–
DAP0 clock fall time	t_{15} SR	–	–	2	ns	–
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	–
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	–
DAP1 valid per DAP0 clock period[1)]	t_{19} SR	8	–	–	ns	80 MHz, C_L = 20 pF
	t_{19} SR	10	–	–	ns	40 MHz, C_L = 50 pF

1) The Host has to find a suitable sampling point by analyzing the sync telegram response.

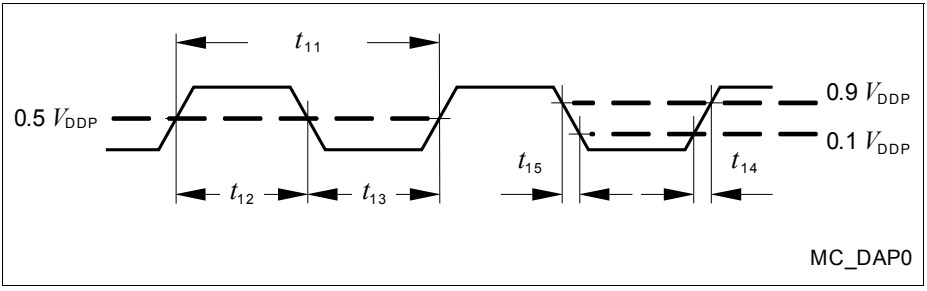

Figure 29 Test Clock Timing (DAP0)

Table 25 SSC Master/Slave Mode Timing
(Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Master Mode Timing							
SCLK clock period	t_{50}	CC	$2 \times T_{SSC}$	–	–	ns	1)2)3)
MTSR/SLSOx delay from SCLK rising edge	t_{51}	CC	0	–	8	ns	–
MRST setup to SCLK falling edge	t_{52}	SR	13	–	–	ns	3)
MRST hold from SCLK falling edge	t_{53}	SR	0	–	–	ns	3)
Slave Mode Timing							
SCLK clock period	t_{54}	SR	$4 \times T_{SSC}$	–	–	ns	1)3)
SCLK duty cycle	t_{55}/t_{54}	SR	45	–	55	%	–
MTSR setup to SCLK latching edge	t_{56}	SR	$T_{SSC} + 5$	–	–	ns	3)4)
MTSR hold from SCLK latching edge	t_{57}	SR	$T_{SSC} + 5$	–	–	ns	3)4)
$\overline{\text{SLSI}}$ setup to first SCLK latching edge	t_{58}	SR	$T_{SSC} + 5$	–	–	ns	3)
$\overline{\text{SLSI}}$ hold from last SCLK latching edge	t_{59}	SR	7	–	–	ns	–
MRST delay from SCLK shift edge	t_{60}	CC	0	–	15	ns	–
$\overline{\text{SLSI}}$ to valid data on MRST	t_{61}	CC	–	–	10	ns	–

1) SCLK signal rise/fall times are the same as the A2 Pads rise/fall times.
2) SCLK signal high and low times can be minimum $1 \times T_{SSC}$.
3) $T_{SSCmin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 80 MHz, t_{50} = 25 ns.
4) Fractional divider switched off, SSC internal baud rate generation used.