Infineon Technologies - TC1767256F80HLADKXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	ASC, CANbus, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	88
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 4x10b, 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1767256f80hladkxuma1

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32-Bit

TC1767

32-Bit Single-Chip Microcontroller

Data Sheet

V1.4 2012-07

Microcontrollers

TC1767 Data Sheet

Revision History: V1.4 2012-07

Previous Versions: V1.3	
Page	Subjects (major changes since last revision)
Page 6	Salescode for Copper-bonded device is added

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register names contain a module name prefix, separated by an underscore character "_" from the actual register name (for example, "ASC0_CON", where "ASC0" is the module name prefix, and "CON" is the kernel register name). In chapters describing the kernels of the peripheral modules, the registers are mainly referenced with their kernel register names. The peripheral module implementation sections mainly refer to the actual register names with module prefixes.

- Variables used to describe sets of processing units or registers appear in mixed upper and lower cases. For example, register name "MSGCFGn" refers to multiple "MSGCFG" registers with variable n. The bounds of the variables are always given where the register expression is first used (for example, "n = 0-31"), and are repeated as needed in the rest of the text.
- The default radix is decimal. Hexadecimal constants are suffixed with a subscript letter "H", as in 100_H. Binary constants are suffixed with a subscript letter "B", as in: 111_B.
- When the extent of register fields, groups register bits, or groups of pins are collectively named in the body of the document, they are represented as "NAME[A:B]", which defines a range for the named group from B to A. Individual bits, signals, or pins are given as "NAME[C]" where the range of the variable C is given in the text. For example: CFG[2:0] and SRPN[0].
- Units are abbreviated as follows:
  - **MHz** = Megahertz
  - **µs** = Microseconds
  - **kBaud, kbit** = 1000 characters/bits per second
  - **MBaud, Mbit** = 1,000,000 characters/bits per second
  - **Kbyte, KB** = 1024 bytes of memory
  - **Mbyte, MB** = 1048576 bytes of memory

    In general, the k prefix scales a unit by 1000 whereas the K prefix scales a unit by 1024. Hence, the Kbyte unit scales the expression preceding it by 1024. The kBaud unit scales the expression preceding it by 1000. The M prefix scales by 1,000,000 or 1048576, and µ scales by .000001. For example, 1 Kbyte is 1024 bytes, 1 Mbyte is 1024 × 1024 bytes, 1 kBaud/kbit are 1000 characters/bits per second, 1 MBaud/Mbit are 1000000 characters/bits per second, and 1 MHz is 1,000,000 Hz.
- Data format quantities are defined as follows:
  - **Byte** = 8-bit quantity
  - **Half-word** = 16-bit quantity
  - **Word** = 32-bit quantity
  - **Double-word** = 64-bit quantity

2.1.3 Reserved, Undefined, and Unimplemented Terminology

In tables where register bit fields are defined, the following conventions are used to indicate undefined and unimplemented function. Furthermore, types of bits and bit fields are defined using the abbreviations as shown in **Table 2**.

Table 2 Bit Function Terminology

Function of Bits	Description
Unimplemented, Reserved	Register bit fields named **0** indicate unimplemented functions with the following behavior. • Reading these bit fields returns 0. • These bit fields should be written with 0 if the bit field is defined as r or rh. • These bit fields have to be written with 0 if the bit field is defined as rw. These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.
rw	The bit or bit field can be read and written.
rwh	As rw, but bit or bit field can be also set or reset by hardware.
r	The bit or bit field can only be read (read-only).
w	The bit or bit field can only be written (write-only). A read to this register will always give a default value back.
rh	This bit or bit field can be modified by hardware (read-hardware, typical example: status flags). A read of this bit or bit field give the actual status of this bit or bit field back. Writing to this bit or bit field has no effect to the setting of this bit or bit field.
s	Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten by software, they can be switched again into their reset state only by a reset operation. Software cannot switch this type of bit into its reset state by writing the register. This attribute can be combined to “rws” or “rwhs”.
f	Bits with this attribute are readable only when they are accessed by an instruction fetch. Normal data read operations will return other values.

2.1.4 Register Access Modes

Read and write access to registers and memory locations are sometimes restricted. In memory and register access tables, the terms as defined in **Table 3** are used.

- Trigger sources that do not depend on a clock, such as the $\overline{\text{PORST}}$. This trigger force the device into an asynchronous reset assertion independently of any clock. The activation of an asynchronous reset is asynchronous to the system clock, whereas its de-assertion is synchronized.
- Trigger sources that need a clock in order to be asserted, such as the input signals $\overline{\text{ESR0}}$, and $\overline{\text{ESR1}}$, the WDT trigger, the parity trigger, or the SW trigger.

2.3.4.4 External Interface

The SCU provides interface pads for system purpose. Various functions are covered by these pins. Due to the different tasks some of the pads can not be shared with other functions but most of them can be shared with other functions. The following functions are covered by the SCU controlled pads:

- Reset request triggers
- Reset indication
- Trap request triggers
- Interrupt request triggers
- Non SCU module triggers

The first three points are covered by the ESR pads and the last two points by the ERU pads.

2.3.4.5 Die Temperature Measurement

The Die Temperature Sensor (DTS) generates a measurement result that indicates directly the current temperature. The result of the measurement can be read via an DTS register.

2.3.5 General Purpose I/O Ports and Peripheral I/O Lines

The TC1767 includes a flexible Ports structure with the following features:

Features

- Digital General-Purpose Input/Output (GPIO) port lines
- Input/output functionality individually programmable for each port line
- Programmable input characteristics (pull-up, pull-down, no pull device)
- Programmable output driver strength for EMI minimization (weak, medium, strong)
- Programmable output characteristics (push-pull, open drain)
- Programmable alternate output functions
- Output lines of each port can be updated port-wise or set/reset/toggled bit-wise

2.4.3 Micro Second Channel Interface

The Micro Second Channel (MSC) interface provides serial communication links typically used to connect power switches or other peripheral devices. The serial communication link includes a fast synchronous downstream channel and a slow asynchronous upstream channel. **Figure 7** shows a global view of the interface signals of the MSC interface.

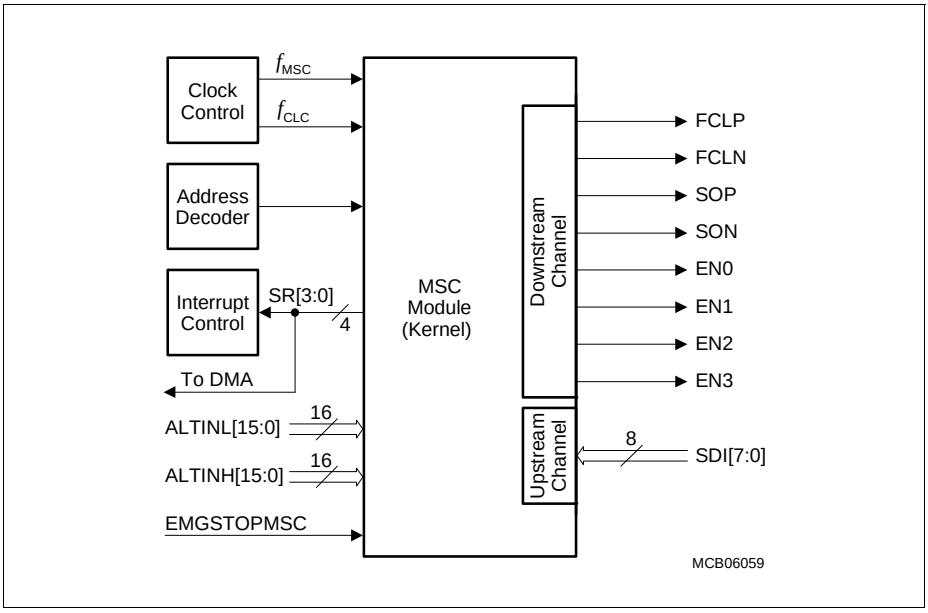

Figure 7 General Block Diagram of the MSC Interface

The downstream and upstream channels of the MSC module communicate with the external world via nine I/O lines. Eight output lines are required for the serial communication of the downstream channel (clock, data, and enable signals). One out of eight input lines SDI[7:0] is used as serial data input signal for the upstream channel. The source of the serial data to be transmitted by the downstream channel can be MSC register contents or data that is provided on the ALTINL/ALTINH input lines. These input lines are typically connected with other on-chip peripheral units (for example with a timer unit such as the GPTA). An emergency stop input signal makes it possible to set bits of the serial data stream to dedicated values in an emergency case.

Clock control, address decoding, and interrupt service request control are managed outside the MSC module kernel. Service request outputs are able to trigger an interrupt or a DMA request.

  - Static allocation commands offer compatibility with MultiCAN applications that are not list-based.
- Advanced interrupt handling
  - Up to 16 interrupt output lines are available. Interrupt requests can be routed individually to one of the 16 interrupt output lines.
  - Message post-processing notifications can be combined flexibly into a dedicated register field of 256 notification bits.

2.4.5 Micro Link Interface

This TC1767 contains one Micro Link Interface, MLI0.

The Micro Link Interface (MLI) is a fast synchronous serial interface to exchange data between microcontrollers or other devices, such as stand-alone peripheral components. **Figure 9** shows how two microcontrollers are typically connected together via their MLI interfaces.

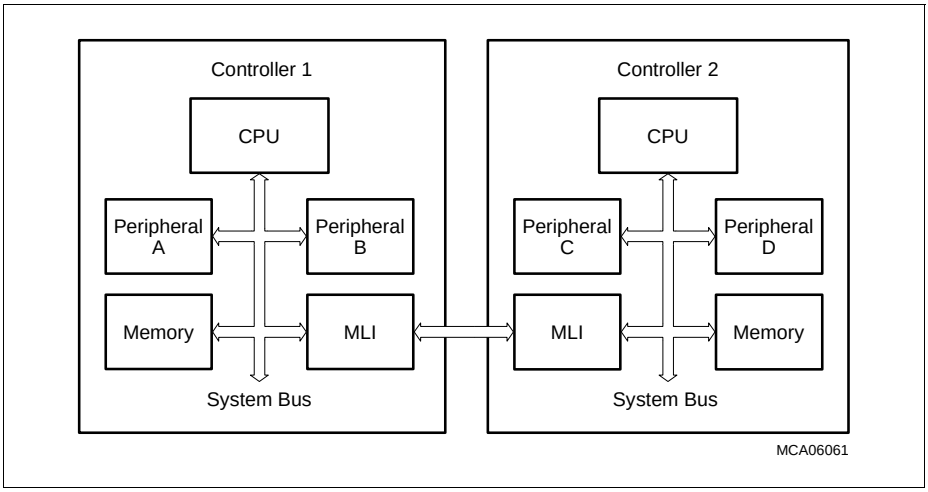

Figure 9 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between an MLI transmitter and an MLI receiver
- Different system clock speeds supported in MLI transmitter and MLI receiver due to full handshake protocol (4 lines between a transmitter and a receiver)
- Fully transparent read/write access supported (= remote programming)
- Complete address range of target device available
- Specific frame protocol to transfer commands, addresses and data
- Error detection by parity bit
- 32-bit, 16-bit, or 8-bit data transfers supported
- Programmable baud rate: $f_{MLI}/2$ (max. $f_{MLI} = f_{SYS}$)
- Address range protection scheme to block unauthorized accesses
- Multiple receiving devices supported

  - f_{GPTA}/4 maximum input signal frequency in 2-sensor Mode, f_{GPTA}/6 maximum input signal frequency in 3-sensor Mode
- Duty Cycle Measurement (DCM)
  - Four independent units
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Clock Distribution Unit (CDU)
  - One unit
  - Provides nine clock output signals: f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
  - Two independent units
  - Two operating modes (Free-Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 units related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Local Timer Cell (LTC)
  - 64 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

Interrupt Sharing Unit

- 143 interrupt sources, generating up to 46 service requests

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
149	P0.8	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 8**
	IN8	I		**GPTA0 Input 8**
	IN8	I		**LTCA2 Input 8**
	OUT8	O1		**GPTA0 Output 8**
	OUT64	O2		**GPTA0 Output 64**
	OUT8	O3		**LTCA2 Output 8**
150	P0.9	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 9**
	IN9	I		**GPTA0 Input 9**
	IN9	I		**LTCA2 Input 9**
	OUT9	O1		**GPTA0 Output 9**
	OUT65	O2		**GPTA0 Output 65**
	OUT9	O3		**LTCA2 Output 9**
151	P0.10	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 10**
	IN10	I		**GPTA0 Input 10**
	OUT10	O1		**GPTA0 Output 10**
	OUT66	O2		**GPTA0 Output 66**
	OUT10	O3		**LTCA2 Output 10**
152	P0.11	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 11**
	IN11	I		**GPTA0 Input 11**
	OUT11	O1		**GPTA0 Output 11**
	OUT67	O2		**GPTA0 Output 67**
	OUT11	O3		**LTCA2 Output 11**
168	P0.12	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 12**
	IN12	I		**GPTA0 Input 12**
	OUT12	O1		**GPTA0 Output 12**
	OUT68	O2		**GPTA0 Output 68**
	OUT12	O3		**LTCA2 Output 12**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
74	P2.0	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 0**
	IN32	I		**GPTA0 Input 32**
	OUT32	O1		**GPTA0 Output 32**
	TCLK0	O2		**MLI0 Transmitter Clock Output 0**
	OUT28	O3		**LTCA2 Output 28**
75	P2.1	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 1**
	IN33	I		**GPTA0 Input 33**
	TREADY0A	I		**MLI0 Transmitter Ready Input A**
	OUT33	O1		**GPTA0 Output 33**
	SLSO03	O2		**SSC0 Slave Select Output Line 3**
	SLSO13	O3		**SSC1 Slave Select Output Line 3**
76	P2.2	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 2**
	IN34	I		**GPTA0 Input 34**
	OUT34	O1		**GPTA0 Output 34**
	TVALID0	O2		**MLI0 Transmitter Valid Output**
	OUT29	O3		**LTCA2 Output 29**
77	P2.3	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 3**
	IN35	I		**GPTA0 Input 35**
	OUT35	O1		**GPTA0 Output 35**
	TDATA0	O2		**MLI0 Transmitter Data Output**
	OUT30	O3		**LTCA2 Output 30**
78	P2.4	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 4**
	IN36	I		**GPTA0 Input 36**
	RCLK0A	I		**MLI Receiver Clock Input A**
	OUT36	O1		**GPTA0 Output 36**
	OUT36	O2		**GPTA0 Output 36**
	OUT31	O3		**LTCA2 Output 31**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1)]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
111	TDI	I	A2/ PU	**JTAG Serial Data Input**
	BRKIN	I		**OCDS Break Input Line**
	BRKOUT	O		**OCDS Break Output Line**
112	TMS	I	A2/ PD	**JTAG State Machine Control Input**
	DAP1	I/O		**Device Access Port Line 1**
113	TDO	I/O	A2/ PU	**JTAG Serial Data Output**
	DAP2	I/O		**Device Access Port Line 2**
	BRKIN	I		**OCDS Break Input Line**
	BRKOUT	O		**OCDS Break Output Line**
114	$\overline{\text{TRST}}$	I	A1/ PD	**JTAG Reset Input**
115	TCK	I	A1/ PD	**JTAG Clock Input**
	DAP0	I		**Device Access Port Line 0**
118	$\overline{\text{TESTMODE}}$	I	PU	**Test Mode Select Input**
120	$\overline{\text{ESR1}}$	I/O	A2/ PD	**External System Request Reset Input 1**
121	$\overline{\text{PORST}}$	I	PD	**Power On Reset Input** (input pad with input spike-filter)
122	$\overline{\text{ESR0}}$	I/O	A2	**External System Request Reset Input 0** Default configuration during and after reset is open-drain driver, corresponding to A2 strong driver, sharp edge. The driver drives low during power-on reset.

1) TC1767 ED: PG-LQFP-176-6

2) This pin is also connected to the analog power supply for comparator of the ADC module.

3) For the TC1767 emulation device (ED), this pin is bonded to VDD_{SB} (ED Stand By RAM supply). In the TC1767 non ED device, this pin is bonded to a VDD pad.

Legend for Table 4

Column "**Ctrl.**":

I = Input (for GPIO port lines with IOCR bit field selection PCx = $0XXX_B$)

O = Output
O0 = Output with IOCR bit field selection PCx = $1X00_B$
O1 = Output with IOCR bit field selection PCx = $1X01_B$ (ALT1)

O2 = Output with IOCR bit field selection PCx = $1X10_B$(ALT2)
O3 = Output with IOCR bit field selection PCx = 1X11(ALT3)

Column “**Type**”:

A1 = Pad class A1 (LVTTL)
A2 = Pad class A2 (LVTTL)
F = Pad class F (LVDS/CMOS)
D = Pad class D (ADC)

PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
TR = tri-state during reset ($\overline{\text{PORST}}$ = 0)

3.1.2 Reset Behavior of the Pins

Table 5 describes the pull-up/pull-down behavior of the System I/O pins during power-on reset.

Table 5 List of Pull-up/Pull-down $\overline{\text{PORST}}$ Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
All GPIOs, TDI, $\overline{\text{TESTMODE}}$	Pull-up	
$\overline{\text{PORST}}$, $\overline{\text{TRST}}$, TCK, TMS	Pull-down	
$\overline{\text{ESR0}}$	The open-drain driver is used to drive low.[1)]	Pull-up[2)]
$\overline{\text{ESR1}}$	Pull-down[3)]	
TDO	Pull-up	High-impedance

1) Valid additionally after deactivation of $\overline{\text{PORST}}$ until the internal reset phase has finished. See the SCU chapter for details.
2) See the SCU_IOCR register description.
3) see the SCU_IOCR register description.

Table 6 TC1767 Identification Registers (cont'd)

Short Name	Value	Address	Stepping
SCU_MANID	0000 1820_H	F000 0644_H	–
SCU_RTID	0000 0007_H	F000 0648_H	AD-step
SSC0_ID	0000 4511_H	F010 0108_H	–
SSC1_ID	0000 4511_H	F010 0208_H	–
STM_ID	0000 $C006_H$	F000 0208_H	–

Table 10 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
5	P1.[7:4]; TDI/$\overline{\text{BRKIN}}$/$\overline{\text{BRKOUT}}$; $\overline{\text{TRST}}$, TCK/DAP0; P1.[1:0]; P1.15; $\overline{\text{TESTMODE}}$; $\overline{\text{ESR0}}$; $\overline{\text{PORST}}$; $\overline{\text{ESR1}}$
6	P3.[10:0]; P3.[15:14]
7	P3.[13:11]; P0.[3:0]; P0.[11:8]
8	P6.[3:0]; P2.[13:8]; P0.[5:4]; P0.[13:12]
9	P0.[7:6]; P0.[15:14]; P5.[7:0]; P5.15

Table 13 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Value	Unit	Note
Conversion time with post-calibration	t_C CC	$2 \times T_{ADC} + (4 + STC + n) \times T_{ADCI}$	µs	n = 8, 10, 12 for n - bit conversion $T_{ADC} = 1 / f_{ADC}$ $T_{ADCI} = 1 / f_{ADCI}$
Conversion time without post-calibration		$2 \times T_{ADC} + (2 + STC + n) \times T_{ADCI}$		

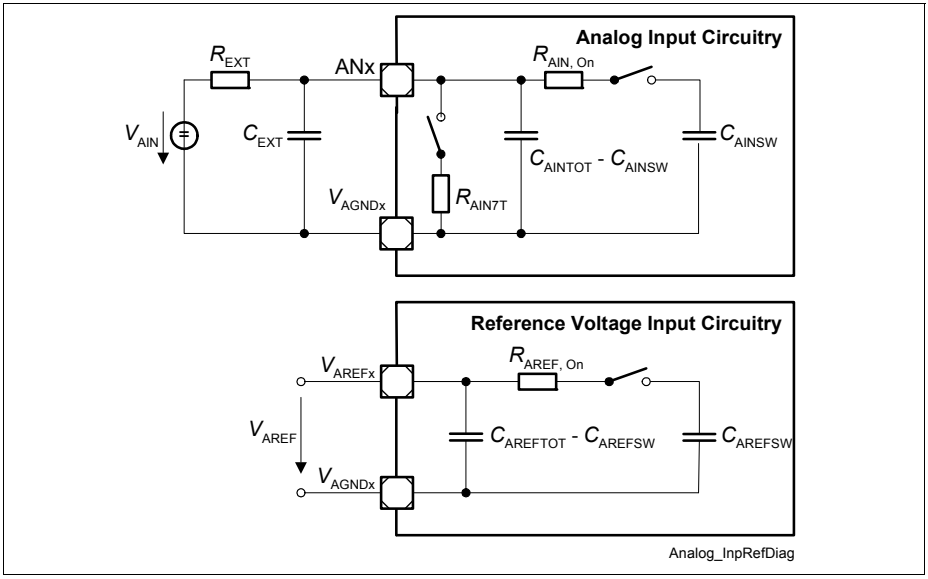

Figure 18 ADC0/ADC1 Input Circuits

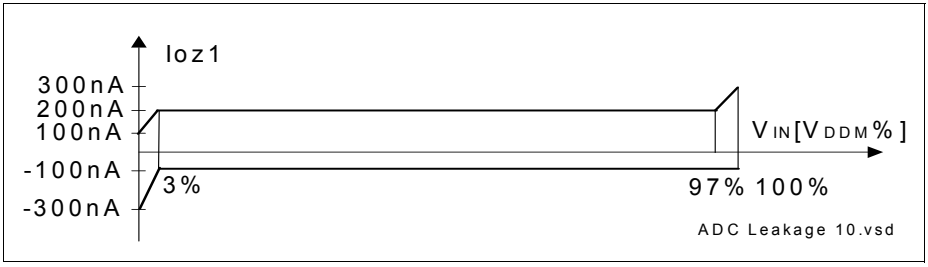

Figure 19 ADC0/ADC1Analog Inputs Leakage

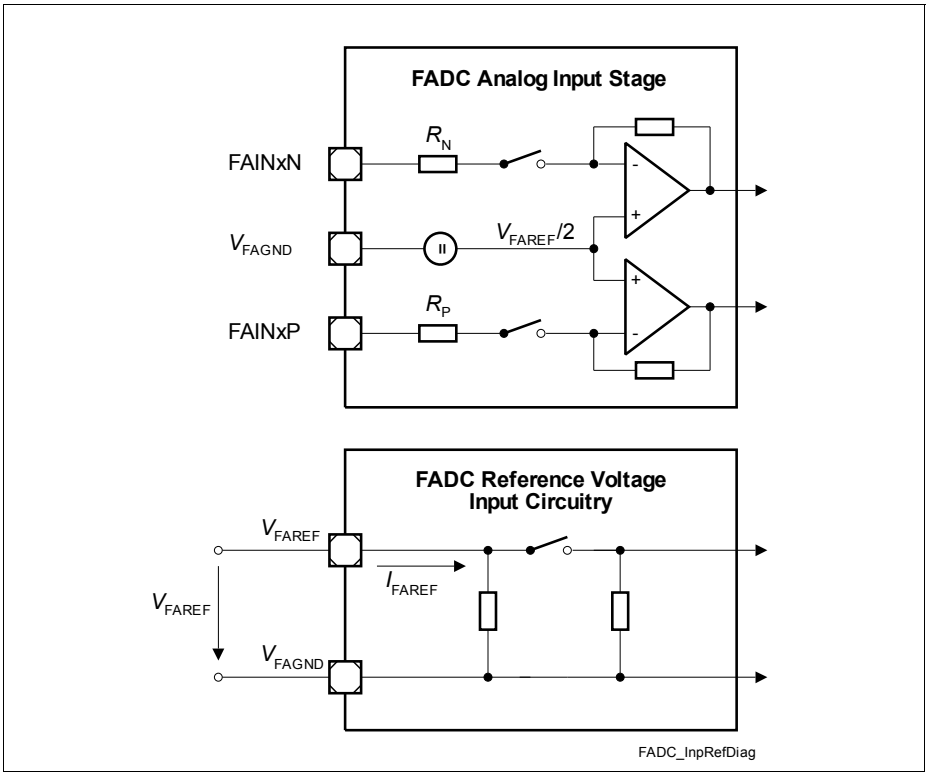

Figure 20 FADC Input Circuits

With rising number m of clock cycles the maximum jitter increases linearly up to a value of m that is defined by the K2-factor of the PLL. Beyond this value of m the maximum accumulated jitter remains at a constant value. Further, a lower LMB-Bus clock frequency f_{LMB} results in a higher absolute maximum jitter value.

Figure 26 gives the jitter curves for several K2 / f_{LMB} combinations.

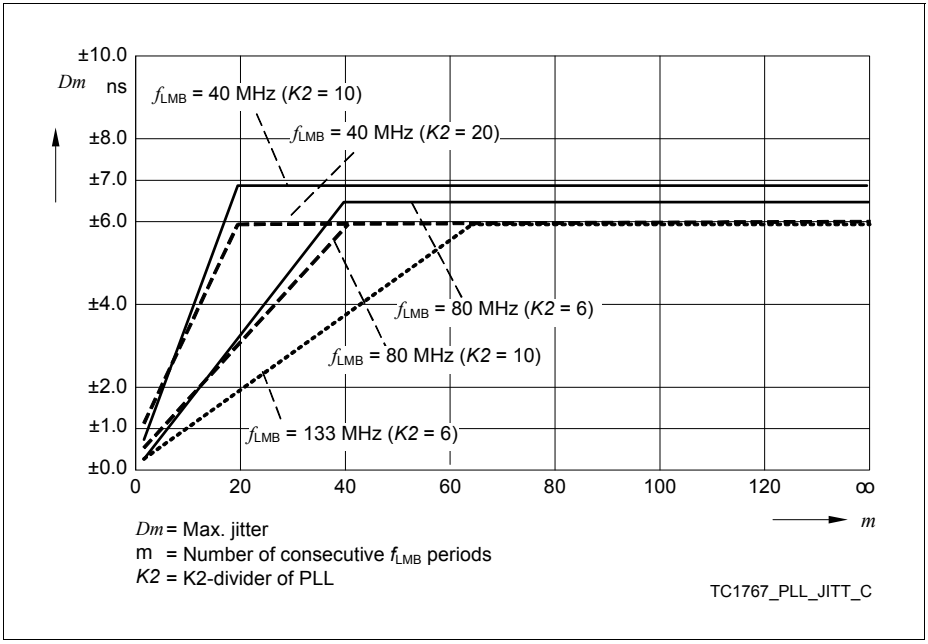

Figure 26 Approximated Maximum Accumulated PLL Jitter for Typical LMB-Bus Clock Frequencies f_{LMB}

Note: The specified PLL jitter values are valid if the capacitive load per output pin does not exceed C_L = 20 pF with the maximum driver and sharp edge. In case of applications with many pins with high loads, driver strengths and toggle rates the specified jitter values could be exceeded.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDOSC3} at pin 106 and V_{SSOSC} at pin 104, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.

The maximum peak-to peak noise on the pad supply votage, measured between V_{DDOSC} at pin 105 and V_{SSOSC} at pin 104, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.

5.4.2 Package Outline

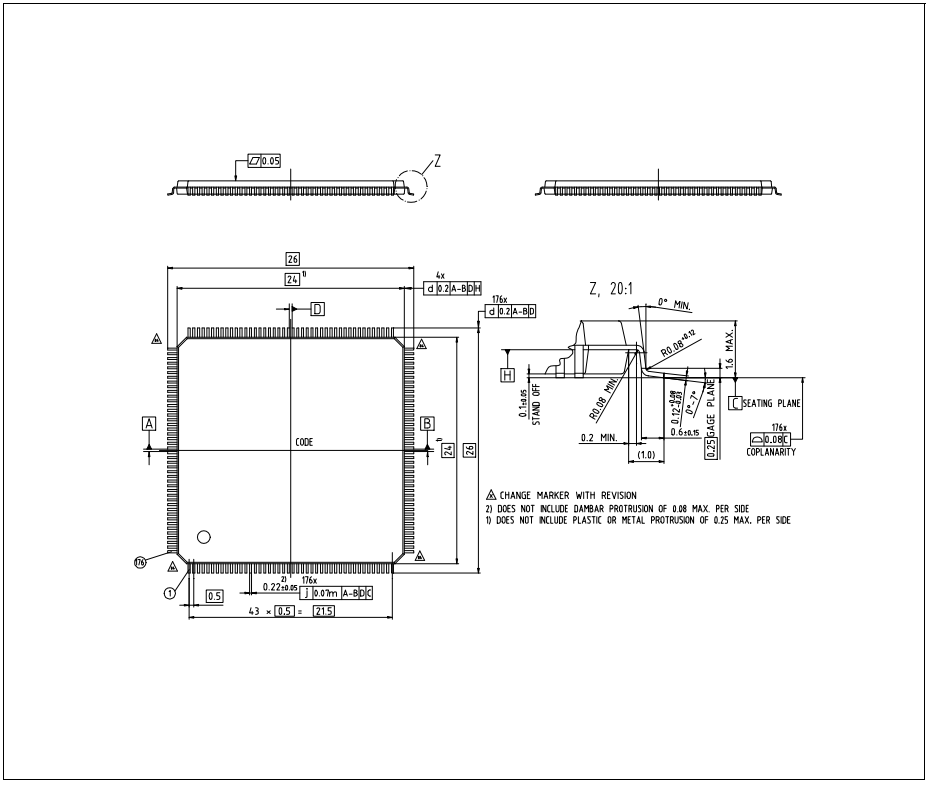

Figure 36 PG-LQFP-176-5, Plastic Green Low Profile Quad Flat Package

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: ***http://www.infineon.com/products***.