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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572clvtaule

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Overview

the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
 - Shared by both cores.
 - Flexible configuration and individually configurable per core.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - Per-way allocation of cache region to a given processor.
 - SRAM features include the following:
 - 1, 2, 4, or 8 ways can be configured as SRAM.
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
 - Twelve local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.



Overview

- Multiplexed 32-bit address and data bus operating at up to 150 MHz
- Eight chip selects support eight external slaves
- Up to 8-beat burst transfers
- The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
- Three protocol engines available on a per-chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - NAND Flash control machine (FCM)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Four IEEE Std 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, RGMII, and SGMII
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
 - Flexible configuration for multiple PHY interface configurations
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (Q-in-Q) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1TM virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision



4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8572E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3V ± 5% or 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
EC_GTX_CLK125 frequency	f _{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t _{G125}	—	8	—	ns	_
EC_GTX_CLK125 rise and fall time L/TV_DD=2.5V L/TV_DD=3.3V	t _{G125R} , t _{G125F}	_	_	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t _{G125H} /t _{G125}	45 47	_	55 53	%	2, 3

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for L/TV_{DD}=2.5V, and from 0.6V and 2.7V for L/TV_{DD}=3.3V.

- 2. Timing is guaranteed by design and characterization.
- 3. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC*n*_GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 DDR Clock Timing

Table 8 provides the DDR clock (DDRCLK) AC timing specifications for the MPC8572E.

Table 8. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
DDRCLK frequency	f _{DDRCLK}	66	—	100	MHz	1
DDRCLK cycle time	t _{DDRCLK}	10.0	—	15.15	ns	_
DDRCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	1.2	ns	2
DDRCLK duty cycle	t _{KHK} /t _{DDRCLK}	40	—	60	%	3



Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t _{DDKHAX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCS[n] output setup with respect to MCK	t _{DDKHCS}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz	t _{DDKHCS}	1.95	_	ns	3
MCS[n] output hold with respect to MCK	t _{DDKHCX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS Skew	t _{DDKHMH}			ns	4
800 MHz		-0.375	0.375		
<= 667 MHz		-0.6	0.6		
MDQ/MECC/MDM output setup with respect to MDQS	t _{DDKHDS,} t _{DDKLDS}			ps	5
800 MHz		375	_		
667 MHz		450	_		
533 MHz		538	_		
400 MHz		700	_		
MDQ/MECC/MDM output hold with respect to MDQS	t _{DDKHDX,} t _{DDKLDX}			ps	5
800 MHz		375	—		
667 MHz		450	_		



Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

Figure 11 shows the GMII receive AC timing diagram.



Figure 11. GMII Receive AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 29 provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t _{MTX} ²	_	400	—	ns
TX_CLK clock period 100 Mbps	t _{MTX}	_	40	—	ns
TX_CLK duty cycle	t _{MTXH} /t _{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t _{MTXR} ²	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	t _{MTXF} ²	1.0	_	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

2. Guaranteed by design.



Table 35. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 19 shows the RMII transmit AC timing diagram.



Figure 19. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 36 shows the RMII receive AC timing specifications.

Table 36. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSECn_TX_CLK clock period	t _{RMR}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t _{RMRH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t _{RMRJ}	_	_	250	ps
Rise time TSECn_TX_CLK (20%-80%)	t _{RMRR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t _{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to TSECn_TX_CLK rising edge	t _{RMRDV}	4.0	—	—	ns



10 Local Bus Controller (eLBC)

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8572E.

10.1 Local Bus DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 3.3 \text{ V}$ DC.

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	BV _{DD}	3.13	3.47	V
High-level input voltage	V _{IH}	2	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current ($BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	I _{IN}	_	±5	μA
High-level output voltage (BV _{DD} = min, I _{OH} = -2 mA)	V _{OH}	BV _{DD} – 0.2	—	V
Low-level output voltage (BV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	_	0.2	V

 Table 46. Local Bus DC Electrical Characteristics (3.3 V DC)

Note:

1. Note that the symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1.

Table 47 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 2.5 V DC$.

Table 47. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Мах	Unit
Supply voltage 2.5V	BV _{DD}	2.37	2.63	V
High-level input voltage	V _{IH}	1.70	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.7	V
Input current	I _{IH}	—	10	μΑ
$(BV_{IN} = 0 V \text{ of } BV_{IN} = BV_{DD})$	Ι _{ΙL}		-15	
High-level output voltage (BV _{DD} = min, I _{OH} = -1 mA)	V _{OH}	2.0	BV _{DD} + 0.3	V
Low-level output voltage (BV _{DD} = min, I _{OL} = 1 mA)	V _{OL}	GND – 0.3	0.4	V

Note:

1. The symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1.



Table 49. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC)—PLL Enabled (continued)

At recommended operating conditions with $\mathsf{BV}_{\mathsf{DD}}$ of 3.3 V ± 5%. (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	—	2.5	ns	5

Note:

- The symbols used for timing specifications herein follow the pattern of t_{(First two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(First two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 8. Guaranteed by design.

Table 50 describes the general timing parameters of the local bus interface at $BV_{DD} = 2.5 \text{ V DC}$.

Tabl	e 50. L	ocal B	lus	Gene	eral	l Tin	ning F	Parameters	(BV _{DD}	= 2.5 \	/ DC)—	-PLL	Enabled

At recommended operating conditions with BV_{DD} of 2.5 V \pm 5%

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	6.67	12	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}		150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	1.9	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.8	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.1	—	ns	3, 4
LALE output negation to high impedance for LAD/LDP (LATCH hold time)	t _{LBOTOT}	1.5		ns	6



Table 52. Local Bus General Timing Parameters—PLL Bypassed (continued)

At recommended operating conditions with BV_{DD} of 3.3 V ± 5%

Parameter	Symbol ¹	Min	Мах	Unit	Notes
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKL2}	-1.3	_	ns	4, 5
LALE output negation to high impedance for LAD/LDP (LATCH hold time)	t _{LBOTOT}	1.5	_	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKLOV1}	_	-0.3	ns	
Local bus clock to data valid for LAD/LDP	t _{LBKLOV2}	—	-0.1	ns	4
Local bus clock to address valid for LAD	t _{LBKLOV3}	—	0.0	ns	4
Local bus clock to LALE assertion	t _{LBKLOV4}	—	0.0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKLOX1}	-3.3	—	ns	4
Output hold from local bus clock for LAD/LDP	t _{LBKLOX2}	-3.3	_	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKLOZ1}	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	t _{LBKLOZ2}	_	0.2	ns	7

Notes:

- The symbols used for timing specifications herein follow the pattern of t<sub>(First two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
- 3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
- 5. Input timings are measured at the pin.
- t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at the falling edge of the internal clock with the exception of LGTA/LUPWAIT (which is captured on the rising edge of the internal clock).



Table 58 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD} = 1.8 \text{ V DC}$. Table 58. GPIO DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 1.8V	BV _{DD}	1.71	1.89	V
High-level input voltage	V _{IH}	0.65 x BV _{DD}	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.35 x BV _{DD}	V
Input current $(BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD})$	I _{IN}	TBD	TBD	μA
High-level output voltage $(I_{OH} = -100 \ \mu A)$	V _{OH}	BV _{DD} – 0.2	—	V
High-level output voltage $(I_{OH} = -2 \text{ mA})$	V _{OH}	BV _{DD} – 0.45	—	V
Low-level output voltage $(I_{OL} = 100 \ \mu A)$	V _{OL}	-	0.2	V
Low-level output voltage (I _{OL} = 2 mA)	V _{OL}	—	0.45	V

Note:

1. The symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1.

14.2 GPIO AC Electrical Specifications

Table 59 provides the GPIO input and output AC timing specifications.

Table 59. GPIO Input AC Timing Specifications¹

Parameter	Symbol	Тур	Unit	Notes
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns	2

Notes:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYSCLK. Timings are measured at the pin.
- 2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 42 provides the AC test load for the GPIO.





15.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, additionally to AC-coupling.

NOTE

Figure 48 to Figure 51 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8572E SerDes reference clock receiver requirement provided in this document.



High-Speed Serial Interfaces (HSSI)

clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.



Figure 50. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 51 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8572E SerDes reference clock input's DC requirement.



15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and



Serial RapidIO



Figure 60. Receiver Input Compliance Mask

Table 75.	Receiver Ir	nput Compliance	Mask Parameters	Exclusive of	of Sinusoidal Jitte
14010 101		ipat eeinpilaliee	maon i aramotoro		

Receiver Type	V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

17.8 Measurement and Test Requirements

Because the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

17.8.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial



Package Description

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_GTX_CLK	Transmit Clock Out	AE17	0	TV _{DD}	
TSEC3_RX_CLK/FEC_RX_CL K/FIFO3_RX_CLK	Receive Clock	AF17	I	TV _{DD}	1
TSEC3_RX_DV/FEC_RX_DV/ FIFO3_RX_DV	Receive Data Valid	AG14	I	TV _{DD}	1
TSEC3_RX_ER/FEC_RX_ER/ FIFO3_RX_ER	Receive Error	AH15	I	TV _{DD}	1
TSEC3_TX_CLK/FEC_TX_CL K/FIFO3_TX_CLK	Transmit Clock In	AF16	I	TV _{DD}	1
TSEC3_TX_EN/FEC_TX_EN/F IFO3_TX_EN	Transmit Enable	AJ18	0	TV _{DD}	1, 22
	Three-Speed Ethern	et Controller 4			
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]/FIFO3_TXD[7:4]	Transmit Data	AD15, AC16, AC14, AB16	0	TV _{DD}	1, 5, 9
TSEC4_RXD[3:0]/TSEC3_RXD [7:4]/FIFO3_RXD[7:4]	Receive Data	AE15, AF13, AE14, AH14	I	TV _{DD}	1
TSEC4_GTX_CLK	Transmit Clock Out	Out AB14		TV _{DD}	_
TSEC4_RX_CLK/TSEC3_COL/ FEC_COL/FIFO3_TX_FC	Receive Clock	AG13	I	TV _{DD}	1
TSEC4_RX_DV/TSEC3_CRS/ FEC_CRS/FIFO3_RX_FC	Receive Data Valid	AD13	I/O	TV _{DD}	1, 23
TSEC4_TX_EN/TSEC3_TX_E R/FEC_TX_ER/FIFO3_TX_ER	Transmit Enable	AB15	0	TV _{DD}	1, 22
	DUAR	Т			
UART_CTS[0:1]	Clear to Send	W30, Y27	I	OV _{DD}	_
UART_RTS[0:1]	Ready to Send	W31, Y30	0	OV _{DD}	5, 9
UART_SIN[0:1]	Receive Data	Y26, W29	Ι	OV _{DD}	
UART_SOUT[0:1]	Transmit Data	Y25, W26	0	OV _{DD}	5, 9
	I ² C Interf	ace			
IIC1_SCL	Serial Clock	AC30	I/O	OV _{DD}	4, 20
IIC1_SDA	Serial Data	AB30	I/O	OV _{DD}	4, 20
IIC2_SCL	Serial Clock	AD30	I/O	OV _{DD}	4, 20
IIC2_SDA	Serial Data	AD29	I/O	OV _{DD}	4, 20
SerDes (x10) PCIe, SRIO					



Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND_SRDS1	SerDes Transceiver Core Logic GND (xcorevss)	C28, C32, D30, E31, F28, F29, G32, H28, H30, J28, K29, L32, M30, N31, P29, R32	_	_	_
SGND_SRDS2	SerDes Transceiver Core Logic GND (xcorevss)	AE28, AE30, AF28, AF32, AG28, AG30, AH28, AJ28, AJ31, AL32	_	_	_
AGND_SRDS1	SerDes PLL GND	J31		—	
AGND_SRDS2	SerDes PLL GND	AH31	_	—	_
OVDD	General I/O Supply	U31, V24, V28, Y31, AA27, AB25, AB29	_	OVDD	_
LVDD	TSEC 1&2 I/O Supply	AC18, AC21, AG21, AL27	_	LVDD	_
TVDD	TSEC 3&4 I/O Supply	AC15, AE16, AH18	_	TVDD	_
GVDD	SSTL_1.8 DDR Supply	B2, B5, B8, B11, B14, D4, D7, D10, D13, E2, F6, F9, F12, G4, H2, H8, H11, H14, J6, K4, K10, K13, L2, L8, M6, N4, N10, P2, P8, R6, T4, T10, U2, U8, V6, W4, W10, Y2, Y8, AA6, AB4, AB10, AC2, AC8, AD6, AD12, AE4, AE10, AF2, AF8, AG6, AG12, AH4, AH10, AH16, AJ2, AJ8, AJ14, AK6, AK12, AK18, AL4, AL10, AL16, AM2		GVDD	
BVDD	Local Bus and GPIO Supply	A26, A30, B21, D16, D21, F18, G20, H17, J22, K15, K20	—	BVDD	—

Table 78. Memory Bus Clocking Specifications

Characteristic	Min	Мах	Unit	Notes
Memory bus clock frequency	200	400	MHz	1, 2, 3, 4

Notes:

- 1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," Section 19.3, "e500 Core PLL Ratio," and Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
- 2. The Memory bus clock refers to the MPC8572E memory controllers' Dn_MCK[0:5] and Dn_MCK[0:5] output clocks, running at half of the DDR data rate.
- 3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
- 4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio." The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

As a general guideline when selecting the DDR data rate or platform (CCB) frequency, the following procedures can be used:

- Start with the processor core frequency selection;
- After the processor core frequency is determined, select the platform (CCB) frequency from the limited options listed in Table 80 and Table 81;
- Check the CCB to SYSCLK ratio to verify a valid ratio can be choose from Table 79;
- If the desired DDR data rate can be same as the CCB frequency, use the synchronous DDR mode; Otherwise, if a higher DDR data rate is desired, use asynchronous mode by selecting a valid DDR data rate to DDRCLK ratio from Table 82. Note that in asynchronous mode, the DDR data rate must be greater than the platform (CCB) frequency. In other words, running DDR data rate lower than the platform (CCB) frequency in asynchronous mode is not supported by MPC8572E.
- Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 79:

- SYSCLK input signal
- Binary value on LA[29:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that, in synchronous mode, the DDR data rate is the determining factor in selecting the CCB bus frequency, because the CCB frequency must equal the DDR data rate. In asynchronous mode, the memory bus clock frequency is decoupled from the CCB bus frequency.



21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8572E.

21.1 System Clocking

The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 19.2, "CCB/SYSCLK PLL Ratio." The MPC8572E includes seven PLLs, with the following functions:

- Two core PLLs have ratios that are individually configurable. Each e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 19.3, "e500 Core PLL Ratio."
- The DDR complex PLL generates the clocking for the DDR controllers.
- The local bus PLL generates the clock for the local bus.
- The PLL for the SerDes1 module is used for PCI Express and Serial Rapid IO interfaces.
- The PLL for the SerDes2 module is used for the SGMII interface.

21.2 Power Supply Design

21.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins $(AV_{DD}PLAT, AV_{DD}CORE0, AV_{DD}CORE1, AV_{DD}DDR, AV_{DD}LBIU, AV_{DD}SRDS1 and AV_{DD}SRDS2 respectively).$ The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 62, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 1023 FC-PBGA footprint, without the inductance of vias.



System Design Information

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- TRST should be tied to HRESET through a 0 k Ω isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.



Document Revision History

Table 90.	. Document	Revision	History	(continued)
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Rev. Number	Date	Substantive Change(s)
6	06/2014	 Updated Table 76, "MPC8572E Pinout Listing," TDO signal is not driven during HRSET* assertion. In Table 86, "Part Numbering Nomenclature—Rev 2.2.1," added full Pb-free part code.
5	01/2011	 Editorial changes throughout Updated Table 4, "MPC8572E Power Dissipation," to include low power product. In Section 22.1, "Part Numbers Fully Addressed by this Document," defined PPC as "Prototype" and changed table headings to say "Package Sphere Type". Added Table 86, "Part Numbering Nomenclature—Rev 2.2.1."
4	06/2010	 In Section 18.3, "Pinout Listings," updated Table 76 showing GPINOUT power rail as BVDD. Updated Section 14.1, "GPIO DC Electrical Characteristics."
3	03/2010	 In Section 2.1, "Overall DC Electrical Characteristics," changed GPIO power from OVDD to BVDD. In Section 22.1, "Part Numbers Fully Addressed by this Document," added Table 87 for Rev 2.1 silicon. In Section 22.1, "Part Numbers Fully Addressed by this Document," updated Table 88 for Rev 1.1.1 silicon.
2	06/2009	 In Section 3, "Power Characteristics," updated CCB Max to 533MHz for 1200MHz core device in Table 5, "MPC8572EL Power Dissipation." In Section 4.4, "DDR Clock Timing," changed DDRCLK Max to 100MHz. This change was announced in Product Bulletin #13572. Clarified restrictions in Section 4.5, "Platform to eTSEC FIFO Restrictions." In Table 9, "RESET Initialization Timing Specifications," added note 2. Added Section 14, "GPIO." In Section 18.1, "Package Parameters for the MPC8572E FC-PBGA," updated material composition to 63% Sn, 37% Pb. In Section 18.2, "Mechanical Dimensions of the MPC8572E FC-PBGA, updated Figure 61 to correct the package thickness and top view. In Section 19.1, "Clock Ranges," updated CCB Max to 533MHz for 1200MHz core device in Table 77, "MPC8572E Processor Core Clocking Specifications." In Section 19.5.2, "Minimum Platform Frequency Requirements for High-Speed Interfaces," changed minimum CCB clock frequency for proper PCI Express operation. Added LPBSE to description of LGPL4/LGTA/LUPWAIT/LPBSE/LFRB signal in Table 76, "MPC8572E Pinout Listing." Corrected supply voltage for GPIO pins in Table 76, "MPC8572E Pinout Listing." Applied note to SD1_PLL_TPA in Table 76, "MPC8572E Pinout Listing." Added note for LAD pins in Table 76, "MPC8572E Pinout Listing." Updated Table 88, ",Part Numbering Nomenclature—Rev 1.1.1" with Rev 2.0 and Rev 2.1 part number information. Added note indicating that silicon version 2.0 is available for prototype purposes only and will not be available as a qualified device.
1	08/2008	• In Section 22.1, "Part Numbers Fully Addressed by this Document," added SVR information in, Table 88 "Part Numbering Nomenclature—Rev 1.1.1," for devices without Security Engine feature.
0	07/2008	Initial release.



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Document Number: MPC8572EEC Rev. 7 03/2016



