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Understanding Embedded - Microprocessors

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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572clvtavne

Email: info@E-XFL.COM

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4 Input Clocks

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8572E.

Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
SYSCLK frequency	f _{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t _{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t _{KHK} /tsysclk	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5, 6

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.

- 2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- 6. For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on SYSCLK.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.



DDR2 and DDR3 SDRAM Controller

Table 17. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t _{CISKEW}	-	-	ps	1, 2
800 MHz	—	-200	200	—	—
667 MHz	—	-240	240	—	—
533 MHz	—	-300	300	—	—
400 MHz	—	-365	365	—	—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.

 The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called tDISKEW. This can be determined by the following equation: tDISKEW =+/-(T/4 – abs(tCISKEW)) where T is the clock period and abs(tCISKEW) is the absolute value of tCISKEW.

Figure 3 shows the DDR2 and DDR3 SDRAM interface input timing diagram.



Figure 3. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

Table 18 contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time	t _{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t _{DDKHAS}			ns	3



Figure 9 shows the GMII transmit AC timing diagram.



Figure 9. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock period	t _{GRX}	_	8.0	_	ns
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40	_	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0	_	_	ns
RX_CLK clock rise (20%-80%)	t _{GRXR} 2	_	_	1.0	ns
RX_CLK clock fall time (80%-20%)	t _{GRXF} 2			1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

2. Guaranteed by design.

Figure 10 provides the AC test load for eTSEC.



MPC8572E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 7



Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

Figure 14 shows the MII receive AC timing diagram.



Figure 14. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 31 provides the TBI transmit AC timing specifications.

Table 31. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t _{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t _{TTKHDX}	1.0	—	—	ns
GTX_CLK rise (20%-80%)	t _{TTXR} ²	_	—	1.0	ns
GTX_CLK fall time (80%–20%)	t _{TTXF} ²	_	_	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.



Ethernet: Enhanced Three-Speed Ethernet (eTSEC)





Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

Table 35 shows the RMII transmit AC timing specifications.

Table 35. RMII Transmit AC Timing Specifications

```
At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V \pm 5%.
```

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TSECn_TX_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t _{RMTH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t _{RMTJ}	—	—	250	ps
Rise time TSECn_TX_CLK (20%-80%)	t _{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t _{RMTF}	1.0	—	2.0	ns



Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

Table 36. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_DD/TV_DD of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RXD[1:0], CRS_DV, RX_ER hold time to TSECn_TX_CLK rising edge	t _{RMRDX}	2.0	—	_	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 20 provides the AC test load for eTSEC.



Figure 20. eTSEC AC Test Load

Figure 21 shows the RMII receive AC timing diagram.



Figure 21. RMII Receive AC Timing Diagram

8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes 2 interface of MPC8572E as shown in Figure 22, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50- Ω output impedance. Each input of the SerDes receiver differential pair features 50- Ω on-die termination to SGND_SRDS2 (xcorevss). The reference circuit of the SerDes transmitter and receiver is shown in Figure 54.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines



8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs ($SD2_TX[n]$ and $\overline{SD2_TX[n]}$) or at the receiver inputs ($SD2_RX[n]$ and $\overline{SD2_RX[n]}$) as depicted in Figure 25, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

Table 40 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 40. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.1V ± 5%.

Parameter	Symbol	Min	Тур	Мах	Unit	Notes
Deterministic Jitter	JD	—	_	0.17	UI p-p	_
Total Jitter	JT	—	_	0.35	UI p-p	_
Unit Interval	UI	799.92	800	800.08	ps	1
V _{OD} fall time (80%-20%)	tfall	50	—	120	ps	—
V _{OD} rise time (20%-80%)	t _{rise}	50	—	120	ps	—

Notes:

1. Each UI is 800 ps \pm 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

Table 41 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 24 shows the SGMII receiver input compliance mask eye diagram.

Table 41. SGMII Receive AC Timing Specifications

At recommended operating conditions with $XV_{DD_SRDS2} = 1.1V \pm 5\%$.

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	_	_	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	_	_	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	_	_	UI p-p	1
Total Jitter Tolerance	JT	0.65	_	_	UI p-p	1
Bit Error Ratio	BER	—	_	10 ⁻¹²	—	_
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C _{TX}	5	_	200	nF	3

Notes:

1. Measured at receiver.

2. Each UI is 800 ps \pm 100 ppm.

3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.

4. See RapidIO 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.



Local Bus Controller (eLBC)



Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)





Figure 34. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)



Table 58 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD} = 1.8 \text{ V DC}$. Table 58. GPIO DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 1.8V	BV _{DD}	1.71	1.89	V
High-level input voltage	V _{IH}	0.65 x BV _{DD}	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.35 x BV _{DD}	V
Input current ($BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	I _{IN}	TBD	TBD	μA
High-level output voltage $(I_{OH} = -100 \ \mu A)$	V _{OH}	BV _{DD} – 0.2	—	V
High-level output voltage $(I_{OH} = -2 \text{ mA})$	V _{OH}	BV _{DD} – 0.45	—	V
Low-level output voltage $(I_{OL} = 100 \ \mu A)$	V _{OL}	_	0.2	V
Low-level output voltage (I _{OL} = 2 mA)	V _{OL}	_	0.45	V

Note:

1. The symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1.

14.2 GPIO AC Electrical Specifications

Table 59 provides the GPIO input and output AC timing specifications.

Table 59. GPIO Input AC Timing Specifications¹

Parameter	Symbol	Тур	Unit	Notes
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns	2

Notes:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYSCLK. Timings are measured at the pin.
- 2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 42 provides the AC test load for the GPIO.





High-Speed Serial Interfaces (HSSI)

15 High-Speed Serial Interfaces (HSSI)

The MPC8572E features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface can be used for PCI Express and/or Serial RapidIO data transfers. The SerDes2 is dedicated for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 43 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and SDn_TX) or a receiver input (SDn_RX and $\overline{SDn_RX}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-Ended Swing

The transmitter output signals and the receiver input signals SDn_TX, SDn_TX, SDn_RX and SDn_RX each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. Differential Output Voltage, V_{OD} (or Differential Output Swing):

The Differential Output Voltage (or Swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential Input Voltage, V_{ID} (or Differential Input Swing):

The Differential Input Voltage (or Swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. Differential Peak-to-Peak, V_{DIFFp-p}

Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2*|(A – B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.



High-Speed Serial Interfaces (HSSI)

Figure 48 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8572E SerDes reference clock input's DC requirement.



Figure 48. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)



Characteristic	Symbol	Range		Unit	Notos	
Characteristic	Symbol	Min	Мах	Unit	NOLES	
Differential Input Voltage	V _{IN}	200	1600	mV p-p	Measured at receiver	
Deterministic Jitter Tolerance	J _D	0.37	—	UI p-p	Measured at receiver	
Combined Deterministic and Random Jitter Tolerance	J _{DR}	0.55	_	UI p-p	Measured at receiver	
Total Jitter Tolerance ¹	J _T	0.65	_	UI p-p	Measured at receiver	
Multiple Input Skew	S _{MI}	_	24	ns	Skew at the receiver input between lanes of a multilane link	
Bit Error Rate	BER	_	10 ⁻¹²	_	_	
Unit Interval	UI	800	800	ps	+/– 100 ppm	

Table 72. Receiver AC Timing Specifications—1.25 GBaud

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Characteristic	Symbol	Range		Unit	Notos	
Characteristic	Gymbol	Min	Мах	Unit	NOLES	
Differential Input Voltage	V _{IN}	200	1600	mV p-p	Measured at receiver	
Deterministic Jitter Tolerance	J _D	0.37	—	UI p-p	Measured at receiver	
Combined Deterministic and Random Jitter Tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver	
Total Jitter Tolerance ¹	J _T	0.65	_	UI p-p	Measured at receiver	
Multiple Input Skew	S _{MI}	_	24	ns	Skew at the receiver input between lanes of a multilane link	
Bit Error Rate	BER	—	10 ⁻¹²	—	—	
Unit Interval	UI	400	400	ps	+/– 100 ppm	

Table 73. Receiver AC Timing Specifications—2.5 GBaud

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.



Package Description

18.1 Package Parameters for the MPC8572E FC-PBGA

The package parameters are as provided in the following list. The package type is $33 \text{ mm} \times 33 \text{ mm}$, 1023 flip chip plastic ball grid array (FC-PBGA).

Package outline	33 mm × 33 mm
Interconnects	1023
Ball Pitch	1 mm
Ball Diameter (Typical)	0.6 mm
Solder Balls	63% Sn
	37% Pb
Solder Balls (Lead-Free)	96.5% Sn
	3.5% Ag



Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
D1_MCAS	Column Address Strobe	AC9	0	GV _{DD}	
D1_MRAS	Row Address Strobe	AB12	0	GV _{DD}	
D1_MCKE[0:3]	Clock Enable	M8, L9, T9, N8	0	GV _{DD}	11
D1_MCS[0:3]	Chip Select	AB9, AF10, AB11, AE11	0	GV _{DD}	_
D1_MCK[0:5]	Clock	V7, E13, AH11, Y9, F14, AG10	0	GV _{DD}	
D1_MCK[0:5]	Clock Complements	Y10, E12, AH12, AA11, F13, AG11	0	GV _{DD}	
D1_MODT[0:3]	On Die Termination	AD10, AF12, AC10, AE12	0	GV _{DD}	_
D1_MDIC[0:1]	Driver Impedance Calibration	E15, G14	I/O	GV _{DD}	25
	DDR SDRAM Mem	ory Interface 2		•	
D2_MDQ[0:63]	Data	A6, B7, C5, D5, A7, C8, D8, D6, C4, A3, D3, D2, B4, A4, B1, C1, E3, E1, G2, G6, D1, E4, G5, G3, J4, J2, P4, R5, H3, H1, N5, N3, Y6, Y4, AC3, AD2, V5, W5, AB2, AB3, AD5, AE3, AF6, AG7, AC4, AD4, AF4, AF7, AH5, AJ1, AL2, AM3, AH3, AH6, AM1, AL3, AK5, AL5, AJ7, AK7, AK4, AM4, AL6, AM7	I/O	GV _{DD}	_
D2_MECC[0:7]	Error Correcting Code	J5, H7, L7, N6, H4, H6, M4, M5	I/O	GV _{DD}	
D2_MAPAR_ERR	Address Parity Error	N1	Ι	GV _{DD}	
D2_MAPAR_OUT	Address Parity Out	W2	0	GV _{DD}	
D2_MDM[0:8]	Data Mask	A5, B3, F4, J1, AA4, AE5, AK1, AM5, K5	0	GV _{DD}	
D2_MDQS[0:8]	Data Strobe	B6, C2, F5, L4, AB5, AF3, AL1, AM6, L6	I/O	GV _{DD}	_
D2_MDQS[0:8]	Data Strobe	C7, A2, F2, K3, AA5, AE6, AK2, AJ6, K6	I/O	GV _{DD}	—
D2_MA[0:15]	Address	W1, U4, U3, T1, T2, T3, R1, R2, T5, R4, Y3, P1, N2, AF1, M2, M1	0	GV _{DD}	_

Table 76. MPC8572E Pinout Listing (continued)



Package Description

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes		
IRQ_OUT	Interrupt Output	U24	0	OV _{DD}	2, 4		
	1588						
TSEC_1588_CLK	Clock In	AM22	I	LV _{DD}	—		
TSEC_1588_TRIG_IN	Trigger In	AM23	I	LV _{DD}	—		
TSEC_1588_TRIG_OUT	Trigger Out	AA23	0	LV _{DD}	5, 9		
TSEC_1588_CLK_OUT	Clock Out	AC23	0	LV _{DD}	5, 9		
TSEC_1588_PULSE_OUT1	Pulse Out1	AA22	0	LV _{DD}	5, 9		
TSEC_1588_PULSE_OUT2	Pulse Out2	AB23	0	LV _{DD}	5, 9		
	Ethernet Managem	ent Interface 1					
EC1_MDC	Management Data Clock	AL30	0	LV _{DD}	5, 9		
EC1_MDIO	Management Data In/Out	AM25	I/O	LV _{DD}	—		
Ethernet Management Interface 3							
EC3_MDC	Management Data Clock	AF19	0	TV _{DD}	5, 9		
EC3_MDIO	Management Data In/Out	AF18	I/O	TV _{DD}			
Ethernet Management Interface 5							
EC5_MDC	Management Data Clock	AF14	0	TV _{DD}	21		
EC5_MDIO	Management Data In/Out	AF15	I/O	TV _{DD}	—		
	Gigabit Ethernet Ro	eference Clock					
EC_GTX_CLK125	Reference Clock	AM24	I	LV _{DD}	32		
Three-Speed Ethernet Controller 1							
TSEC1_RXD[7:0]/FIFO1_RXD[7:0]	Receive Data	AM28, AL28, AM26, AK23, AM27, AK26, AL29, AM30	I	LV _{DD}	1		
TSEC1_TXD[7:0]/FIFO1_TXD[7:0]	Transmit Data	AC20, AD20, AE22, AB22, AC22, AD21, AB21, AE21	0	LV _{DD}	1, 5, 9		
TSEC1_COL/FIFO1_TX_FC	Collision Detect/Flow Control	AJ23	I	LV _{DD}	1		
TSEC1_CRS/FIFO1_RX_FC	Carrier Sense/Flow Control	AM31	I/O	LV _{DD}	1, 16		
TSEC1_GTX_CLK	Transmit Clock Out	AK27	0	LV _{DD}			
TSEC1_RX_CLK/FIFO1_RX_C LK	Receive Clock	AL25	I	LV _{DD}	1		



Package Description

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes		
Power and Ground Signals							
GND	Ground	A18, A25, A29, C3, C6, C9, C12, C15, C20, C22, E5, E8, E11, E14, F3, G7, G10, G13, G16, H5, H21, J3, J9, J12, J18, K7, L5, L13, L15, L16, L21, M3, M9, M12, M14, M16, M18, N7, N13, N15, N17, N19, N21, N23, P5, P12, P14, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, R26, T7, T12, T14, T16, T18, T20, T22, T30, U5, U11, U13, U15, U16, U17, U19, U21, U23, U25, V3, V9, V12, V14, V16, V18, V20, V22, W7, W11, W13, W15, W17, W19, W21, W27, W32, Y5, Y12, Y14, Y16, Y18, Y20, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA30, AB7, AB26, AC5, AC11, AC13, AD3, AD9, AD14, AD17, AD22, AE7, AE13, AF5, AF11, AG3, AG9, AG15, AG19, AH7, AH13, AH22, AJ5, AJ11, AJ17, AK3, AK9, AK15, AK24, AL7, AL13, AL19, AL26					
XGND_SRDS1	SerDes Transceiver Pad GND (xpadvss)	C23, C27, D23, D25, E23, E26, F23, F24, G23, G27, H23, H25, J23, J26, K23, K24, L27, M25	_				
XGND_SRDS2	SerDes Transceiver Pad GND (xpadvss)	AD23, AD25, AE23, AE27, AF23, AF24, AG23, AG26, AH23, AH25, AJ27	_	_			

Table 76. MPC8572E Pinout Listing (continued)



Clocking

Binary Value of LA[29:31] Signals	CCB:SYSCLK Ratio
000	4:1
001	5:1
010	6:1
011	8:1
100	10:1
101	12:1
110	Reserved
111	Reserved

Table 79. CCB Clock Ratio

19.3 e500 Core PLL Ratio

The clock speed for each e500 core can be configured differently, determined by the values of various signals at power up.

Table 80 describes the clock ratio between e500 Core0 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LBCTL, LALE and LGPL2/LOE/LFRE at power up, as shown in Table 80.

Binary Value of LBCT <u>L, LALE,</u> LGPL2/LOE/LFRE Signals	e500 Core0:CCB Clock Ratio	Binary Value of LBCT <u>L, LALE,</u> LGPL2/LOE/LFRE Signals	e500 Core0:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

Table 80. e500 Core0 to CCB Clock Ratio



System Design Information

Figure 62 shows the PLL power supply filter circuits.



Figure 62. PLL Power Supply Filter Circuit

NOTE

It is recommended to have the minimum number of vias in the AV_{DD} trace for board layout. For example, zero vias might be possible if the AV_{DD} filter is placed on the component side. One via might be possible if it is placed on the opposite of the component side. Additionally, all traces for AV_{DD} and the filter components should be low impedance, 10 to 15 mils wide and short. This includes traces going to GND and the supply rails they are filtering.

The AV_{DD}_SRDSn signal provides power for the analog portions of the SerDesn PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDSn ball to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDSn ball. The 0.003- μ F capacitor is closest to the ball, followed by the two 2.2 μ F capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDSn to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 63. SerDes PLL Power Supply Filter

NOTE

AV_{DD}_SRDSn should be a filtered version of SV_{DD}_SRDSn.

NOTE

Signals on the SerDesn interface are fed from the XV_{DD} -SRDS*n* power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads.



System Design Information

21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8572E requires weak pull-up resistors (2–10 k Ω is recommended) on open drain type pins including I²C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must NOT be pulled down during power-on reset: DMA_DACK[0:1], EC5_MDC, HRESET_REQ, TRIG_OUT/READY_P0/QUIESCE, MSRCID[2:4], MDVAL, and ASLEEP. The TEST_SEL pin must be set to a proper state during POR configuration. For more details, refer to the pinlist table of the individual device.

21.7 Output Buffer DC Impedance

The MPC8572E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 64). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.



Figure 64. Driver Impedance Measurement