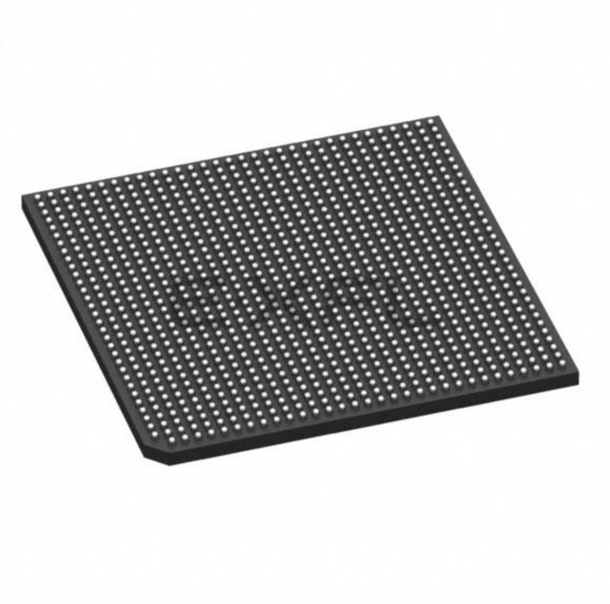

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8572ecpxaulb

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

<table>
<tr><th colspan="2">Characteristic</th><th>Symbol</th><th>Range</th><th>Unit</th><th>Notes</th></tr>
<tr><td colspan="2">Core supply voltage</td><td>V_{DD}</td><td>–0.3 to 1.21</td><td>V</td><td>—</td></tr>
<tr><td colspan="2">PLL supply voltage</td><td>AV_{DD}</td><td>–0.3 to 1.21</td><td>V</td><td>—</td></tr>
<tr><td colspan="2">Core power supply for SerDes transceivers</td><td>SV_{DD}</td><td>–0.3 to 1.21</td><td>V</td><td>—</td></tr>
<tr><td colspan="2">Pad power supply for SerDes transceivers</td><td>XV_{DD}</td><td>–0.3 to 1.21</td><td>V</td><td>—</td></tr>
<tr><td rowspan="2">DDR SDRAM Controller I/O supply voltage</td><td>DDR2 SDRAM Interface</td><td>GV_{DD}</td><td>–0.3 to 1.98</td><td rowspan="2">V</td><td>—</td></tr>
<tr><td>DDR3 SDRAM Interface</td><td>—</td><td>–0.3 to 1.65</td><td>—</td></tr>
<tr><td colspan="2" rowspan="2">Three-speed Ethernet I/O, FEC management interface, MII management voltage</td><td>LV_{DD} (for eTSEC1 and eTSEC2)</td><td>–0.3 to 3.63
–0.3 to 2.75</td><td>V</td><td>2</td></tr>
<tr><td>TV_{DD} (for eTSEC3 and eTSEC4, FEC)</td><td>–0.3 to 3.63
–0.3 to 2.75</td><td>—</td><td>2</td></tr>
<tr><td colspan="2">DUART, system control and power management, I[2]C, and JTAG I/O voltage</td><td>OV_{DD}</td><td>–0.3 to 3.63</td><td>V</td><td>—</td></tr>
<tr><td colspan="2">Local bus and GPIO I/O voltage</td><td>BV_{DD}</td><td>–0.3 to 3.63
–0.3 to 2.75
–0.3 to 1.98</td><td>V</td><td>—</td></tr>
<tr><td rowspan="5">Input voltage</td><td>DDR2 and DDR3 SDRAM interface signals</td><td>MV_{IN}</td><td>–0.3 to (GV_{DD} + 0.3)</td><td>V</td><td>3</td></tr>
<tr><td>DDR2 and DDR3 SDRAM interface reference</td><td>$MV_{REF}n$</td><td>–0.3 to (GV_{DD}/2 + 0.3)</td><td>V</td><td>—</td></tr>
<tr><td>Three-speed Ethernet signals</td><td>LV_{IN}
TV_{IN}</td><td>–0.3 to (LV_{DD} + 0.3)
–0.3 to (TV_{DD} + 0.3)</td><td>V</td><td>3</td></tr>
<tr><td>Local bus and GPIO signals</td><td>BV_{IN}</td><td>–0.3 to (BV_{DD} + 0.3)</td><td>—</td><td>—</td></tr>
<tr><td>DUART, SYSCLK, system control and power management, I[2]C, and JTAG signals</td><td>OV_{IN}</td><td>–0.3 to (OV_{DD} + 0.3)</td><td>V</td><td>3</td></tr>
<tr><td colspan="2">Storage temperature range</td><td>T_{STG}</td><td>–55 to 150</td><td>°C</td><td>—</td></tr>
</table>

Notes:

1. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,” for details on the recommended operating conditions per protocol.
3. (M,L,O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

Table 8. DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK jitter	—	—	—	+/– 150	ps	4, 5, 6

Notes:

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
6. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

> FIFO TX/RX clock frequency <= platform clock (CCB) frequency/4.2
>
> For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

> FIFO TX/RX clock frequency <= platform clock (CCB) frequency/3.2
>
> For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

5 RESET Initialization

Table 9 describes the AC electrical specifications for the RESET initialization timing.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	2
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1

Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics (continued)

Parameters	Symbol	Min	Max	Unit	Notes
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	μA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	3

Note:

1 LV_{DD} supports eTSECs 1 and 2.
2 TV_{DD} supports eTSECs 3 and 4 or FEC.
3 Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, because they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back on the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, because the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is a relationship between the maximum FIFO speed and the platform (CCB) frequency. For more information see Section 4.5, "Platform to eTSEC FIFO Restrictions."

Table 25 and Table 26 summarize the FIFO AC specifications.

Table 25. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period[1]	t_{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}/t_{FIT}	45	50	55	%

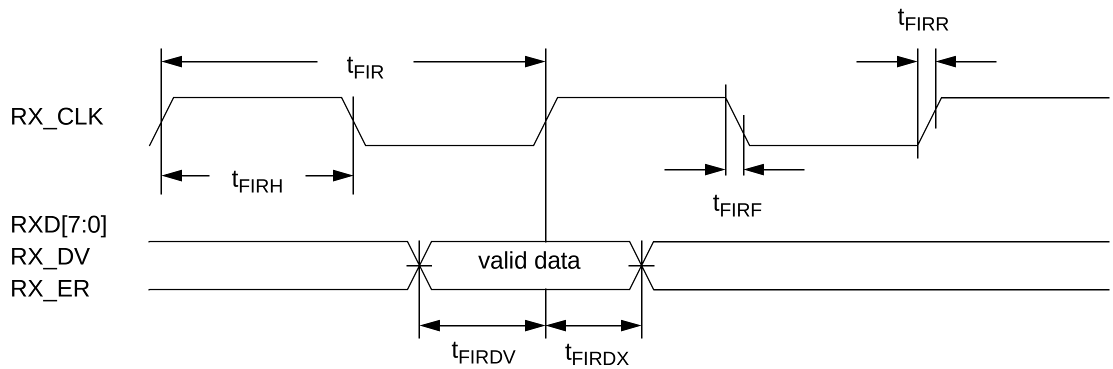

Figure 8. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

Table 27 provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t_{GTXR}[2]	—	—	1.0	ns
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 12 shows the MII transmit AC timing diagram.

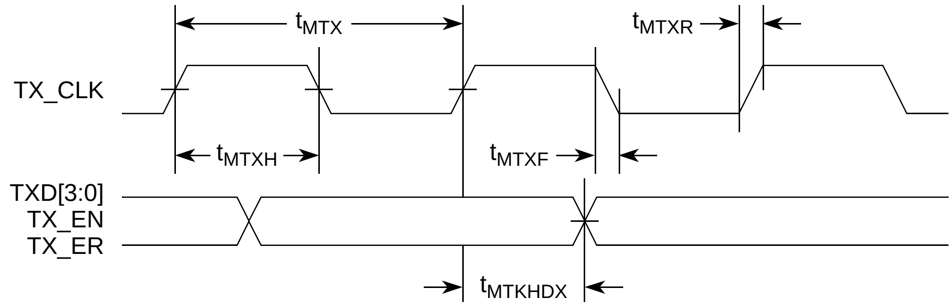

Figure 12. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX} [2]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{MRXR} [2]	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF} [2]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 13 provides the AC test load for eTSEC.

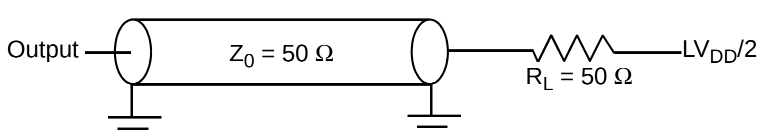

Figure 13. eTSEC AC Test Load

Table 36. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER hold time to TSECn_TX_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 20 provides the AC test load for eTSEC.

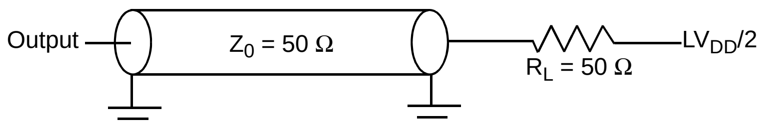

Figure 20. eTSEC AC Test Load

Figure 21 shows the RMII receive AC timing diagram.

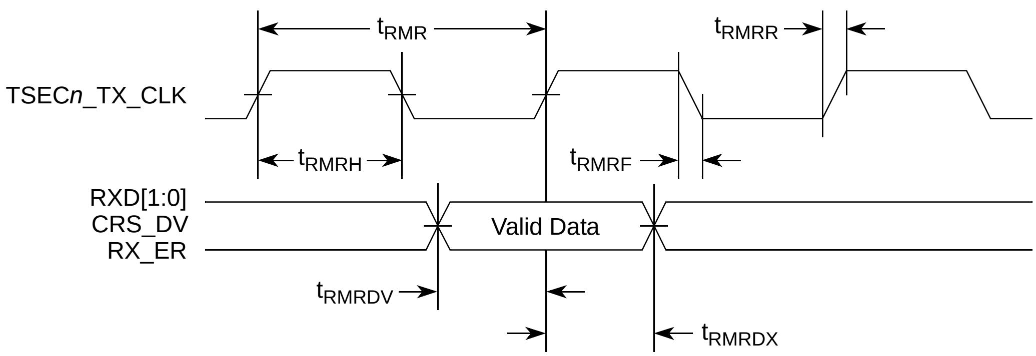

Figure 21. RMII Receive AC Timing Diagram

8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes 2 interface of MPC8572E as shown in Figure 22, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to SGND_SRDS2 (xcorevss). The reference circuit of the SerDes transmitter and receiver is shown in Figure 54.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines

8.4 eTSEC IEEE Std 1588™ AC Specifications

Figure 26 shows the data and command output timing diagram.

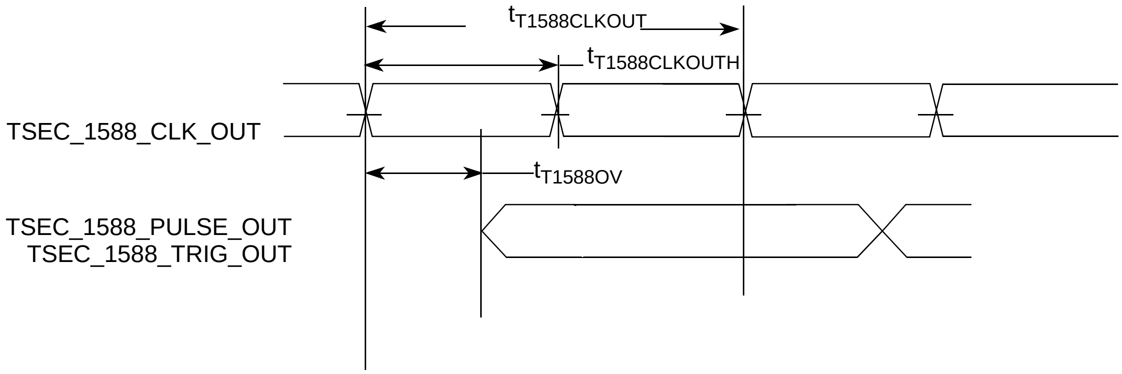

Figure 26. eTSEC IEEE 1588 Output AC Timing

[1] The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

Figure 27 shows the data and command input timing diagram.

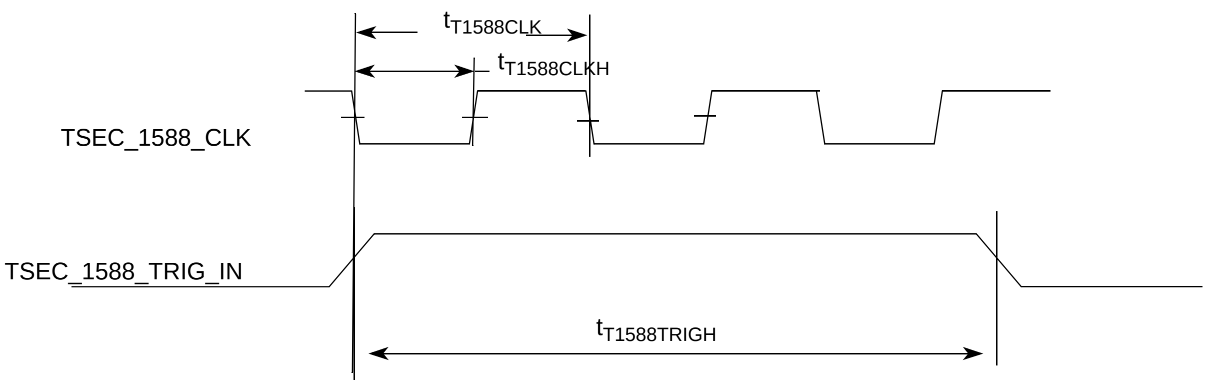

Figure 27. eTSEC IEEE 1588 Input AC timing

Table 42 provides the IEEE 1588 AC timing specifications.

Table 42. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.3	—	T_{TX_CLK}*9	ns	1
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2*$t_{T1588CLK}$	—	—	ns	—

Table 50. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)—PLL Enabled (continued)

At recommended operating conditions with BV_{DD} of 2.5 V ± 5% (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.4	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Table 51 describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC

Table 51. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)—PLL Enabled

At recommended operating conditions with BV_{DD} of 1.8 V ± 5%

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	6.67	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	2.4	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4

15.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, additionally to AC-coupling.

NOTE

Figure 48 to Figure 51 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8572E SerDes reference clock receiver requirement provided in this document.

16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 57.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

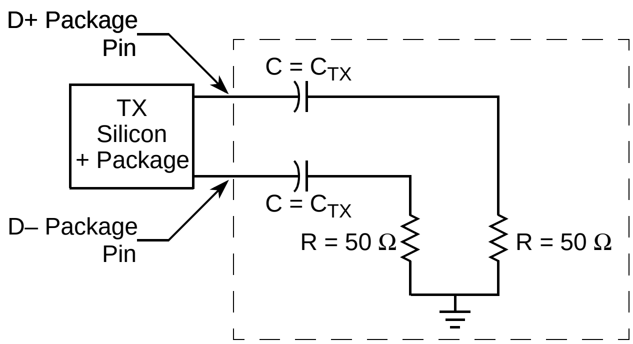

Figure 57. Compliance Test/Measurement Load

17 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8572E for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

17.1 DC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, “SerDes Reference Clocks.”

17.2 AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

Figure 64lists the AC requirements.

Table 64. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics.” The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

17.5 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Table 65. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{D1\_MCAS}}$	Column Address Strobe	AC9	O	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	Row Address Strobe	AB12	O	GV_{DD}	—
D1_MCKE[0:3]	Clock Enable	M8, L9, T9, N8	O	GV_{DD}	11
$\overline{\text{D1\_MCS}}$[0:3]	Chip Select	AB9, AF10, AB11, AE11	O	GV_{DD}	—
D1_MCK[0:5]	Clock	V7, E13, AH11, Y9, F14, AG10	O	GV_{DD}	—
$\overline{\text{D1\_MCK}}$[0:5]	Clock Complements	Y10, E12, AH12, AA11, F13, AG11	O	GV_{DD}	—
D1_MODT[0:3]	On Die Termination	AD10, AF12, AC10, AE12	O	GV_{DD}	—
D1_MDIC[0:1]	Driver Impedance Calibration	E15, G14	I/O	GV_{DD}	25
DDR SDRAM Memory Interface 2					
D2_MDQ[0:63]	Data	A6, B7, C5, D5, A7, C8, D8, D6, C4, A3, D3, D2, B4, A4, B1, C1, E3, E1, G2, G6, D1, E4, G5, G3, J4, J2, P4, R5, H3, H1, N5, N3, Y6, Y4, AC3, AD2, V5, W5, AB2, AB3, AD5, AE3, AF6, AG7, AC4, AD4, AF4, AF7, AH5, AJ1, AL2, AM3, AH3, AH6, AM1, AL3, AK5, AL5, AJ7, AK7, AK4, AM4, AL6, AM7	I/O	GV_{DD}	—
D2_MECC[0:7]	Error Correcting Code	J5, H7, L7, N6, H4, H6, M4, M5	I/O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	Address Parity Error	N1	I	GV_{DD}	—
D2_MAPAR_OUT	Address Parity Out	W2	O	GV_{DD}	—
D2_MDM[0:8]	Data Mask	A5, B3, F4, J1, AA4, AE5, AK1, AM5, K5	O	GV_{DD}	—
D2_MDQS[0:8]	Data Strobe	B6, C2, F5, L4, AB5, AF3, AL1, AM6, L6	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS}}$[0:8]	Data Strobe	C7, A2, F2, K3, AA5, AE6, AK2, AJ6, K6	I/O	GV_{DD}	—
D2_MA[0:15]	Address	W1, U4, U3, T1, T2, T3, R1, R2, T5, R4, Y3, P1, N2, AF1, M2, M1	O	GV_{DD}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
D2_MBA[0:2]	Bank Select	Y1, W3, P3	O	GV_{DD}	—
D2_MWE	Write Enable	AA2	O	GV_{DD}	—
D2_MCAS	Column Address Strobe	AD1	O	GV_{DD}	—
D2_MRAS	Row Address Strobe	AA1	O	GV_{DD}	—
D2_MCKE[0:3]	Clock Enable	L3, L1, K1, K2	O	GV_{DD}	11
D2_MCS[0:3]	Chip Select	AB1, AG2, AC1, AH2	O	GV_{DD}	—
D2_MCK[0:5]	Clock	V4, F7, AJ3, V2, E7, AG4	O	GV_{DD}	—
D2_MCK[0:5]	Clock Complements	V1, F8, AJ4, U1, E6, AG5	O	GV_{DD}	—
D2_MODT[0:3]	On Die Termination	AE1, AG1, AE2, AH1	O	GV_{DD}	—
D2_MDIC[0:1]	Driver Impedance Calibration	F1, G1	I/O	GV_{DD}	25
Local Bus Controller Interface					
LAD[0:31]	Muxed Data/Address	M22, L22, F22, G22, F21, G21, E20, H22, K22, K21, H19, J20, J19, L20, M20, M19, E22, E21, L19, K19, G19, H18, E18, G18, J17, K17, K14, J15, H16, J14, H15, G15	I/O	BV_{DD}	34
LDP[0:3]	Data Parity	M21, D22, A24, E17	I/O	BV_{DD}	—
LA[27]	Burst Address	J21	O	BV_{DD}	5, 9
LA[28:31]	Port Address	F20, K18, H20, G17	O	BV_{DD}	5, 7, 9
LCS[0:4]	Chip Selects	B23, E16, D20, B25, A22	O	BV_{DD}	10
LCS[5]/DMA2_DREQ[1]	Chip Selects / DMA Request	D19	I/O	BV_{DD}	1, 10
LCS[6]/DMA2_DACK[1]	Chip Selects / DMA Ack	E19	O	BV_{DD}	1, 10
LCS[7]/DMA2_DDONE[1]	Chip Selects / DMA Done	C21	O	BV_{DD}	1, 10
LWE[0]/LBS[0]/LFWE	Write Enable / Byte Select	D17	O	BV_{DD}	5, 9
LWE[1]/LBS[1]	Write Enable / Byte Select	F15	O	BV_{DD}	5, 9
LWE[2]/LBS[2]	Write Enable / Byte Select	B24	O	BV_{DD}	5, 9
LWE[3]/LBS[3]	Write Enable / Byte Select	D18	O	BV_{DD}	5, 9
LALE	Address Latch Enable	F19	O	BV_{DD}	5, 8, 9
LBCTL	Buffer Control	L18	O	BV_{DD}	5, 8, 9

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD1_RX[7:0]	Receive Data (positive)	P32, N30, M32, L30, G30, F32, E30, D32	I	XV_{DD_SRDS1}	—
$\overline{\text{SD1\_RX}}$[7:0]	Receive Data (negative)	P31, N29, M31, L29, G29, F31, E29, D31	I	XV_{DD_SRDS1}	—
SD1_TX[7]	PCIe1 Tx Data Lane 7 / SRIO or PCIe2 Tx Data Lane 3 / PCIe3 TX Data Lane 1	M26	O	XV_{DD_SRDS1}	—
SD1_TX[6]	PCIe1 Tx Data Lane 6 / SRIO or PCIe2 Tx Data Lane 2 / PCIe3 TX Data Lane 0	L24	O	XV_{DD_SRDS1}	—
SD1_TX[5]	PCIe1 Tx Data Lane 5 / SRIO or PCIe2 Tx Data Lane 1	K26	O	XV_{DD_SRDS1}	—
SD1_TX[4]	PCIe1 Tx Data Lane 4 / SRIO or PCIe2 Tx Data Lane 0	J24	O	XV_{DD_SRDS1}	—
SD1_TX[3]	PCIe1 Tx Data Lane 3	G24	O	XV_{DD_SRDS1}	—
SD1_TX[2]	PCIe1 Tx Data Lane 2	F26	O	XV_{DD_SRDS1}	—
SD1_TX[1]	PCIe1 Tx Data Lane 1]	E24	O	XV_{DD_SRDS1}	—
SD1_TX[0]	PCIe1 Tx Data Lane 0	D26	O	XV_{DD_SRDS1}	—
$\overline{\text{SD1\_TX}}$[7:0]	Transmit Data (negative)	M27, L25, K27, J25, G25, F27, E25, D27	O	XV_{DD_SRDS1}	—
SD1_PLL_TPD	PLL Test Point Digital	J32	O	XV_{DD_SRDS1}	17
SD1_REF_CLK	PLL Reference Clock	H32	I	XV_{DD_SRDS1}	—
$\overline{\text{SD1\_REF\_CLK}}$	PLL Reference Clock Complement	H31	I	XV_{DD_SRDS1}	—
Reserved	—	C29, K32	—	—	26
Reserved	—	C30, K31	—	—	27
Reserved	—	C24, C25, H26, H27	—	—	28
Reserved	—	AL20, AL21	—	—	29
SerDes (x4) SGMII					
SD2_RX[3:0]	Receive Data (positive)	AK32, AJ30, AF30, AE32	I	XV_{DD_SRDS2}	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Signals					
GND	Ground	A18, A25, A29, C3, C6, C9, C12, C15, C20, C22, E5, E8, E11, E14, F3, G7, G10, G13, G16, H5, H21, J3, J9, J12, J18, K7, L5, L13, L15, L16, L21, M3, M9, M12, M14, M16, M18, N7, N13, N15, N17, N19, N21, N23, P5, P12, P14, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, R26, T7, T12, T14, T16, T18, T20, T22, T30, U5, U11, U13, U15, U16, U17, U19, U21, U23, U25, V3, V9, V12, V14, V16, V18, V20, V22, W7, W11, W13, W15, W17, W19, W21, W27, W32, Y5, Y12, Y14, Y16, Y18, Y20, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA30, AB7, AB26, AC5, AC11, AC13, AD3, AD9, AD14, AD17, AD22, AE7, AE13, AF5, AF11, AG3, AG9, AG15, AG19, AH7, AH13, AH22, AJ5, AJ11, AJ17, AK3, AK9, AK15, AK24, AL7, AL13, AL19, AL26	—	—	—
XGND_SRDS1	SerDes Transceiver Pad GND (xpadvss)	C23, C27, D23, D25, E23, E26, F23, F24, G23, G27, H23, H25, J23, J26, K23, K24, L27, M25	—	—	—
XGND_SRDS2	SerDes Transceiver Pad GND (xpadvss)	AD23, AD25, AE23, AE27, AF23, AF24, AG23, AG26, AH23, AH25, AJ27	—	—	—

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD1_IMP_CAL_RX	SerDes1 Rx Impedance Calibration	B32	I	200Ω ($\pm 1\%$) to GND	—
SD1_IMP_CAL_TX	SerDes1 Tx Impedance Calibration	T32	I	100Ω ($\pm 1\%$) to GND	—
SD1_PLL_TPA	SerDes1 PLL Test Point Analog	J30	O	AVDD_SRDS analog	17
SD2_IMP_CAL_RX	SerDes2 Rx Impedance Calibration	AC32	I	200Ω ($\pm 1\%$) to GND	—
SD2_IMP_CAL_TX	SerDes2 Tx Impedance Calibration	AM32	I	100Ω ($\pm 1\%$) to GND	—
SD2_PLL_TPA	SerDes2 PLL Test Point Analog	AH30	O	AVDD_SRDS analog	17
TEMP_ANODE	Temperature Diode Anode	AA31	—	internal diode	14
TEMP_CATHODE	Temperature Diode Cathode	AB31	—	internal diode	14
No Connection Pins					

21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8572E requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must NOT be pulled down during power-on reset: $\overline{\text{DMA\_DACK[0:1]}}$, EC5_MDC, $\overline{\text{HRESET\_REQ}}$, TRIG_OUT/READY_P0/$\overline{\text{QUIESCE}}$, MSRCID[2:4], MDVAL, and ASLEEP. The $\overline{\text{TEST\_SEL}}$ pin must be set to a proper state during POR configuration. For more details, refer to the pinlist table of the individual device.

21.7 Output Buffer DC Impedance

The MPC8572E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 64). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

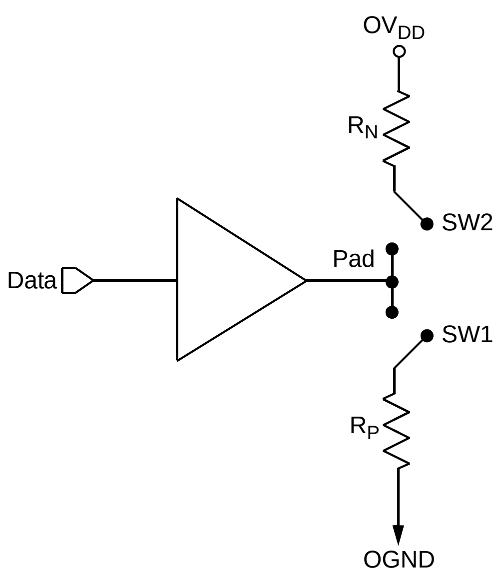

Figure 64. Driver Impedance Measurement

Table 85 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 85. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R_N	45 Target	18 Target (full strength mode) 36 Target (half strength mode)	Z_0	Ω
R_P	45 Target	18 Target (full strength mode) 36 Target (half strength mode)	Z_0	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

21.8 Configuration Pin Muxing

The MPC8572E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio, DDR complex PLL and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary

Table 90. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
6	06/2014	• Updated Table 76, “MPC8572E Pinout Listing,” TDO signal is not driven during HRSET* assertion. • In Table 86, “Part Numbering Nomenclature—Rev 2.2.1,“ added full Pb-free part code.
5	01/2011	• Editorial changes throughout • Updated Table 4, “MPC8572E Power Dissipation,” to include low power product. • In Section 22.1, “Part Numbers Fully Addressed by this Document,” defined PPC as “Prototype” and changed table headings to say “Package Sphere Type”. • Added Table 86, “Part Numbering Nomenclature—Rev 2.2.1.”
4	06/2010	• In Section 18.3, “Pinout Listings,” updated Table 76 showing GPINOUT power rail as BVDD. • Updated Section 14.1, “GPIO DC Electrical Characteristics.”
3	03/2010	• In Section 2.1, “Overall DC Electrical Characteristics,” changed GPIO power from OVDD to BVDD. • In Section 22.1, “Part Numbers Fully Addressed by this Document,” added Table 87 for Rev 2.1 silicon. • In Section 22.1, “Part Numbers Fully Addressed by this Document,” updated Table 88 for Rev 1.1.1 silicon.
2	06/2009	• In Section 3, “Power Characteristics,” updated CCB Max to 533MHz for 1200MHz core device in Table 5, “MPC8572EL Power Dissipation.” • In Section 4.4, “DDR Clock Timing,” changed DDRCLK Max to 100MHz. This change was announced in Product Bulletin #13572. • Clarified restrictions in Section 4.5, “Platform to eTSEC FIFO Restrictions.” • In Table 9, “RESET Initialization Timing Specifications,” added note 2. • Added Section 14, “GPIO.” • In Section 18.1, “Package Parameters for the MPC8572E FC-PBGA,” updated material composition to 63% Sn, 37% Pb. • In Section 18.2, “Mechanical Dimensions of the MPC8572E FC-PBGA, updated Figure 61 to correct the package thickness and top view. • In Section 19.1, “Clock Ranges,” updated CCB Max to 533MHz for 1200MHz core device in Table 77, “MPC8572E Processor Core Clocking Specifications.” • In Section 19.5.2, “Minimum Platform Frequency Requirements for High-Speed Interfaces,” changed minimum CCB clock frequency for proper PCI Express operation. • Added LPBSE to description of LGPL4/LGTA/LUPWAIT/LPBSE/LFRB signal in Table 76, “MPC8572E Pinout Listing.” • Corrected supply voltage for GPIO pins in Table 76, “MPC8572E Pinout Listing.” • Applied note to SD1_PLL_TPA in Table 76, “MPC8572E Pinout Listing.” • Updated note regarding MDIC in Table 76, “MPC8572E Pinout Listing.” • Added note for LAD pins in Table 76, “MPC8572E Pinout Listing.” • Updated Table 88, “,Part Numbering Nomenclature—Rev 1.1.1” with Rev 2.0 and Rev 2.1 part number information. Added note indicating that silicon version 2.0 is available for prototype purposes only and will not be available as a qualified device.
1	08/2008	• In Section 22.1, “Part Numbers Fully Addressed by this Document,” added SVR information in, Table 88 “Part Numbering Nomenclature—Rev 1.1.1,” for devices without Security Engine feature.
0	07/2008	• Initial release.