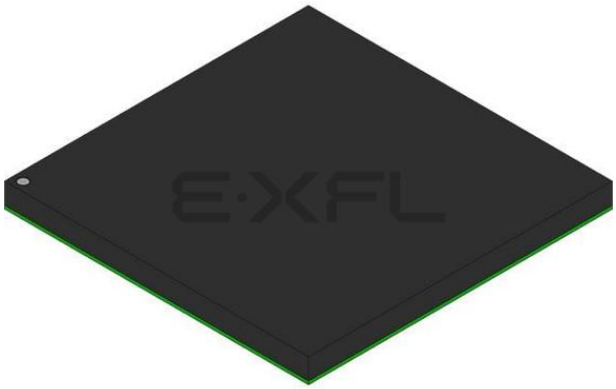

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8572ecpxauld

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Range	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage		AV_{DD}	–0.3 to 1.21	V	—
Core power supply for SerDes transceivers		SV_{DD}	–0.3 to 1.21	V	—
Pad power supply for SerDes transceivers		XV_{DD}	–0.3 to 1.21	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	–0.3 to 1.98	V	—
	DDR3 SDRAM Interface	—	–0.3 to 1.65		—
Three-speed Ethernet I/O, FEC management interface, MII management voltage		LV_{DD} (for eTSEC1 and eTSEC2) TV_{DD} (for eTSEC3 and eTSEC4, FEC)	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 3.63 –0.3 to 2.75	V — —	2 2
DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus and GPIO I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2 and DDR3 SDRAM interface signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2 and DDR3 SDRAM interface reference	$MV_{REF}n$	–0.3 to (GV_{DD}/2 + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	3
	Local bus and GPIO signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,” for details on the recommended operating conditions per protocol.
3. (M,L,O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-on reset, and extra current may be drawn by the device.

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with out the L in its part ordering is shown in Table 4.

Table 4. MPC8572E Power Dissipation [1]

CCB Frequency	Core Frequency	Typical-65[2]	Typical-105[3]	Maximum[4]	Unit
533	1067	12.3	17.8	18.5	W
533	1200	12.3	17.8	18.5	W
533	1333	16.3	22.8	24.5	W
600	1500	17.3	23.9	25.9	W

Notes:

1. This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.
2. Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.
3. Typical-105 is based on V_{DD} = 1.1 V, T_j = 105 °C, running Dhrystone.
4. Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with the L in its port ordering is shown in Table 5.

Table 5. MPC8572EL Power Dissipation [1]

CCB Frequency	Core Frequency	Typical-65[2]	Typical-105[3]	Maximum[4]	Unit
533	1067	12	15	15.8	W
533	1200	12	15.5	16.3	W
533	1333	12	15.9	16.9	W
600	1500	13	18.7	20.0	W

Notes:

1. This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.
2. Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.
3. Typical-105 is based on V_{DD} = 1.1 V, T_j = 105 °C, running Dhrystone.
4. Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8572E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3V ± 5% or 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time L/TV_{DD}=2.5V L/TV_{DD}=3.3V	t_{G125R}, t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2, 3

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for L/TV_{DD}=2.5V, and from 0.6V and 2.7V for L/TV_{DD}=3.3V.
2. Timing is guaranteed by design and characterization.
3. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC*n*_GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 DDR Clock Timing

Table 8 provides the DDR clock (DDRCLK) AC timing specifications for the MPC8572E.

Table 8. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	66	—	100	MHz	1
DDRCLK cycle time	t_{DDRCLK}	10.0	—	15.15	ns	—
DDRCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	3

Table 20 provides the differential specifications for the MPC8572E differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$ when in DDR3 mode.

Table 20. DDR3 SDRAM Differential Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
DC Input Signal Voltage	V_{IN}	—	—	mV	—
DC Differential Input Voltage	V_{ID}	—	—	mV	—
AC Differential Input Voltage	V_{IDAC}	—	—	mV	—
DC Differential Output Voltage	V_{OH}	—	—	mV	—
AC Differential Output Voltage	V_{OHAC}	—	—	mV	—
AC Differential Cross-point Voltage	V_{IXAC}	—	—	mV	—
Input Midpoint Voltage	V_{MP}	—	—	mV	—

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8572E.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1.

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1, 2
Maximum baud rate	f_{CCB}/16	baud	1, 2, 3
Oversample rate	16	—	1, 4

Notes:
1. Guaranteed by design
2. f_{CCB} refers to the internal platform clock frequency.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at both 2.5 V and 3.3V .

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 9, “Ethernet Management Interface Electrical Characteristics.”

The electrical characteristics for SGMII is specified in Section 8.3, “SGMII Interface Electrical Characteristics.” The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics (continued)

Parameters	Symbol	Min	Max	Unit	Notes
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	µA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	µA	3

Note:

1 LV_{DD} supports eTSECs 1 and 2.
2 TV_{DD} supports eTSECs 3 and 4 or FEC.
3 Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, because they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back on the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, because the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is a relationship between the maximum FIFO speed and the platform (CCB) frequency. For more information see Section 4.5, "Platform to eTSEC FIFO Restrictions."

Table 25 and Table 26 summarize the FIFO AC specifications.

Table 25. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period[1]	t_{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}/t_{FIT}	45	50	55	%

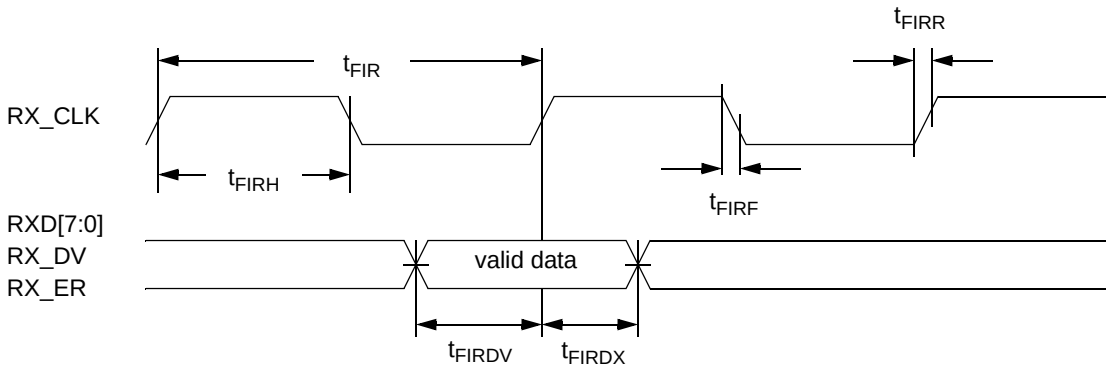

Figure 8. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

Table 27 provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t_{GTXR}[2]	—	—	1.0	ns
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 11 shows the GMII receive AC timing diagram.

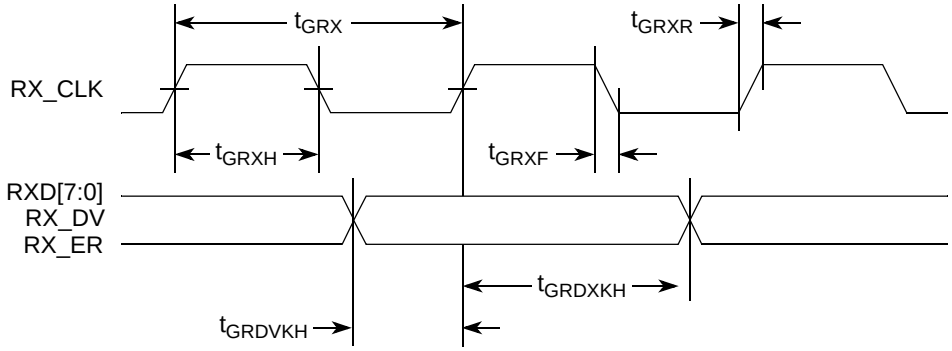

Figure 11. GMII Receive AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 29 provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}[2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t_{MTXR}[2]	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	t_{MTXF}[2]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Table 35. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 19 shows the RMII transmit AC timing diagram.

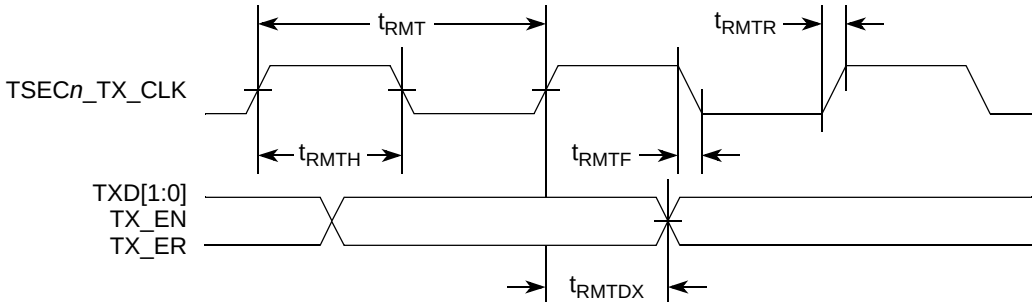

Figure 19. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 36 shows the RMII receive AC timing specifications.

Table 36. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_TX_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t_{RMRH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSECn_TX_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to TSECn_TX_CLK rising edge	t_{RMRDV}	4.0	—	—	ns

8.4 eTSEC IEEE Std 1588™ AC Specifications

Figure 26 shows the data and command output timing diagram.

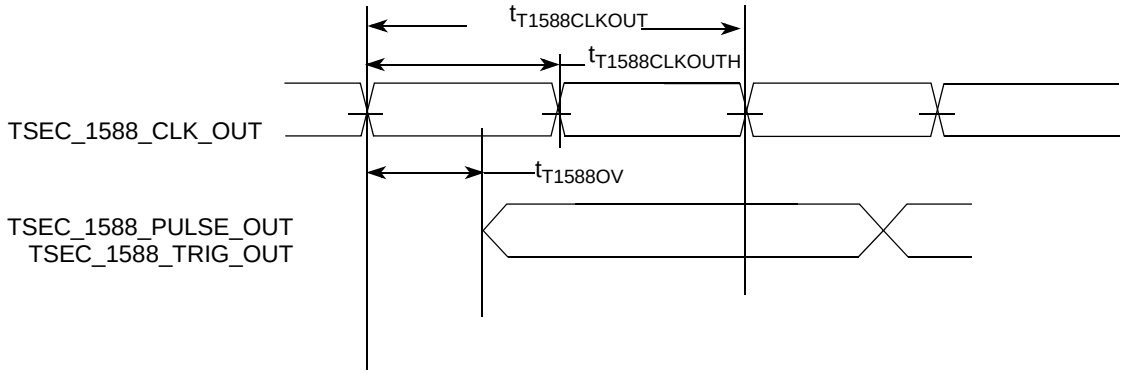

Figure 26. eTSEC IEEE 1588 Output AC Timing

1 The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

Figure 27 shows the data and command input timing diagram.

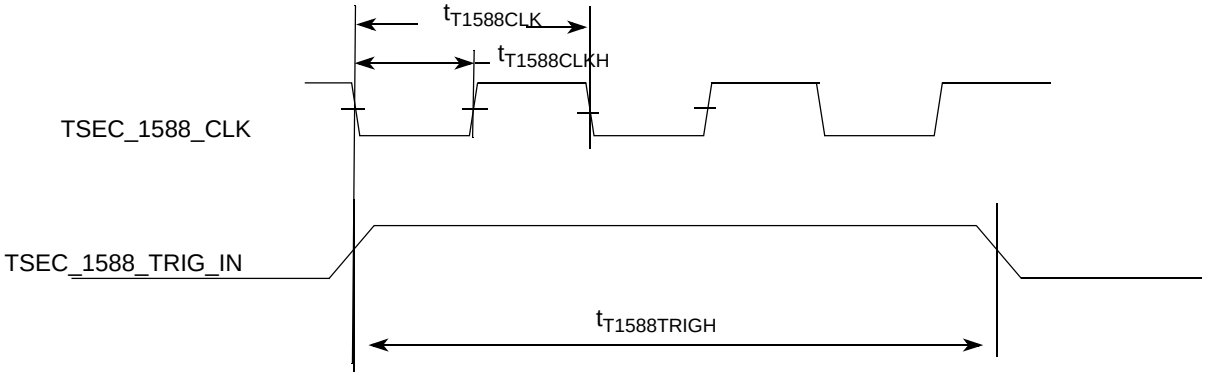

Figure 27. eTSEC IEEE 1588 Input AC timing

Table 42 provides the IEEE 1588 AC timing specifications.

Table 42. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.3	—	T_{TX_CLK}*9	ns	1
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2*$t_{T1588CLK}$	—	—	ns	—

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8572E.

14.1 GPIO DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the GPIO interface operating at BV_{DD} = 3.3 V DC.

Table 56. GPIO DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	BV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	BV_{DD} – 0.2	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:
1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

Table 57 provides the DC electrical characteristics for the GPIO interface operating at BV_{DD} = 2.5 V DC.

Table 57. GPIO DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5V	BV_{DD}	2.37	2.63	V
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.7	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IH}	—	10	μA
	I_{IL}		–15	
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	BV_{DD} + 0.3	V
Low-level output voltage (BV_{DD} min, I_{OL} = 1 mA)	V_{OL}	GND – 0.3	0.4	V

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

Figure 49 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Because LVDS clock driver's common mode voltage is higher than the MPC8572E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

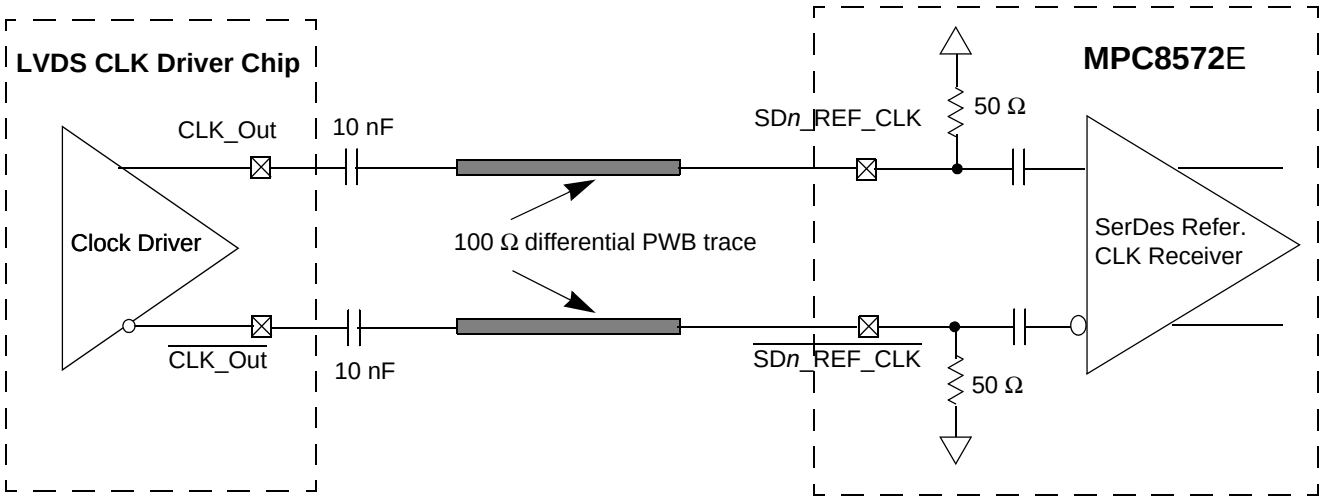

Figure 49. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 50 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Because LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8572E SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 50 assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8572E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Consult

clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

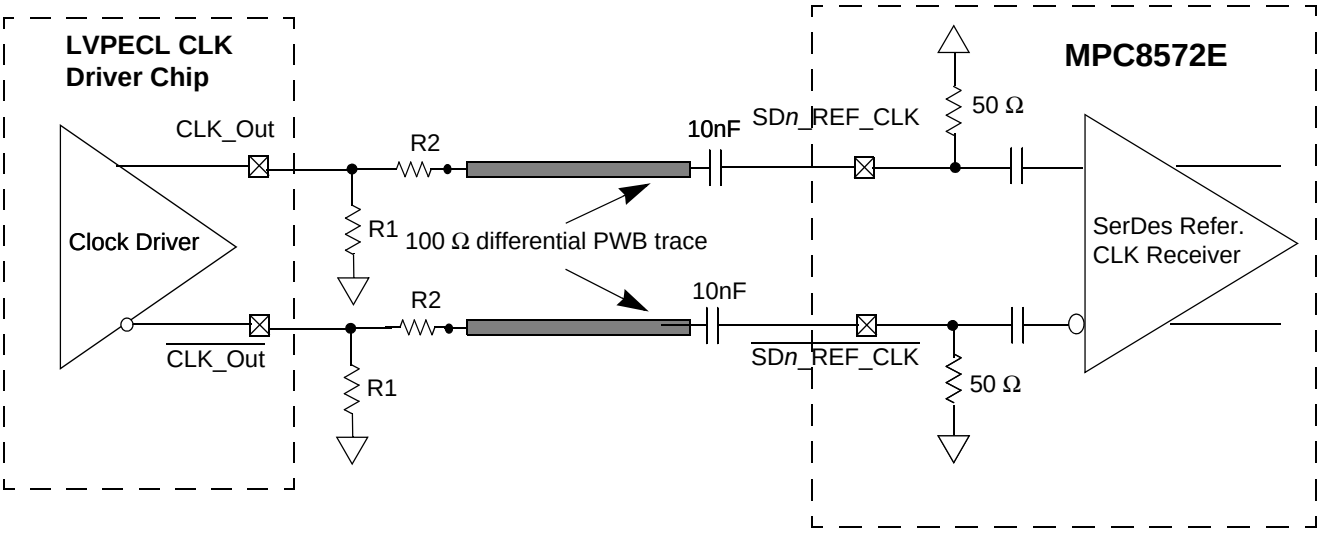

Figure 50. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 51 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8572E SerDes reference clock input's DC requirement.

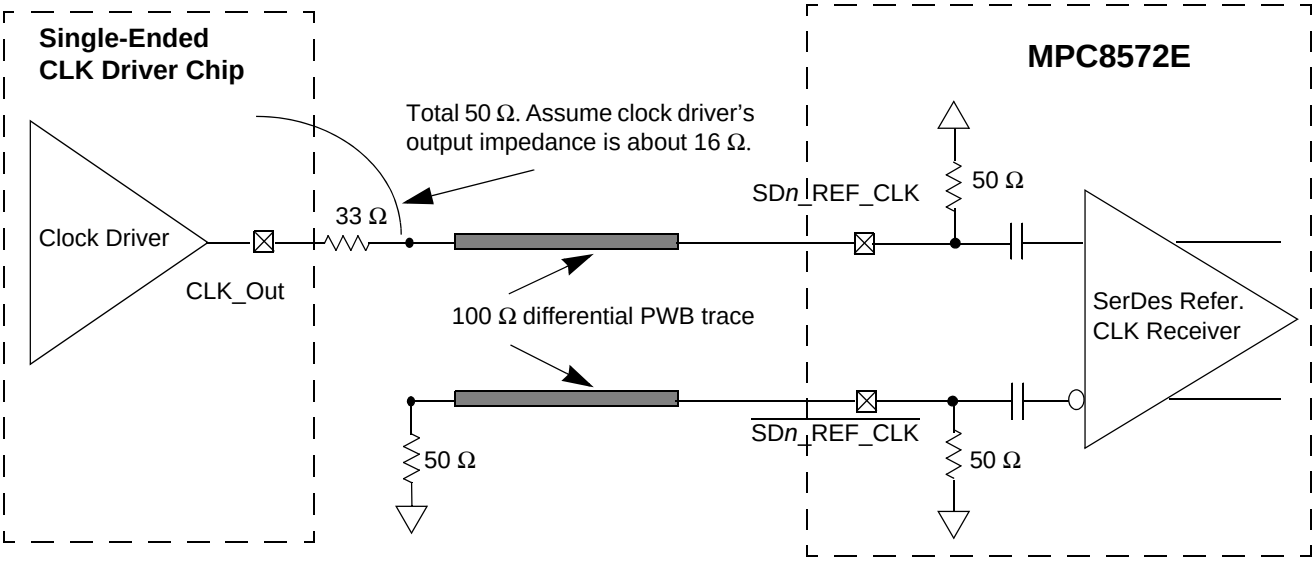

Figure 51. Single-Ended Connection (Reference Only)

15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and

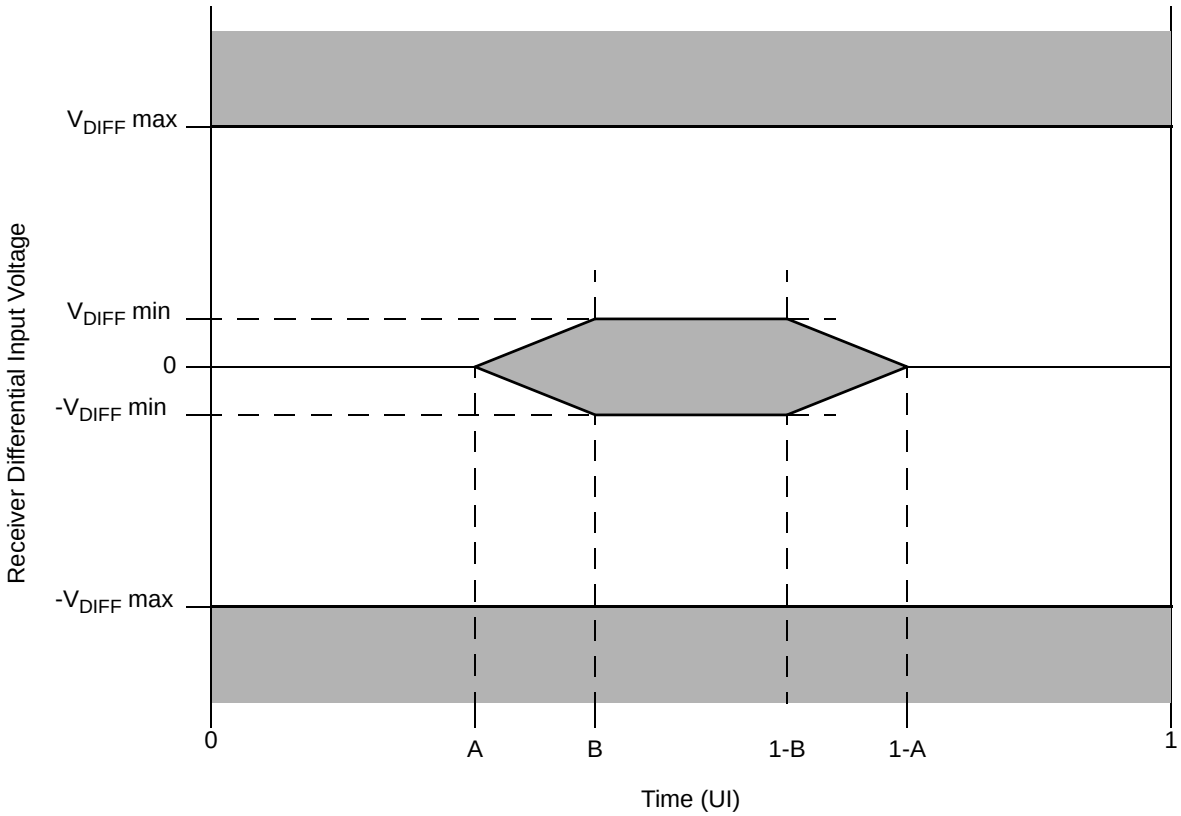

Figure 60. Receiver Input Compliance Mask

Table 75. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

17.8 Measurement and Test Requirements

Because the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

17.8.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial

Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LGPL0/LFCLE	UPM General Purpose Line 0 / Flash Command Latch Enable	J13	O	BV_{DD}	5, 9
LGPL1/$\overline{\text{LFALE}}$	UPM General Purpose Line 1/ Flash Address Latch Enable	J16	O	BV_{DD}	5, 9
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2 / Output Enable / Flash Read Enable	A27	O	BV_{DD}	5, 8, 9
LGPL3/$\overline{\text{LFWP}}$	UPM General Purpose Line 3 / Flash Write Protect	K16	O	BV_{DD}	5, 9
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE/LFRB	UPM General Purpose Line 4 / Target Ack / Wait / Parity Byte Select / Flash Ready-Busy	L17	I/O	BV_{DD}	—
LGPL5	UPM General Purpose Line 5 / Amux	B26	O	BV_{DD}	5, 9
LCLK[0:2]	Local Bus Clock	F17, F16, A23	O	BV_{DD}	—
LSYNC_IN	Local Bus DLL Synchronization	B22	I	BV_{DD}	—
LSYNC_OUT	Local Bus DLL Synchronization	A21	O	BV_{DD}	—
DMA					
$\overline{\text{DMA1\_DACK}}$[0:1]	DMA Acknowledge	W25, U30	O	OV_{DD}	21
$\overline{\text{DMA2\_DACK}}$[0]	DMA Acknowledge	AA26	O	OV_{DD}	5, 9
$\overline{\text{DMA1\_DREQ}}$[0:1]	DMA Request	Y29, V27	I	OV_{DD}	—
$\overline{\text{DMA2\_DREQ}}$[0]	DMA Request	V29	I	OV_{DD}	—
$\overline{\text{DMA1\_DDONE}}$[0:1]	DMA Done	Y28, V30	O	OV_{DD}	5, 9
$\overline{\text{DMA2\_DDONE}}$[0]	DMA Done	AA28	O	OV_{DD}	5, 9
$\overline{\text{DMA2\_DREQ}}$[2]	DMA Request	M23	I	BV_{DD}	—
Programmable Interrupt Controller					
$\overline{\text{UDE0}}$	Unconditional Debug Event Processor 0	AC25	I	OV_{DD}	—
$\overline{\text{UDE1}}$	Unconditional Debug Event Processor 1	AA25	I	OV_{DD}	—
$\overline{\text{MCP0}}$	Machine Check Processor 0	M28	I	OV_{DD}	—
$\overline{\text{MCP1}}$	Machine Check Processor 1	L28	I	OV_{DD}	—
IRQ[0:11]	External Interrupts	T24, R24, R25, R27, R28, AB27, AB28, P27, R30, AC28, R29, T31	I	OV_{DD}	—

Table 81 describes the clock ratio between e500 Core1 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LWE[0]/LBS[0]/LFWE, UART_SOUT[1], and READY_P1 signals at power up, as shown in Table 81.

Table 81. e500 Core1 to CCB Clock Ratio

Binary Value of LWE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio	Binary Value of LWE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

19.4 DDR/DDRCLK PLL Ratio

The dual DDR memory controller complexes can be synchronous with, or asynchronous to, the CCB, depending on configuration.

Table 82 describes the clock ratio between the DDR memory controller complexes and the DDR PLL reference clock, DDRCLK, which is not the memory bus clock. The DDR memory controller complexes clock frequency is equal to the DDR data rate.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for both DDR controllers to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 82 reflects the DDR data rate to DDRCLK ratio, because the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode. MPC8572E does not support running one DDR controller in synchronous mode and the other in asynchronous mode.

Table 82. DDR Clock Ratio

Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio
000	3:1
001	4:1
010	6:1
011	8:1
100	10:1

in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

See Section 20.4, "1x/4x LP-Serial Signal Descriptions," in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for Serial RapidIO interface width and frequency details.

20 Thermal

This section describes the thermal specifications of the MPC8572E.

Table 84 shows the thermal characteristics for the package, 1023 33 × 33 FC-PBGA.

The package uses a 29.6 × 29.6 mm lid that attaches to the substrate. Recommended maximum heat sink force is 10 pounds force (45 Newton).

Table 84. Package Thermal Characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer (1s)	$R_{\Theta JA}$	15	°C/W	1, 2
Junction to ambient, natural convection	Four-layer (2s2p)	$R_{\Theta JA}$	11	°C/W	1, 3
Junction to ambient (at 200 ft./min.)	Single-layer (1s)	$R_{\Theta JMA}$	11	°C/W	1, 3
Junction to ambient (ar 200 ft./min.)	Four-layer (2s2p)	$R_{\Theta JMA}$	8	°C/W	1, 3
Junction to board	—	$R_{\Theta JB}$	4	°C/W	4
Junction to case	—	$R_{\Theta JC}$	0.5	°C/W	5

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883, Method 1012.1).

20.1 Temperature Diode

The MPC8572E has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each MPC8572E device be calibrated.

The following are the specifications of the on-board temperature diode:

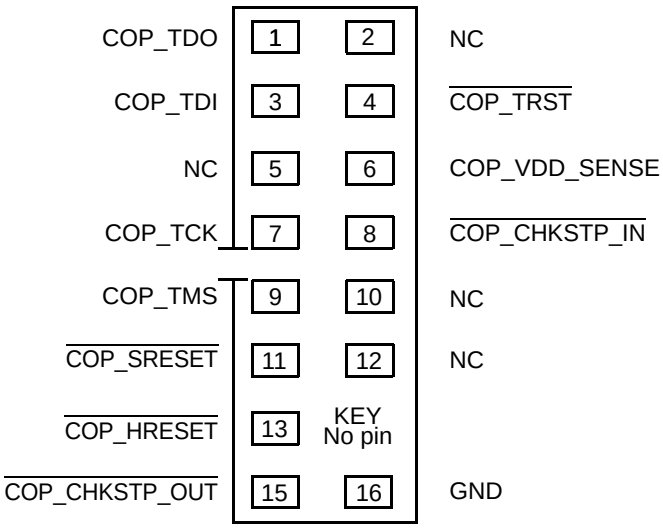

Figure 65. COP Connector Physical Pinout

21.10.3 SerDes 2 Interface (SGMII) Entirely Unused

If the high-speed SerDes 2 interface (SGMII) is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD2_TX[3:0]
- $\overline{\text{SD2\_TX}}$[3:0]
- Reserved pins: AF26, AF27

The following pins must be connected to XGND_SRDS2:

- SD2_RX[3:0]
- $\overline{\text{SD2\_RX}}$[3:0]
- SD2_REF_CLK
- $\overline{\text{SD2\_REF\_CLK}}$

The POR configuration pin cfg_srds_sgmii_en on $\overline{\text{UART\_RTS}}$[1] can be used to power down SerDes 2 block for power saving. Note that both SVDD_SRDS2 and XVDD_SRDS2 must remain powered.

21.10.4 SerDes 2 Interface (SGMII) Partly Unused

If only part of the high speed SerDes 2 interface (SGMII) pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD2_TX[3:0]
- $\overline{\text{SD2\_TX}}$[3:0]
- Reserved pins: AF26, AF27

The following pins must be connected to XGND_SRDS2:

- SD2_RX[3:0]
- $\overline{\text{SD2\_RX}}$[3:0]

[3] Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

22.2 Part Marking

Parts are marked as the example shown in Figure 67.

FC-PBGA

Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWW is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 67. Part Marking for FC-PBGA Device

Table 89 explains line four of Figure 67.

Table 89. Meaning of Last Line of Part Marking

Digit	Description
A	Assembly Site E Oak Hill Q KLM
WL	Lot number
YY	Year assembled
WW	Work week assembled

23 Document Revision History

Table 90 provides a revision history for the MPC8572E hardware specification.

Table 90. Document Revision History

Rev. Number	Date	Substantive Change(s)
7	03/2016	• Updated Section 22.2, “Part Marking,” changed the five-digit mask number to six digits.