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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

E·XFI

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BFBGA, FCBGA
Supplier Device Package	1023-FCBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8572ecpxavnd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

The Fast Ethernet Controller (FEC) operates in MII mode only, and complies with the AC and DC electrical characteristics specified in this chapter for MII. Note that if FEC is used, eTSEC 3 and 4 are only available in SGMII mode.

8.1.1 eTSEC DC Electrical Characteristics

All MII, GMII, RMII, and TBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. All RGMII, RTBI and FIFO drivers and receivers comply with the DC parametric attributes specified in Table 24. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV _{DD} TV _{DD}	3.13	3.47	V	1, 2
Output high voltage $(LV_{DD}/TV_{DD} = Min, IOH = -4.0 mA)$	VOH	2.40	LV _{DD} /TV _{DD} + 0.3	V	—
Output low voltage $(LV_{DD}/TV_{DD} = Min, IOL = 4.0 mA)$	VOL	GND	0.50	V	—
Input high voltage	V _{IH}	2.0	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	V _{IL}	-0.3	0.90	V	—
Input high current $(V_{IN} = LV_{DD}, V_{IN} = TV_{DD})$	IIH	_	40	μΑ	1, 2,3
Input low current (V _{IN} = GND)	Ι _{ΙL}	-600	_	μA	3

Table 23.	GMII.	MII. RMII.	and TBI DC	Electrical	Characteristics
	. ,	,		Liootiioui	0114140101101100

Notes:

¹ LV_{DD} supports eTSECs 1 and 2.

 2 TV_{DD} supports eTSECs 3 and 4 or FEC.

 3 The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1.

Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Мах	Unit	Notes
Supply voltage 2.5 V	LV _{DD/} TV _{DD}	2.37	2.63	V	1,2
Output high voltage ($LV_{DD}/TV_{DD} = Min, IOH = -1.0 mA$)	V _{OH}	2.00	$LV_{DD}/TV_{DD} + 0.3$	V	—
Output low voltage $(LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)$	V _{OL}	GND – 0.3	0.40	V	—
Input high voltage	V _{IH}	1.70	$LV_{DD}/TV_{DD} + 0.3$	V	—
Input low voltage	V _{IL}	-0.3	0.70	V	—



Figure 9 shows the GMII transmit AC timing diagram.



Figure 9. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock period	t _{GRX}	_	8.0	_	ns
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40	_	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0	_	_	ns
RX_CLK clock rise (20%-80%)	t _{GRXR} 2	_	_	1.0	ns
RX_CLK clock fall time (80%-20%)	t _{GRXF} 2			1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

2. Guaranteed by design.

Figure 10 provides the AC test load for eTSEC.



MPC8572E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 7



Ethernet: Enhanced Three-Speed Ethernet (eTSEC)





Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

Table 35 shows the RMII transmit AC timing specifications.

Table 35. RMII Transmit AC Timing Specifications

```
At recommended operating conditions with LV_{DD}/TV_{DD} of 2.5/ 3.3 V \pm 5%.
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Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TSECn_TX_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t _{RMTH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t _{RMTJ}	—	—	250	ps
Rise time TSECn_TX_CLK (20%-80%)	t _{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t _{RMTF}	1.0	—	2.0	ns



8.4 eTSEC IEEE Std 1588[™] AC Specifications

Figure 26 shows the data and command output timing diagram.



Figure 26. eTSEC IEEE 1588 Output AC Timing

¹ The output delay is count starting rising edge if t_{T1588CLKOUT} is non-inverting. Otherwise, it is count starting falling edge.

Figure 27 shows the data and command input timing diagram.





Table 42 provides the IEEE 1588 AC timing specifications.

Table 42. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with LV_{DD}/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Тур	Max	Unit	Note
TSEC_1588_CLK clock period	t _{T1588CLK}	3.3	—	T _{TX_CLK} *9	ns	1
TSEC_1588_CLK duty cycle	t _{T1588CLKH} /t _{T1588CLK}	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	t _{T1588CLKINJ}	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%-80%)	t _{T1588CLKINR}	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%-20%)	t _{T1588CLKINF}	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	t _{T1588} CLKOUT	2*t _{T1588CLK}	—	_	ns	_

MPC8572E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 7

NXP Semiconductors



Local Bus Controller (eLBC)



Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)



Local Bus Controller (eLBC)



Figure 35. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)



JTAG

Table 53. JTAG AC Timing Specifications (Independent of SYSCLK) ¹ (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{JTKLDZ} t _{JTKLOZ}	3 3	19 9	ns	5, 6

Notes:

 All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 36). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

- 2. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK} .
- 6. Guaranteed by design.

Figure 36 provides the AC test load for TDO and the boundary-scan outputs.



Figure 36. AC Test Load for the JTAG Interface

Figure 37 provides the JTAG clock input timing diagram.



Figure 37. JTAG Clock Input Timing Diagram

Figure 38 provides the $\overline{\text{TRST}}$ timing diagram.



High-Speed Serial Interfaces (HSSI)

15 High-Speed Serial Interfaces (HSSI)

The MPC8572E features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface can be used for PCI Express and/or Serial RapidIO data transfers. The SerDes2 is dedicated for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 43 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and SDn_TX) or a receiver input (SDn_RX and $\overline{SDn_RX}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-Ended Swing

The transmitter output signals and the receiver input signals SDn_TX, SDn_TX, SDn_RX and SDn_RX each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. Differential Output Voltage, V_{OD} (or Differential Output Swing):

The Differential Output Voltage (or Swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential Input Voltage, V_{ID} (or Differential Input Swing):

The Differential Input Voltage (or Swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. Differential Peak-to-Peak, V_{DIFFp-p}

Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2*|(A – B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.







16.4.3 Differential Receiver (RX) Input Specifications

Table 63 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Symbol	Parameter	Min	Nominal	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
V _{RX-DIFFp-p}	Differential Input Peak-to-Peak Voltage	0.175	_	1.200	V	$V_{RX-DIFFp-p} = 2^{*} V_{RX-D+} - V_{RX-D-} $ See Note 2.
T _{RX-EYE}	Minimum Receiver Eye Width	0.4			UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.

Table 63. Differential Receiver (RX) Input Specifications



Package Description

18.1 Package Parameters for the MPC8572E FC-PBGA

The package parameters are as provided in the following list. The package type is $33 \text{ mm} \times 33 \text{ mm}$, 1023 flip chip plastic ball grid array (FC-PBGA).

Package outline	33 mm × 33 mm
Interconnects	1023
Ball Pitch	1 mm
Ball Diameter (Typical)	0.6 mm
Solder Balls	63% Sn
	37% Pb
Solder Balls (Lead-Free)	96.5% Sn
	3.5% Ag



18.2 Mechanical Dimensions of the MPC8572E FC-PBGA

Figure 61 shows the mechanical dimensions of the MPC8572E FC-PBGA package with full lid.



Figure 61. Mechanical Dimensions of the MPC8572E FC-PBGA with Full Lid

NOTES:

- 1. All dimensions are in millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M-1994.
- 3. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
- 4. Maximum solder ball diameter measured parallel to datum A.



Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
D1_MCAS	Column Address Strobe	AC9	0	GV _{DD}	
D1_MRAS	Row Address Strobe	AB12	0	GV _{DD}	
D1_MCKE[0:3]	Clock Enable	M8, L9, T9, N8	0	GV _{DD}	11
D1_MCS[0:3]	Chip Select	AB9, AF10, AB11, AE11	0	GV _{DD}	_
D1_MCK[0:5]	Clock	V7, E13, AH11, Y9, F14, AG10	0	GV _{DD}	
D1_MCK[0:5]	Clock Complements	Y10, E12, AH12, AA11, F13, AG11	0	GV _{DD}	
D1_MODT[0:3]	On Die Termination	AD10, AF12, AC10, AE12	0	GV _{DD}	_
D1_MDIC[0:1]	Driver Impedance Calibration	E15, G14	I/O	GV _{DD}	25
	DDR SDRAM Mem	ory Interface 2		•	
D2_MDQ[0:63]	Data	A6, B7, C5, D5, A7, C8, D8, D6, C4, A3, D3, D2, B4, A4, B1, C1, E3, E1, G2, G6, D1, E4, G5, G3, J4, J2, P4, R5, H3, H1, N5, N3, Y6, Y4, AC3, AD2, V5, W5, AB2, AB3, AD5, AE3, AF6, AG7, AC4, AD4, AF4, AF7, AH5, AJ1, AL2, AM3, AH3, AH6, AM1, AL3, AK5, AL5, AJ7, AK7, AK4, AM4, AL6, AM7	I/O	GV _{DD}	_
D2_MECC[0:7]	Error Correcting Code	J5, H7, L7, N6, H4, H6, M4, M5	I/O	GV _{DD}	
D2_MAPAR_ERR	Address Parity Error	N1	Ι	GV _{DD}	
D2_MAPAR_OUT	Address Parity Out	W2	0	GV _{DD}	
D2_MDM[0:8]	Data Mask	A5, B3, F4, J1, AA4, AE5, AK1, AM5, K5	0	GV _{DD}	
D2_MDQS[0:8]	Data Strobe	B6, C2, F5, L4, AB5, AF3, AL1, AM6, L6	I/O	GV _{DD}	_
D2_MDQS[0:8]	Data Strobe	C7, A2, F2, K3, AA5, AE6, AK2, AJ6, K6	I/O	GV _{DD}	—
D2_MA[0:15]	Address	W1, U4, U3, T1, T2, T3, R1, R2, T5, R4, Y3, P1, N2, AF1, M2, M1	0	GV _{DD}	_

Table 76. MPC8572E Pinout Listing (continued)



Table 76. MPC8572E Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes	
- 25. When exceptions in DDD2 mode, economic Dr. MDIC[0] to except dthrough d0.2.0. (full attemptible mode) or 20.4.0. (holf attemptible						

25. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor, and connect Dn_MDIC[1] to GVDD through 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor, and connect Dn_% resistor, and connect Dn_MDIC[1] to GVDD through 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.

- 26. These pins should be connected to XVDD_SRDS1.
- 27. These pins should be pulled to ground (XGND_SRDS1) through a 300- Ω (±10%) resistor.
- 28. These pins should be left floating.
- 29. These pins should be pulled up to TVDD through a 2–10 K Ω resistor.
- 30. These pins have other manufacturing or debug test functions. It is recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
- 31. DDRCLK input is only required when the MPC8572E DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting cfg_ddr_pll[0:2]=111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the MPC8572E PowerQUICC[™] III Integrated Host Processor Family Reference Manual Rev.0, Table 4-3 in section 4.2.2 "Clock Signals", section 4.4.3.2 "DDR PLL Ratio" and Table 4-10 "DDR Complex Clock PLL Ratio" for more detailed description regarding DDR controller operation in asynchronous and synchronous modes.
- 32. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
- 33. These pins should be pulled to ground (GND).
- 34. These pins are sampled at POR for General Purpose configuration use by software. Their value has no impact on the functionality of the hardware.

Table 78. Memory Bus Clocking Specifications

Characteristic	Min	Мах	Unit	Notes
Memory bus clock frequency	200	400	MHz	1, 2, 3, 4

Notes:

- 1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," Section 19.3, "e500 Core PLL Ratio," and Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
- 2. The Memory bus clock refers to the MPC8572E memory controllers' Dn_MCK[0:5] and Dn_MCK[0:5] output clocks, running at half of the DDR data rate.
- 3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
- 4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio." The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

As a general guideline when selecting the DDR data rate or platform (CCB) frequency, the following procedures can be used:

- Start with the processor core frequency selection;
- After the processor core frequency is determined, select the platform (CCB) frequency from the limited options listed in Table 80 and Table 81;
- Check the CCB to SYSCLK ratio to verify a valid ratio can be choose from Table 79;
- If the desired DDR data rate can be same as the CCB frequency, use the synchronous DDR mode; Otherwise, if a higher DDR data rate is desired, use asynchronous mode by selecting a valid DDR data rate to DDRCLK ratio from Table 82. Note that in asynchronous mode, the DDR data rate must be greater than the platform (CCB) frequency. In other words, running DDR data rate lower than the platform (CCB) frequency in asynchronous mode is not supported by MPC8572E.
- Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 79:

- SYSCLK input signal
- Binary value on LA[29:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that, in synchronous mode, the DDR data rate is the determining factor in selecting the CCB bus frequency, because the CCB frequency must equal the DDR data rate. In asynchronous mode, the memory bus clock frequency is decoupled from the CCB bus frequency.



Table 81 describes the clock ratio between e500 Core1 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LWE[0]/LBS[0]/LFWE, UART_SOUT[1], and READY_P1 signals at power up, as shown in Table 81.

<u>Bina</u> ry <u>Value</u> of <u>L</u> WE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio	<u>Bina</u> ry V <u>alue</u> of <u>L</u> WE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals	e500 Core1:CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2 (2.5:1)
010	Reserved	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

Table 81.	e500	Core1	to	ССВ	Clock	Ratio

19.4 DDR/DDRCLK PLL Ratio

The dual DDR memory controller complexes can be synchronous with, or asynchronous to, the CCB, depending on configuration.

Table 82 describes the clock ratio between the DDR memory controller complexes and the DDR PLL reference clock, DDRCLK, which is not the memory bus clock. The DDR memory controller complexes clock frequency is equal to the DDR data rate.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for both DDR controllers to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 82 reflects the DDR data rate to DDRCLK ratio, because the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode. MPC8572E does not support running one DDR controller in synchronous mode and the other in asynchronous mode.

Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio
000	3:1
001	4:1
010	6:1
011	8:1
100	10:1

Table 82. DDR Clock Ratio



Table 85 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R _N	45 Target	18 Target (full strength mode) 36 Target (half strength mode)	Z ₀	Ω
R _P	45 Target	18 Target (full strength mode) 36 Target (half strength mode)	Z ₀	Ω

Table 85. Impedance Characteristics

Note: Nominal supply voltages. See Table 1, $T_i = 105^{\circ}C$.

21.8 Configuration Pin Muxing

The MPC8572E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio, DDR complex PLL and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary



System Design Information

logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- TRST should be tied to HRESET through a 0 k Ω isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.



System Design Information

21.10.3 SerDes 2 Interface (SGMII) Entirely Unused

If the high-speed SerDes 2 interface (SGMII) is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD2_TX[3:0]
- <u>SD2_TX[3:0]</u>
- Reserved pins: AF26, AF27

The following pins must be connected to XGND_SRDS2:

- SD2_RX[3:0]
- $\overline{\text{SD2}_RX}[3:0]$
- SD2_REF_CLK
- SD2_REF_CLK

The POR configuration pin cfg_srds_sgmii_en on UART_RTS[1] can be used to power down SerDes 2 block for power saving. Note that both SVDD_SRDS2 and XVDD_SRDS2 must remain powered.

21.10.4 SerDes 2 Interface (SGMII) Partly Unused

If only part of the high speed SerDes 2 interface (SGMII) pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD2_TX[3:0]
- <u>SD2_TX[3:0]</u>
- Reserved pins: AF26, AF27

The following pins must be connected to XGND_SRDS2:

- SD2_RX[3:0]
- <u>SD2_RX[3:0]</u>



22 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 22.1, "Part Numbers Fully Addressed by this Document."

22.1 Part Numbers Fully Addressed by this Document

Table 86 through Table 88 provide the Freescale part numbering nomenclature for the MPC8572E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

MPC	nnnn	е	t	1	рр	ffm	r
Product Code ¹	Part Identifier	Security Engine	Temperature	Power	Package Sphere Type ²	Processor Frequency/ DDR Data Rate ³	Silicon Revision
MPC PPC	8572	E = Included	Blank = 0 to 105°C C = −40 to 105°C	Blank = Standard L = Low	PX = Leaded, FC-PBGA VT = Pb-free,	AVN = 1500-MHz processor; 800 MT/s DDR data rate	E = Ver. 2.2.1 (SVR = 0x80E8_0022) SEC included
		Blank = Not included	*		FC-PBGA* VJ = Fully Pb-free FC-PBGA ⁵	AUL = 1333-MHz processor; 667 MT/s DDR data rate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	E = Ver. 2.2.1 (SVR = 0x80E0_0022) SEC not included

Notes:

- ¹ MPC stands for "Qualified."
- PPC stands for "Prototype"
- ² See Section 18, "Package Description," for more information on the available package types.
- ³ Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- 4. The VT part number is ROHS-compliant with the permitted exception of the C4 die bumps.
- 5. The VJ part number is entirely lead-free. This includes the C4 die bumps.



Ordering Information

MPC	nnnn	е	t	1	рр	ffm	r
Product Code ¹	Part Identifier	Security Engine	Temperature	Power	Package Sphere Type ²	Processor Frequency/ DDR Data Rate ³	Silicon Revision
MPC PPC	8572	E = Included	Blank = 0 to 105°C C = −40 to 105°C	Blank = Standard L = Low	PX = Leaded, FC-PBGA VT = Pb-free,	AVN = 150- MHz processor; 800 MT/s DDR data rate	D= Ver. 2.1 (SVR = 0x80E8_0021) SEC included
		Blank = Not included			FC-PBGA	AUL = 1333-MHz processor; 667 MT/s DDR data rate ATL = 1200-MHz processor; 667 MT/s DDR data rate	D= Ver. 2.1 (SVR = 0x80E0_0021) SEC not included
						ARL = 1067-MHz processor; 667 MT/s DDR data rate	

Table 87. Part Numbering Nomenclature—Rev 2.1

Notes:

¹ MPC stands for "Qualified."

PPC stands for "Prototype"

² See Section 18, "Package Description," for more information on the available package types.

³ Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

Table 88. Part Numbering Nomenclature—Rev 1.1.1

MPC	nnnn	е	t	рр	ffm	r
Product Code ¹	Part Identifier	Security Engine	Temperature	Package Sphere Type ²	Processor Frequency/ DDR Data Rate ³	Silicon Revision
MPC PPC	8572	E = Included Blank = Not included	Blank=0 to 105°C C= −40 to 105°C	PX = Leaded, FC-PBGA VT = Pb-free, FC-PBGA	AVN = 1500-MHz processor; 800 MT/s DDR data rate AUL = 1333-MHz process or; 667 MT/s DDR datarate ATL = 1200-MHz processor; 667 MT/s DDR data rate ARL = 1067-MHz processor; 667 MT/s DDR data rate	B = Ver. 1.1.1 (SVR = 0x80E8_0011) SEC included B = Ver. 1.1.1 (SVR = 0x80E0_0011) SEC not included

Notes:

¹ MPC stands for "Qualified."

PPC stands for "Prototype"

² See Section 18, "Package Description," for more information on the available package types.